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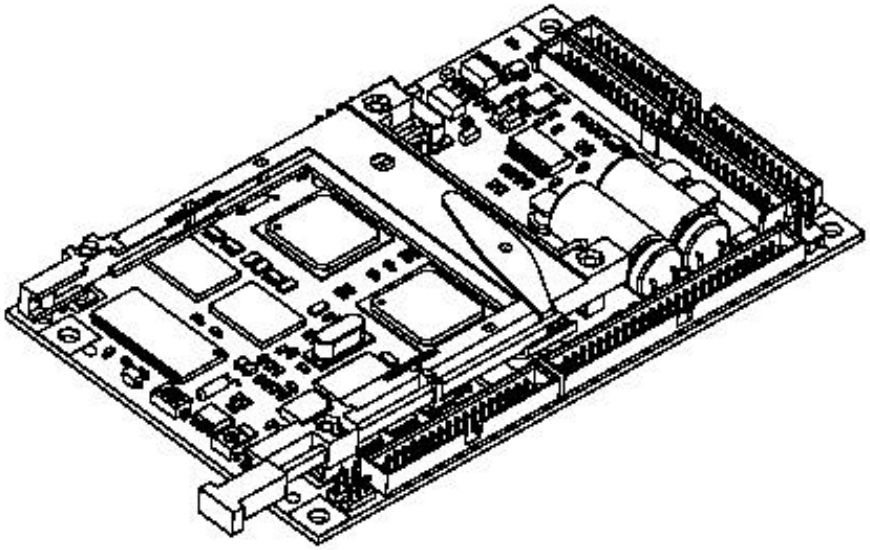
Embedded Computer Systems

Bitsy Plus
User's Manual



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About the Cover Image

The cover image shows a Rev A Bitsy Plus populated with the supercapacitor option.

Printing this Manual

This manual has been designed for printing on both sides of a 8.5x11 inch paper, but can be printed single-sided as well. It has also been optimized for use in electronic form with active cross-reference links for quick access to information.

Revision History

This table summarizes the changes made between revisions of this manual.

REV	DESCRIPTION	DATE/BY
6	Initial release	11/04/02 ak
A	**Product Specification Changes and Updates** Add Vcc and Vddx sleep current specs (6.2.4) Add power consumption measurements and plots (6.2.5)Change ADSmartIO PA5 from VBATT_NEG to DC_GOOD (4.3.7, 6.2.1) Change DCIN_POS parameter to VBATT_POS, reduce minimum voltage from 6 to 5 V and add note 15. Add Vsleep,hyst parameter and note (6.2.1) Lower Vsleep voltage specification (6.2.1) Update value for Rtl (6.2.6, 7.2.5) Update value for Rp pcmcia (6.2.12) Add max current drain on Vref (6.2.6) Add specs for PCMCIA VS and CD pull-up voltage and resistance (6.2.12) Add contrast circuit power specifications to section 6.2.2. Add note about analog input resolution (6.2.6) Indicate that PD0 and PD1 are for dedicated functions and not available for general purpose use (3.3.8, 4.3.7) Increase 5 V PCMCIA/CF socket power to 2.5W (6.2.12)	5/2/2003 ak

A	**New Information** Update PD3 from /RqOnOff to CPLD wakeup in section 4.3.7 Update SA-1110 signal cross-reference (4.1.6) with GP11 and GP12 changes Add notes about the USB_Reconn signal in sections 3.3.3 and 4.5.2. Add ADSmartIO voltage reference power control to section 5.3.2 and 6.2.6. Expand information about A/Ds and digital I/Os in section 1.2.6 Expand information about connections for external interrupt sources, section 4.1.4 Add section 5.4.2, *Power Loads During Sleep* Add cross-references to section 3.3.1 (J1). Expand introduction to section 5.2 Add note about /BacklightOn changes in Revision History (7.2.1) Add FAQ about LEDs in section 2.2 Add introduction to section 4.5 Add details about processor voltages (6.2.10) Expand information about PCMCIA/CF current leaks during sleep (6.2.12) Add "Printing this Manual" section Add pin direction information to pinouts (3.3) Add note about change in 3.3V PCMCIA power control (7.2.4) Add information about driver of LED; expand note about GP20, which is shared by LED0/DTR1 (3.1.2) Add rev. 5 Vref and /RqOnOff changes to power management diagram (5.3.2) Add diagram of audio architecture (6.2.9) Update mechanical drawing and clearances (6.1.1) and note lower height profile (7.2.4) Add 5-wire touch panel signal names to J3 signal table (3.3.3) Add detail about availability of 128 MiB RAM (1.2.3, 4.1.2) Remove unimplemented "Reset CPU" feature from ADSmartIO table (4.3.2) Update USB wording and add details about the USB_Reconn signal (4.5.2) Add USB devices to 5V and Sleep loads (5.4.1, 5.4.2) Credit Linear Tech for "Burst Mode" (5.3.8) Change diode in battery charger to fuse (5.5.3) Clarified USB_PWR_SENSE and USB_PWR_CTRL voltage specs (6.2.8) Add section 5.3.3, *System Sleep*	

A	**Clarifications** Clarify availability of A/Ds in section 4.3.4 Update backlight power section (5.3.6) to clarify that backlight power is not handled by the Bitsy Plus Add to Rev 2 Revision History that EIOn I/Os can source/sink more current Update signal tables to include analog and open-collector signal types; indicate direction of power signals Clarify how SPI chip select controlled (4.5.3) Clarify that OS can put the system to sleep when power fails (5.2.2) Clarify that voltage ref for ADSmartIO A/Ds is not software controlled; it is turned off when system is asleep (5.3.2, 7.2.5) Add 64 MiB flash and footnote about availability (1.2.3) Add note about Vsleep and wakeup (5.3.4) Add Note 4 about Vsleep (6.2.1) Add sleep current notes 16 and 17 (6.2.4)	
A	**Corrections** Correct reversal of MOSI and MISO signals in section 3.3.3 and add signal name details in section 4.5.3. Correct usage of GP 27 in table of section 4.1.6 (not available on J3) Correct error: JP3 does not control panel data voltage. Sections updated: 3.2.1(remove note), 4.6.2 and 4.6.3 (correct text), 6.2.2 (add information about R288 and R289) Correct Serial 1 connector (J1 to J10) (4.1.6) Remove extra close parenthesis in Icharge equation of section 5.3.7 Correct ADSmartIO cross-reference (4.3.1) Correct "Vdd" to "V" in controller specs and remove reference to PowerEnable (6.2.7) Correct information about JP3 and LED; add diagram of LED circuit (3.1.2) Correct IrDAOn notes: no pull-up (3.3.3) Update and correct power supply diagram (esp. 3.3V powered from DC_IN); add notes about factory options (5.3.1) Correct Note 13 (6.2.2) to indicate that Vee and Vcon available concurrently Correct typo: LLD to LDD	

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Table of Contents

1 Introduction

1.1 Overview

The Bitsy Plus is a full-featured single board computer using the SA-1110 StrongARM RISC microprocessor and SA-1111 Companion Chip. The Bitsy Plus is designed to meet the needs of embedded and graphical systems developers.

This manual applies to Revision A of the Bitsy Plus. The revision history of the Bitsy Plus is listed in chapter 7.

1.2 Features

1.2.1 Processor

- SA-1110 32-bit StrongARM
- SA-1111 Companion Chip
- Clock rates up to 206 MHz
- Battery-Backed Real-Time Clock

1.2.2 Power Supply

- 6-15 V Input Range
- Battery Trickle Charger

1.2.3 Memory

- 16, 32, 64 or 128 [1] MiB[2] synchronous DRAM
- 8, 16, 32 or 64 [3] MiB Flash
- PCMCIA and CompactFlash[4] (CF), Type I and II, 3.3 and 5 V
- Supports CF cards with optional personality board

1.2.4 Communications

- USB 1.1 Host port (low 1.5 Mbit/s and full 12 Mbit/s speeds) and full speed Client port
- Three Serial Ports
  - Serial 1: RS-232, 3.3V CMOS (9-wire)
  - Serial 2: 3.3V CMOS (3-wire); IrDA and RS-232 with optional personality board
  - Serial 3: RS-232, 3.3V CMOS (5-wire)

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[1] The Bitsy Plus supports 128 MiB SDRAM. However, those components are not yet commercially available as of April 2003.

[2] MiB is the IEC abbreviation for mebibyte = 2^{20} byte = 1 048 576 byte. The kibi and mebi abbreviations are based on the 1998 IEC standard for binary multiples. For further reading, see the US NIST web site, http://physics.nist.gov/cuu/Units/binary.html

[3] The Bitsy Plus supports synchronous and asynchronous flash. The 64 MiB flash option is available only in synchronous flash.

[4] CompactFlash is a trademark of the CompactFlash Association, http://www.compactflash.org/.

- 10/100BT Ethernet, RJ45 (with optional personality board)
- CompactFlash Interface (with optional personality board)

1.2.5 User Interface and Display

- Flat Panel Interface
- Software-Controlled VEE Generator for passive LCD contrast control
- Analog Touch Panel Interface (four- or five-wire options)
- External PS/2 Keyboard Support

1.2.6 I/O

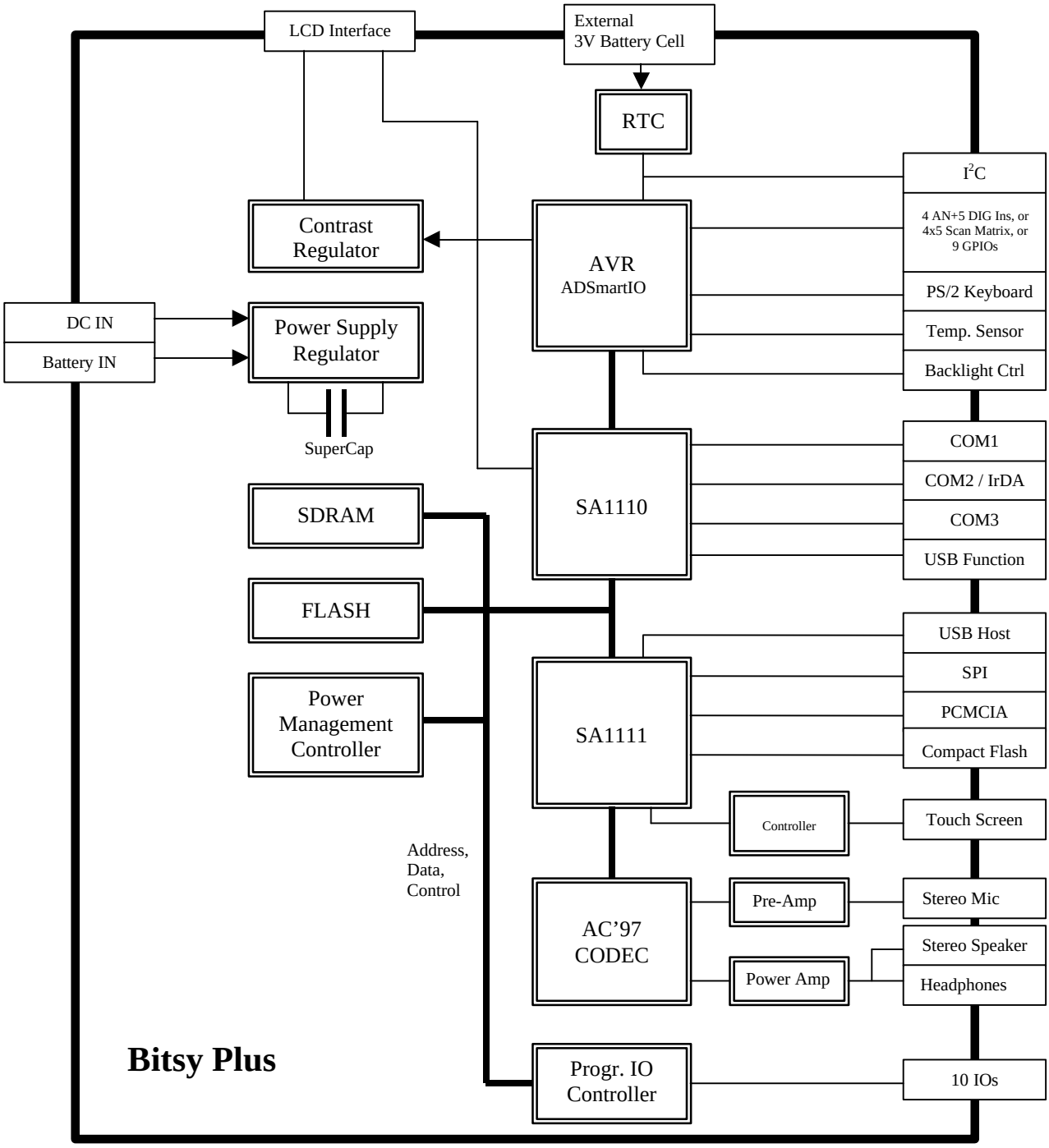
- Nine ADSmartIO™ ports configurable for digital I/O, A/D inputs (up to four) and/or up to 4x5 keypad
- Ten digital I/Os
- Backlight Control Signals for Intensity and On/Off
- External Temperature Probe support

1.2.7 Audio Interface

- AC'97 Codec
- Stereo Microphone Input
- Stereo 1W Speaker Outputs
- Headphone Output

1.3 Block Diagram

The following diagram illustrates the system organization of the Bitsy Plus.



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2 Getting Started

2.1 Development Systems

Bitsy Plus boards are shipped as development systems designed to get the developer up and running quickly.

To use the system, simply plug power supply into the mini DIN-8 receptacle on the system.

If the screen does not display anything after five to ten seconds, check the *Frequently Asked Questions*, below. Most operating systems cold boot within twenty seconds.

2.1.1 System Components

A typical development system consists of the following:

- Bitsy Plus single-board computer
- Bitsy Personality Board with CompactFlash or 10/100BT Ethernet
- Flat panel display and cable
- Backlight inverter and cable
- Touch screen and cable
- 120 VAC power adapter
- Plexiglas mounting
- Developer's Cable Kit including
  - Serial Port DB9 adapter (ADS cable #610111-80001)
  - DB9F/F null modem cable
- Operating system of your choice
- User's Guide (this document and operating system guide)

Please make sure you have received ***all*** the components before you begin your development.

2.1.2 Bitsy Plus Personality Boards

The Bitsy Plus often works in tandem with another board to add functionality and customize the system for its application. Personality boards can add custom circuits and locate connectors best suited for the application design.

In production volumes, the Bitsy Plus can be built with interface connectors J1, J3, J9 and J10 on the underside of the board. This allows the Bitsy rest above custom personality boards rather than below them.

At the time of writing, ADS supplies a reference design for personality board. Schematics are and user manuals available on the ADS support site. The ADS design can be populated as either a "CF" or "Ethernet" personality board.

ADS CF Personality Board

The CF Personality board breaks out signals to the Bitsy for a wide range of functions including USB, audio, keyboard, power, serial, LCD display, backlight, IrDA and touch screen. It also includes a reset button and CF socket.

For further details about this board, please consult the Personality Board user's manual, ADS document #110111-8001.

ADS Ethernet Personality Board

The Ethernet Personality Board uses the same circuit board as the ADS CF Personality Board. An RJ-45 jack replaces the CF socket, and the board adds an SMSC LAN91C111 10/100 Ethernet chip and associated line drivers. Otherwise, the board is identical to the CF Personality Board.

2.2 Frequently Asked Questions

The following are some of the most commonly asked questions for development systems:

Q: When I plug in power, my screen is white and nothing comes up on it.

A: Check the connector seating. The flat panel connector may have come loose in shipping. Press it firmly into the panel and reapply power to your system.

Q: When I plug in power, my screen stays black.

A: If your system has supercapacitors installed (section 5.3.3), your system may be asleep. Try waking up the system by shorting the wakeup signal (J3 pin 45) to ground. Development systems include a two-pin header on the personality board whose pins can be shorted together to wake the system. You may also press the reset button to fully restart the system.

Q: When I plug in power, the LED doesn't turn on.

A: Your system may still be booting. The LED is software controlled and is not necessarily turned on at boot.

Q: Do I have to turn off the system before I insert a PCMCIA or CompactFlash card?

A: No. The Bitsy Plus supports hot-swapping of PCMCIA and CompactFlash cards. Consult the operating system documentation for details.

Q: Do I need to observe any ESD precautions when working with the system?

A: Yes. If possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the board or touching any components on the board.

Q: What do I need to start developing my application for the system?

A: You will need a flash ATA card (16 MiB or larger, 32 MiB recommended) and the cables supplied with your system to interface your development station to the system. For further direction, consult the ADS guide for the installed operating system.

Q: Who can I call if I need help developing my application?

A: ADS provides technical support to get your development system running. For customers who establish a business relationship with ADS, we provide support to develop applications and drivers.

Q: Is there online support?

A: Yes. Information about the Bitsy Plus hardware and software is available on the ADS support site at http://www.applieddata.net/support. See section 2.4 for further details.

Q: Can I upgrade the version of the operating system?

A: Yes. ADS provides regular operating system updates on its developers' web site. For operating systems not maintained by ADS, contact the operating system vendor.

Q: I would like to interface to a different display panel. How can I do this?

A: ADS may have already interfaced to the panel you are interested in. Consult ADS for availability.

2.3 Organization of this Manual

The manual organizes information in five key sections:

Introduction	Provides an overview of the functionality and organization of the Bitsy Plus, as well as how to use this manual.
Hardware Reference	Describes the configuration settings and pinouts for all connectors and jumpers on the Bitsy Plus.
Feature Reference	Gives details about the various subsystems of the Bitsy Plus.
Power Management	Provides key information about power management, tips for system integration and electrical and mechanical interface specifications.
Specifications	Electrical and mechanical interface specifications.

To locate the information you need, try the following:

1. Browse the *Table of Contents.* Section titles include connector designators and their function.
2. Follow cross-references between sections.
3. View and search this manual in PDF format

2.4 Errata, Addenda and Further Information

Errata and addenda to this manual are posted on the ADS support forums along with the latest release of the manual. Consult the support forums any time you need further information or feel information in this manual is in error. You may access the forums from the ADS support site,

http://www.applieddata.net/Support

In addition to manuals, the support forums include downloads, troubleshooting guides, operating system updates and answers to hundreds of questions about developing applications for ADS products. You may also post questions you have about ADS products on the forums.

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3 Hardware Reference

This section gives an overview of the hardware features of the Bitsy Plus. This overview includes a description of the switches, jumper settings, connectors and connector pinouts.

Many connectors and headers have a visible number or marking on the board that indicates pin 1. If that pin is not clearly marked, there are two other ways to locate pin 1:

1. The easiest method is to look at the underside of the board. The square pad is pin 1.

2. Download the mechanical drawing of the Bitsy Plus available on the ADS Support site (section 2.4). The square or indicated pad on each connector is pin 1.

3.1 Switches and Indicators

3.1.1 S1: DIP Switch

S1 is a two-position DIP switch. When in the "ON" position, switches are closed and connect to ground. Otherwise they are pulled up.

DIP switch positions "1" and "2" connect to the SA-1111.

Most operating systems on the Bitsy Plus reserve these switches for their use. Consult the operating system manual for details.

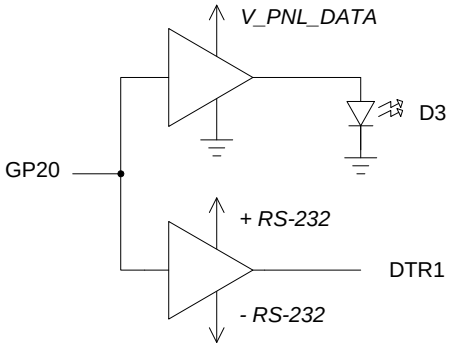
3.1.2 LED Indicator

The Bitsy Plus has one onboard LED mapped as follows:

Signal	GPIO line	Part Designator	Color
LED0	*20*	*D3*	*Green*

LED0 shares StrongARM GPIO20 with the DTR signal of Serial 1 (J10), as shown at right. The LED is not available for application use when the DTR line is in use by the Serial 1 driver.

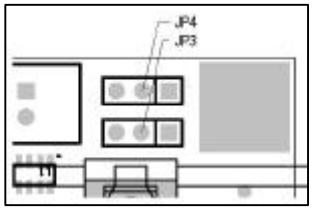
The LED is driven by the same buffers as the display driver data lines. The LED will be off when the display buffers are disabled (see power management section 5.3.2).



3.2 Jumper Settings

Jumpers on the Bitsy Plus select a variety of operational modes. All use 2mm shorting blocks (shunts) to select settings. Make sure power is turned off to the Bitsy Plus when changing the position of a shunt.

JP3 and JP4 are located at the corner of the board near the PCMCIA ejector as shown at right:



3.2.1 JP3: Flat Panel Power Select

Type: 3-post header, 2mm

This jumper selects the supply voltage for the flat panel. It is located near the PCMCIA ejector button.

Jumper setting	Voltage Selected
1-2	*Vddx (3.3 V)*
2-3	*Vcc (5.0 V)*

WARNING! Make sure you have selected the correct voltage before connecting the panel. Flat panels are notoriously sensitive to--and are often irreparably damaged by--incorrect voltages.

3.2.2 JP4: Vee Polarity Select

Type: 3-post header, 2mm

This jumper selects the polarity of Vee, the contrast control voltage for passive displays. Vee is controlled with a PWM signal from the ADSmartIO (section 4.3). See section 4.6.7 for further details bout Vee.

Jumper setting	Vee
1-2	*positive*
2-3	*negative*
n/c	*no Vee*

3.3 Connector Pinouts

The following tables describe connector pinouts and the type of connector. At least one pin of every connector is labeled on the Bitsy Plus. Pin 1 of the connector is also typically indicated by a square pad where the pin is soldered to the board.

```
2 4 6 8...
1 3 5 7...
```

As seen from the component side[5], double-row headers on the board are all numbered as shown in the figure to the right.

For information about the location of the connectors on the Bitsy Plus, refer to section 6.1.1.

Legend:

n/c	Not connected
GND	Bitsy Plus ground plane
(3.3)	Reference sections for signals
I	signal is an input to the system
O	signal is an output from the system
IO	signal may be input or output
P	power and ground
A	analog signals
OC	open collector output

[5] The "component side" of the Bitsy Plus is the one on which the PCMCIA ejector is installed. As a factory option, some connectors may be installed on the "bottom side" of the Bitsy Plus.

3.3.1 J1: LCD Panel Interface Connector

Board Connector: Samtec #STMM-117-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-117-02-F-D-500)

The following table describes the signals on the LCD interface connector. Signal names shown are for TFT active matrix color LCDs at 16 bpp (bit-per-pixel). For other color depths and LCD technologies, consult the table in section 4.6.4. Signals from the StrongARM are buffered and RFI filtered before reaching J1. See section 4.6 for further details about displays.

Pin	SA-1110 Signal Name	Color Active TFT Display at 16bpp	
		ADS Signal Name	Description
1		*PNL_VEE*	*V_{EE} (contrast); see JP4*
2		*GND*	*ground*
3	*L-PCLK*	*PNL_PIXCLK*	*Pixel Clock*
4	*L-LCLK*	*PNL_HSYNC*	*Horizontal Sync.*
5	*L-FCLK*	*PNL_VSYNC*	*Vertical Sync.*
6		*GND*	*ground*
7	*LDD15*	*PNL_RED0*	*Red Bit 0*
8	*LDD11*	*PNL_RED1*	*Red Bit 1*
9	*LDD12*	*PNL_RED2*	*Red Bit 2*
10	*LDD13*	*PNL_RED3*	*Red Bit 3*
11	*LDD14*	*PNL_RED4*	*Red Bit 4*
12	*LDD15*	*PNL_RED5*	*Red Bit 5*
13		*GND*	*ground*
14	*LDD5*	*PNL_GREEN0*	*Green Bit 0*
15	*LDD6*	*PNL_GREEN1*	*Green Bit 1*
16	*LDD7*	*PNL_GREEN2*	*Green Bit 2*
17	*LDD8*	*PNL_GREEN3*	*Green Bit 3*
18	*LDD9*	*PNL_GREEN4*	*Green Bit 4*
19	*LDD10*	*PNL_GREEN5*	*Green Bit 5*
20		*GND*	*ground*
21	*LDD4*	*PNL_BLUE0*	*Blue Bit 0*
22	*LDD0*	*PNL_BLUE1*	*Blue Bit 1*
23	*LDD1*	*PNL_BLUE2*	*Blue Bit 2*
24	*LDD2*	*PNL_BLUE3*	*Blue Bit 3*
25	*LDD3*	*PNL_BLUE4*	*Blue Bit 4*
26	*LDD4*	*PNL_BLUE5*	*Blue Bit 5*
27		*GND*	*ground*
28	*L-BIAS*	*PNL_LBIAS*	*Data_Enable*
29		*PNL_PWR*	*Vcc (5 V) or 3.3 V (JP3)*
30			
31		*PNL_RL*	*Horizontal Mode Select (set by R22 or R87)*
32		*PNL_UD*	*Vertical Mode Select (set by R79 or R17)*
33	*ADSmartIO PD0*	*PNL_ENA*	*Panel enable signal*
34		*VCON*	*low-voltage adjust for contrast control of some displays (6.2.2)*

3.3.2 J2: PCMCIA

Integrated ejector: FCI #95620-050CA

The 68-pin PCMCIA socket conforms to the PCMCIA standard for 5V-tolerant Type II cards, and can also be run at 3.3 V. The socket is normally de-energized; the operating system is responsible for turning on the socket when a card is inserted and turning it off when the card is removed. Ejector hardware is standard.

Vpp (pins 18 and 52), which is 12 V in older PCMCIA implementations, is left unconnected in this implementation. See section 6.2.12 for electrical specifications.

3.3.3 J3: Power, I/O, Serial 2 & 3, USB, Touch Screen and others

Board Connector : Samtec #STMM-125-02-T-D

Recommended Mating Connector: Samtec # TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-125-02-F-D-500)

Pin	Name	Pin	Type	Description		
1	*EIO9*		*IO*	*Digital I/Os (6.2.7)*		
	EIO8	*2*	*IO*			
3	*EIO7*		*IO*			
	GND	*4*	*P*	*ground*		
		6				
	VCC	*8*	*PO*	*+5 V*		
		10				
5	*TEMP_SENSOR_MINUS*		*AI*	*External Temperature Probe Connection (4.3.5)*		
7	*TEMP_SENSOR_PLUS*		*PO*			
9	*/IRDAON*		*O*	*External IRDA control output*		
11	*TSPX*		*AIO*	*right*	*UL*	*Touch screen (6.2.3)*
13	*TSMY*		*AIO*	*top*	*LR*	
15	*TSMX*		*AIO*	*left*	*LL*	
17	*TSPY*		*AIO*	*bottom*	*UR*	
	EIO5	*12*	*IO*	*Digital I/Os (6.2.7)*		
	EIO6	*14*	*IO*			
	BACKLIGHT PWM	*16*	*AO*	*Backlight Intensity (PWM) (4.6.6, 6.2.2)*		
	/BACKLIGHT ON	*18*	*OC*	*Backlight On/Off (open-collector) (4.6.6, 6.2.2)*		
19	*RXD2T*		*I*	*Serial 2 (3.3 V CMOS) (4.5.1)*		
	TXD2T	*20*	*O*			
21	*WIPER*		*AI*	*Touch screen wiper (optional 5-wire touch)*		
	CHARGE	*22*	*O*	*Charge Enable output (PB0[6]) (5.3.7)*		
23	*GND*		*P*	*ground*		
	PE2	*24*	*O*	*Power Enable #2 for external devices (5.3.2)*		
25	*CTS3*		*I*	*Serial 3 (RS-232) (4.5.1)*		
	TXD3	*26*	*O*			
27	*RTS3*		*O*			
	RXD3	*28*	*I*			

[6] This output does not have any series resistance or ESD protection

Pin	Name	Pin	Type	Description	
29	*USB+*		*IO*	*USB Client (4.5.2)*	
	USB-	*30*	*IO*		
31	*GND*		*P*	*Ground*	
	HP_IN	*32*	*I*	*Headphone connected (4.4.2, 6.2.9)*	
33	*USB_RECONN*		*0*	*USB Client power management (4.5.2)* [6]	
	GND	*34*	*P*	*connects to ground through R281(0W)*	
	GND	*36*	*P*	*ground*	
35	*STXD*		*O*	*MOSI*	*SPI signals (4.5.3)*
37	*SRXD*		*I*	*MISO*	
39	*SCLK2*		*O*	*SCLK*	
43	*SFRM2*		*O*	*SS*	
	VBATT_POS	*38*	*PI*	*External Battery Input (5.3.7)*	
	VBATT_NEG	*40*	*P*		
41	*POWERENABLE*		*O*	*Power Supply Control Output (5.3.2)*	
	/PE1	*42*	*O*	*Power Enable #1 for external devices (5.3.2)*	
	DCIN_POS	*44*	*PI*	*External Power Input (also on J6)*	
		48			
45	*/RQONOFF*		*I*	*"Request On/Off" Switch Input (5.3.3, 6.2.1)*	
	GND	*46*	*P*	*ground*	
47					
49					
	BATPOS	*50*	*PI*	*Real-time clock backup battery (4.2, 6.2.4)*	

3.3.4 J4: Manufacturing Test Connector

Type: 2x3 header, 0.100-inch spacing

This header is used during manufacturing to load the ADSmartIO firmware. It is not supported for any other use.

3.3.5 J5: JTAG Connector

Type: 1x6 header, 0.100-inch spacing

This header is used during manufacturing to program the boot flash and onboard logic. It is intended for factory use.

3.3.6 J6: Input Power Connector

Board Connector: Molex #22-23-2021

Recommended mating connector: Molex 22-01-3027

These power inputs are also connected to J3. See Chapter 5 and section 6.2.3 for input power specifications.

Pin	Name	Type	Description
1	*DCIN_POS*	*PI*	*DC Power Input*
2	*GND*	*P*	*Ground*

3.3.7 J9: External CompactFlash / Expansion Bus

Board Connector : Samtec #STMM-125-02-T-D

Recommended Mating Connector: Samtec # TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-125-02-F-D-500)

The Bitsy Plus makes its CompactFlash bus signals available on J9. These signals can be used to add a CompactFlash socket to a daughter board or to expand the capabilities of the Bitsy Plus as a digital expansion bus. See section 4.1.5 for details.

Pin	Name	Pin	Type	Description
1	*GND*		*P*	*ground*
	/CARDBDET2	*2*	*I*	*Card Detect 2*
	/CARDB16	*4*	*I*	*16 Bit Access*
3	*PCBD10*		*IO*	*Data8-10*
5	*PCBD9*		*IO*	
7	*PCBD8*		*IO*	
	PCBD2	*6*	*IO*	*Data0-2*
	PCBD1	*8*	*IO*	
	PCBD0	*10*	*IO*	
9	*CARDBSTSCHG*		*I*	*Status Change*
11	*CARDBSPK*		*I*	*Speaker Input*
13	*/CARDBREG*		*O*	*Register Access*
15	*VCC*		*PO*	*5 V*
17	*/CARDBWAIT*		*I*	*Wait*
19	*CARDBRES*		*O*	*Reset*
21	*/CARDBVS2*		*I*	*Voltage Sense 2 Input*
	PCBA0	*12*	*O*	*Address0-6*
	PCBA1	*14*	*O*	
	PCBA2	*16*	*O*	
	PCBA3	*18*	*O*	
	PCBA4	*20*	*O*	
	PCBA5	*22*	*O*	
	PCBA6	*24*	*O*	
23	*+3.3V*		*P0*	*+3.3 V*
25	*/CARDBON*		*O*	*5 V Power Control*
	CARDBVCC	*26*	*PI*	*External Switched CardB Power Input*
27	*CARDBIRQ*		*I*	*Interrupt Signal*
29	*/CARDBMWR*		*O*	*Memory Write*
31	*/CARDBIOWR*		*O*	*IO Write*
33	*/CARDBIORD*		*O*	*IO Read*
	PCBA7	*28*	*O*	*Address7-10*
	PCBA8	*30*	*O*	
	PCBA9	*32*	*O*	
	PCBA10	*36*	*O*	
	/CARDBMRD	*34*	*O*	*Memory Read*
35	*/CARDB_VS1*		*I*	*Voltage Sense 1 Input*
37	*/CARDBCE2*		*O*	*Low Byte Chip Select*
	/CARDBCE1	*38*	*O*	*High Byte Chip Select*

Pin	Name	Pin	Type	Description
39	*PCBD15*		*IO*	*Data11-15*
41	*PCBD14*		*IO*	
43	*PCBD13*		*IO*	
45	*PCBD12*		*IO*	
47	*PCBD11*		*IO*	
	PCBD7	*40*	*IO*	*Data3-7*
	PCBD6	*42*	*IO*	
	PCBD5	*44*	*IO*	
	PCBD4	*46*	*IO*	
	PCBD3	*48*	*IO*	
49	*/CARDBDET1*		*I*	*Card Detect 1*
	/CARDBON_3P3V	*50*	*O*	*3.3 V Power Control*

3.3.8 J10: ADSmartIO, USB, Serial 1, Stereo Audio, I/Os

Board Connector : Samtec #STMM-125-02-T-D

Recommended Mating Connector: Samtec # TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-125-02-F-D-500)

Pin	Name	Pin	Type	Description	
1	*/EXT_IRQ1*		*I*	*External Interrupt 1 Input*	
3	*/EXT_IRQ2*		*I*	*External Interrupt 2 Input*	
5	*EIO4*		*IO*	*Digital I/Os (6.2.7)*	
	EIO3	*2*	*IO*		
	EIO2	*4*	*IO*		
	EIO1	*6*	*IO*		
	EIO0	*8*	*IO*		
7	*SIGPS2*		*IO*	*External PS/2 keyboard inputs*	
9	*CLKPS2*		*IO*		
	USB_PWR_ SENSE	*10*	*I*	*Sense Input from external USB host power switch (4.5.2)*	
	USB_PWR_ CTRL	*12*	*O*	*Discrete output to control external USB host power switch (4.5.2)*	
	USB_UDC-	*14*	*IO*	*USB Host (4.5.2)*	
	USB_UDC+	*16*	*IO*		
11	*SMTIO2*		*IO*	*PC6*	*RTC/I²C or ADSmartIO*[7]
13	*SMTIO1*		*IO*	*PD1*	*Thermistor energize (4.3.5)*
15	*SMTIO0*		*IO*	*PD0*	*Passive panel enable (PNL_ENA)*
	SPKR_L-	*18*	*AO*	*Stereo Speaker, left channel (4.4.2)*	
	SPKR_L+	*20*	*AO*		
	SPKR_R-	*22*	*AO*	*Stereo Speaker, right channel (4.4.2)*	
	SPKR_R+	*24*	*AO*		

[7] PC6 and PC7 are used for the I²C bus master interface. These communicate with the real-time clock and any I²C off-board devices, if installed. See sections 4.2 and 4.5.4 for details.

Pin	Name	Pin	Type	Description	
17	*ROW0*		*IO*	*PC0*	*ADSmartIO (see section 6.2.6)*
19	*ROW1*		*IO*	*PC1*	
21	*ROW2*		*IO*	*PC2*	
23	*ROW3*		*IO*	*PC3*	
25	*ROW4*		*IO*	*PC4*	
27	*COL0*		*IO*	*PA0*	
29	*COL1*		*IO*	*PA1*	
31	*COL2*		*IO*	*PA2*	
33	*COL3*		*IO*	*PA3*	
	RI1	*26*	*I*	*Serial 1 [8] (RS-232 with 3.3 V CMOS factory option) (4.5.1)*	
	DCD1	*28*	*I*		
	DSR1	*30*	*I*		
	DTR1	*32*	*O*		
	RXD1	*34*	*I*		
	TXD1	*36*	*O*		
	CTS1	*38*	*I*		
	RTS1	*40*	*O*		
35	*/EXT_IRQ3*		*I*	*External Interrupt 3 Input*	
37	*VDDX*		*PO*	*3.3 V*	
39	*MIC_GND*		*P*	*Microphone ground*	
41					
	MIC_L	*42*	*AI*	*Stereo Microphone Input*	
	MIC_R	*44*	*AI*		
43	*VREF*		*AO*	*ADSmartIO A/D reference voltage*	
45	*/RESET_IN*		*I*	*External Reset Input (6.2.1)*	
47	*VDDX*		*PO*	*3.3 V*	
	VCC	*46*	*PO*	*5 V*	
		48			
49	*SMTIO3*		*IO*	*PC7*	*RTC/I²C or ADSmartIO [9]*
	GND	*50*	*P*	*ground*	

[8] Serial 1 signals RTS, CTS, DCD, DTR, DSR and RI are controlled by the StrongARM GPIO lines. See section 4.1.6 for details.

[9] See footnote 7.

4 Feature Reference

This chapter provides details about the architecture and many features of the Bitsy Plus, and how they can fit together to create a system that meets your application needs.

4.1 System Architecture

4.1.1 Boot Code

The Bitsy Plus uses the first block of onboard flash to store the boot code. At the factory, boot code is loaded using the JTAG interface (J6, section 3.3.5). Most ADS Bitsy Plus boot loaders are field-upgradeable using a flash card on either the CompactFlash or PCMCIA port.

4.1.2 Synchronous DRAM

One bank of synchronous DRAM (SDRAM) can be populated for a system total of 16, 32, 64 or 128 MiB of RAM[10]. The data bus width is 32 bit.

The memory clock speed is one half the CPU core clock speed. Typical memory bus operation is at 103 MHz.

The self-refreshed RAM consumes most of the system sleep current. Sleep current increases roughly in direct proportion to the amount of RAM installed.

4.1.3 Non-Volatile Memory

There are several ways to store data on the Bitsy Plus that will survive a power failure. Some devices can only be accessed through operating system drivers, and not all are available for application data storage.

Flash Memory

Flash memory is the primary site for non-volatile data storage. The Bitsy Plus includes a bank of flash memory for non-volatile data storage. The board supports 8, 16 or 32 MiB of installed flash. The data bus width is 32 bit.

ADS systems store the operating system, applications and system configuration settings in the onboard flash. Most operating systems configure a portion of the flash as a flash disk, which acts like a hard disk drive.

ADSmartIO EEPROM

The ADSmartIO controller includes 256 bytes or more of EEPROM storage. ADS reserves a portion of this memory for future use. Drivers are not yet available for all operating systems.

CompactFlash and PCMCIA/ATA Cards

CF and ATA cards provide removable storage in a wide variety of capacities. These cards can be cost-effective means to expand system storage capacity for applications that provide access to the PCMCIA and CF slots. A CF slot must be placed on a daughter board, as it is not included on the Bitsy Plus.

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[10] 128 MiB SDRAM was not yet commercially available as of April 2003.

RTC NVRAM

The real-time clock chip includes 56 bytes of non-volatile RAM. The RAM is maintained as long as main or backup power is provided to the chip. Drivers are not yet available to access this feature. Contact ADS Sales if your application requires this feature.

4.1.4 Interrupts

The Bitsy Plus includes several sources for external interrupts. The following table summarizes the external interrupt sources and the devices to which they are connected.

Interrupt Signal	Pin	IRQ Handler
/RqOnOff	*J3.45*	*ADSmartIO*
CARDBIRQ	*J9.27*	*SA-1111*
/EXT_IRQ1	*J10.1*	*SA-1111, GPIO_B<5>*
/EXT_IRQ2	*J10.3*	*SA-1111, GPIO_B<4>*
/EXT_IRQ3	*J10.35*	*SA-1110, GP 10*

Your operating system may not include drivers for all interrupt sources.

4.1.5 CompactFlash / Expansion Bus

The Bitsy Plus makes its CompactFlash bus signals available on J9. These signals can be used to add a CompactFlash socket to a daughter board or to expand the capabilities of the Bitsy Plus as a digital expansion bus. The voltage of the bus signals are set by the CardBVcc voltage (3.3 V or 5 V).

The ADS Bitsy CF and Ethernet Personality Boards use this bus for CF and digital expansion, respectively. The schematic (ADS document number 640111-8000, available on the ADS Support Forums) illustrates how to use this bus both ways.

4.1.6 SA-1110 GPIO Cross-Reference

The following table describes how the Bitsy Plus utilizes the StrongARM GPIO lines (*GPn*). They are offered for reference purposes only. Most operating systems make this information transparent to developers.

GP	Signal Name	I/O[11]	Function, Connector
0	*SA1111_IRQ*	*I*	*SA-1111 interrupt*
1	*WAKE_UP*	*I*	*wakeup from ADSmartIO*
2	*LDD8*	*O*	*LCD display (J1)*
3	*LDD9*	*O*	
4	*LDD10*	*O*	
5	*LDD11*	*O*	
6	*LDD12*	*O*	
7	*LDD13*	*O*	
8	*LDD14*	*O*	
9	*LDD15*	*O*	
10	*EXT_IRQ3*	*I*	*External interrupt 3 (4.1.4)*
11	*CODEC_RES*	*O*	*Codec reset*
12	*USB_RECONN*	*O*	*USB Reconnect (J3)*
13	*IRQ_SSP*	*I*	*ADSmartIO interrupt*

[11] I=input, O=output

GP	Signal Name	I/O[11]	Function, Connector
14	*CTS1*	*I*	*Serial 1 (J10, 4.5.1)*
15	*RTS1*	*O*	
16	*RIB1*	*I*	
17	*DCD1*	*I*	
18	*CTS3*	*I*	*Serial 3 (J3, 4.5.1)*
19	*RTS3*	*O*	
20	*LED0/DTR1*	*O*	*LED0 or Serial 1 (J10)*
21	*GPIO21_MBGNT*	*O*	*SA-1111 Memory Request Bus Grant*
22	*GPIO22_MBREQ*	*I*	*SA-1111 Memory Bus Request*
23	*/IRDAON*	*O*	*IRDA enable (J3)*
24	*DSR1*	*I*	*Serial 1 (J3)*
25	*/RESET_AVR*	*O*	*Reset ADSmartIO*
26	*/SA1111_RESET*	*O*	*Reset SA-1111*
27	*GPIO27_CLK*	*O*	*System clock for use by SA-1111*

4.2 Real-Time Clock (RTC)

The Bitsy Plus uses the DS1307 real-time clock chip to maintain the system date and time when the system is powered down. The operating system typically reads the RTC on boot and wakeup, and sets the RTC when the system time or date is changed.

The RTC is powered from the BATPOS input. Connect a long-life 3 V battery to the BATPOS input (J3 pin 50) to maintain the system time.

The RTC is accessible through the ADSmartIO's I^2C bus (section 4.5.4). See section 6.2.4 for electrical specifications.

4.3 ADSmartIO

ADSmartIO™ is a RISC microcontroller on the Bitsy Plus that is programmed with ADS firmware. This device provides additional I/O functionality for specialized tasks. Your application software can configure the standard ADSmartIO for a variety of functions, such as digital I/O, PWM, A/D, I^2C, keypad scan and PS/2 keyboard operation.

4.3.1 Overview

The ADSmartIO controller has four, eight-pin I/O ports named PA, PB, PC and PD. Some of these ports' pins are used internally, while others are available for user applications. See the signal cross-reference in section 4.3.7 for details.

Generally, ADSmartIO ports are referenced by port and pin number (e.g. PA2), but I/O signals may go by several names based on its functionality. See the connector pinouts to cross-reference ADSmartIO signal names.

Electrical specifications for the ADSmartIO are listed in section 6.2.6. The *ADSmartIO Programmer's Reference* (ADS document 110110-4004) gives information about how to use the ADSmartIO features.

4.3.2 ADSmartIO Features

The following are some of the functions that the ADSmartIO can perform. The functions actually implemented depend on the firmware loaded on your system:

- General purpose digital I/O and A/D
- Keypad scan (section 4.3.6)
- PS/2 keyboard input
- Backlight on/off and brightness control (section 4.6.6)
- Contrast control for display (enabled only when pixel clock is running) (section 4.6.7)
- Read/set real-time clock (RTC) (section 4.2)
- Wakeup via RQONOFF signal (section 5.3.3)
- Trickle-charge a battery (section 5.3.7)
- Read a temperature sensor (section 4.3.5)
- Monitor system power
- Reset CPU

4.3.3 Digital I/Os

All available ports on the ADSmartIO controller can be individually configured as inputs or outputs. If you write a "1" to an I/O port when it is configured as an input, it enables a pull-up resistor. Electrical specifications are listed in section 6.2.6.

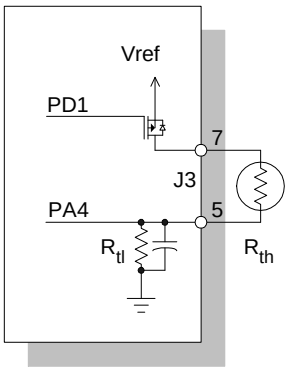
4.3.4 Analog Inputs (A/D)

Each of the Port A I/Os (PA0-PA7) includes an analog-to-digital (A/D) converter. The converters give full-scale readings when the input voltage is equal to voltage reference Vref (e.g. V=Vref•reading/1023). Not all ports are available for external A/D use; see section 4.3.7 for port assignments. Electrical specifications are listed in section 6.2.6.

4.3.5 Temperature Sensing

The Bitsy Plus ADSmartIO can read the temperature of an external thermistor connected across pins 5 and 7 of J3. The ADSmartIO controller drives a transistor to energize the thermistor, then reads the result through the voltage divider created by the thermistor (R_{th}) and an internal resistor (R_{tl}). The thermistor circuit is shown at right.

Electrical specifications for the temperature sensing circuit are listed in section 6.2.6.



4.3.6 Keypad Scan

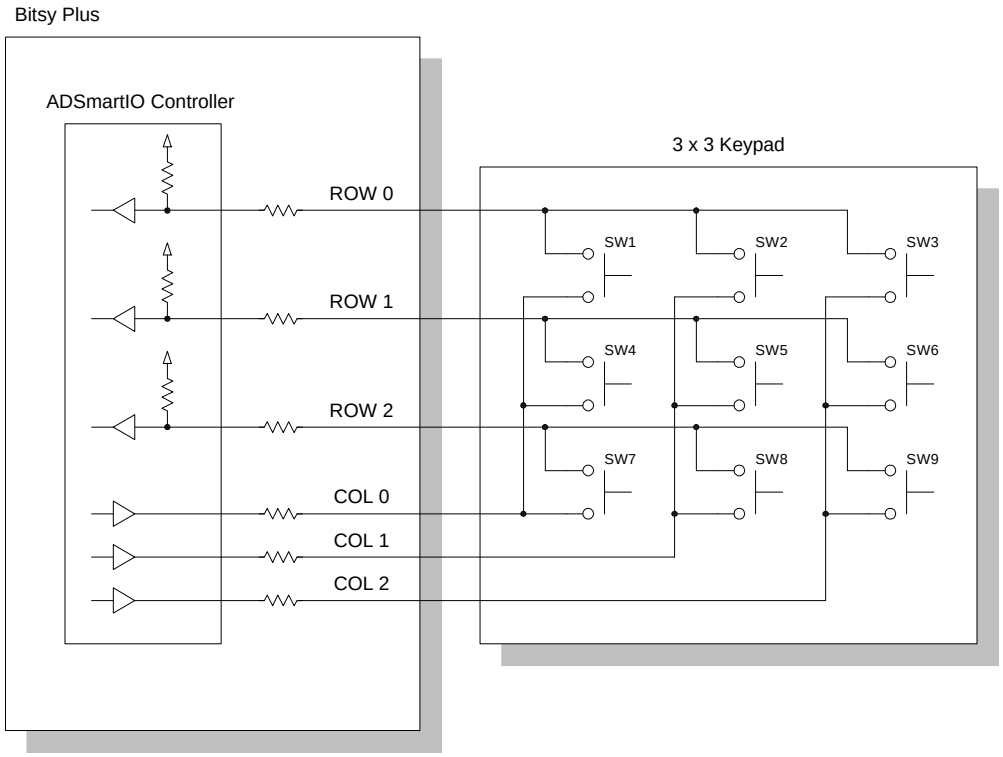
The ADSmartIO can scan a matrix keypad up to four by five keys in size. Matrix keypads are simpler and cost less than full keyboards and can be easily customized for your application. You can also create a keypad matrix from a collection of normally-open switches.

When configured to scan a keypad, the ADSmartIO configures the ROWn lines as inputs with software pull-ups enabled and configures the COLn lines as outputs set to "1"(high). For the scan,

the keypad scanner sets successive COLn outputs to "0"(low), then looks for a "0" on one of the ROWn inputs. The scanner re-reads the pressed key after a delay to debounce the key press.

Unused row and column lines can be used for general purpose I/O or A/D.

The following diagram illustrates how to connect a 3x3 keypad matrix. The pull-ups are the software-activated internal resistors of the ADSmartIO, while the series resistors are part of the Bitsy Plus.



4.3.7 ADSmartIO Signal Cross-Reference

The ADSmartIO microcontroller serves many functions in the Bitsy Plus. The following table illustrates how the microcontroller ports are utilized for ADSmartIO functionality on the Bitsy Plus.

Entries in parentheses indicate indirect connections to the listed pin (e.g. through voltage dividers or additional circuits). Signals with conventional protection circuits are considered directly connected. I=input, O=output.

Port	Pin	Type	Function	
PA0	*J10.27*	*IO*	*Keypad, A/D or digital I/O*	
PA1	*J10.29*	*IO*		
PA2	*J10.31*	*IO*		
PA3	*J10.33*	*IO*		
PA4	*J3.5*	*AI*	*Thermistor reading*	
PA5	-	*I*	*DC_GOOD*[12]	
PA6	-	*O*	*Reset CPU*	
PA7	*(J3.38)*	*AI*	*VBATT_POS divided by 7.2*	
PB0	*J3.22*	*O*	*Battery charger*	
PB1	-	*I*	*System Power enable*	
PB2	-	*O*	*Wake up CPU*	
PB3	-	*O*	*IRQ to CPU*	
PB4	-		*SSP_SFRM*	*SSP communication with CPU*
PB5	-		*SSP RX*	
PB6	-		*SSP TX*	
PB7	-		*SSP CLK*	
PC0	*J10.17*	*IO*	*Keypad, A/D or digital I/O*	
PC1	*J10.19*	*IO*		
PC2	*J10.21*	*IO*		
PC3	*J10.23*	*IO*		
PC4	*J10.25*	*IO*		
PC5	*(J1.3)*	*I*	*Pixel clock*	
PC6	*J10.11*	*IO*	*RTC/I²C or digital I/O* [13]	
PC7	*J10.49*	*IO*	*RTC/I²C or digital I/O*	
PD0	*J10.15*	*IO*	*Passive panel enable (PNL_ENA)*	
PD1	*J10.13*	*IO*	*Thermistor energize (4.3.5)*	
PD2	*J10.9*	*IO*	*PS/2 Clock*	
PD3	*J3.45*	*I*	*wakeup signal from CPLD*	
PD4	*(J1.1)*	*O*	*Vee PWM*	
PD5	*(J3.16)*	*O*	*Backlight PWM*	
PD6	*J10.7*	*IO*	*PS/2 Data*	
PD7	*(J3.18)*	*O*	*Backlight on/off*	

[12] DC_GOOD is an internal digital signal that goes low when the input voltage drops below Vsleep (6.2.1).

[13] PC6 and PC7 are used for the I^2C bus master interface. These communicate with the real-time clock and any off-board I^2C devices, if installed. See section 4.5.4 for details.

4.4 Audio

The Bitsy Plus includes an AC97 codec for stereo audio input and output. Electrical specifications for the audio system are listed in section 6.2.9.

4.4.1 Microphone Pre-amps

The Bitsy Plus supports the connection of a stereo electret microphone to the MIC_R and MIC_L inputs on J10. The audio signals run through pre-amplifiers that low-pass filter and boost the signal before being passed on to the audio codec.

When connecting external electret microphones to the Bitsy Plus, use the MIC_GND analog ground plane for improved signal-to-noise ratio. The Bitsy Plus includes pull-ups to power electret microphones.

4.4.2 Audio Outputs: Speakers and Headphones

The Bitsy Plus audio amplifier supports both differential and single-ended output devices. Differential (or "bridge") drive delivers greater output power and is suitable for speakers, which can be wired independently from each other. Single-ended mode is used for devices like headphones, which have a common ground between output channels.

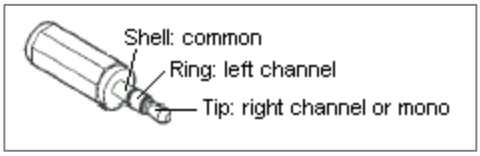
The HP_IN input (J3.32) determines the output mode of the amplifier: When HP_IN is high, the audio output drive is single-ended, when HP_IN is low, the output drive is differential. An on-board pull-up normally keeps HP_IN high.

Connecting Speakers

When using the Bitsy Plus to drive speakers, short the HP_IN signal to ground. This places the output amplifier in differential mode. Connect speakers to the SPKR_L and SPKR_R outputs on J3.

Connecting Headphones

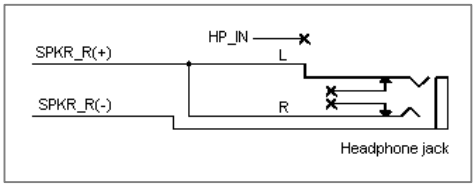
Standard headphones use a plug wired as shown at right. Three rings on the plug provide right and left channels and a common return. Mono headphones do not include the center ring.



The mating headphone jacks include spring contacts to make an electrical connection with the headphone and to mechanically hold the plug in place. Some jacks include a mechanical switch suitable for use with the HP_IN signal that is activated when a plug is inserted into the jack.

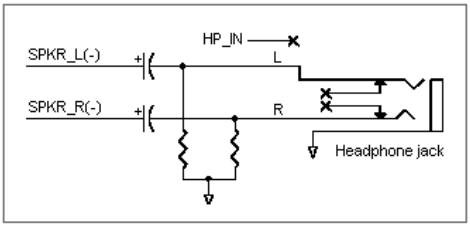
Mono Headphones

You can connect mono headphones directly to the Bitsy Plus as shown at right. Keep in mind that the resulting impedance of the parallel-connected headphone speakers is half that of a single headphone speaker. See the audio driver specifications in section 6.2.9 for details about the minimum impedance an audio output channel can drive.



Stereo Headphones

When wiring for stereo headphones, wire blocking capacitors in series with the Bitsy Plus SPKR-



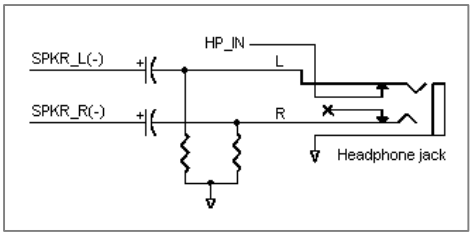
signals as shown at right. These capacitors block the DC component of the audio signal and complete the conversion from differential to single-ended output drive. Leave the HP_IN signal pulled high to enable headphone output.

Select blocking capacitor size based on the lowest frequency your application will need to play out. Larger capacitors give improved bass response (lower frequency cutoff), but are physically larger and cost more. The corner frequency for the low-pass filter created by the capacitor and the headphone speaker is calculated as $fo=1/(2\pi R_L C)$. A 330 uF capacitor into a 32 ohm headphone speaker will give a low cutoff frequency of 15 Hz. Use electrolytic capacitors rated for at least 6.3 V.

The pull-down resistors shown in the diagram drain any charge that builds up on the headphone outputs when headphones are not connected. Use 1 kΩ resistors.

Using Stereo Headphones and Speakers in the Same System

Some applications use both headphones and speakers. You can wire the headphone jack to automatically switch the amplifier to single-ended mode when a headphone plug is inserted in the jack. This will disable the drive to any speakers that are wired into the system.



Most headphone jacks include mechanical switches that indicate when a headphone plug has been inserted. The diagram at right shows a circuit that pulls down the HP_IN signal when a headphone plug is removed.

For this circuit to work reliably in differential mode, the HP_IN signal must remain below V_{HP_IN} through the largest output voltage swings of SPKR_L. Use of 1 kΩ resistors meets this requirement.

4.5 Data Communications

The Bitsy Plus has several built-in channels for communication with peripheral and peer devices. These include RS-232 and logic-level serial, USB host and client ports, SPI bus and I^2C.

4.5.1 Serial Ports

The Bitsy Plus has three StrongARM serial ports configured as follows:

Port	# signals	Connector	Standard	Factory options
Serial 1	9-wire	J10	RS-232 (9-wire)	3.3 V CMOS
Serial 2	3-wire	J3	3.3 V CMOS	(none)
Serial 3	5-wire	J3	RS-232	3.3 V CMOS

The StrongARM serial ports supply two signals: TX and RX ("three-wire" serial, counting GND). The Bitsy Plus uses StrongARM GPIO lines to generate additional signals (RTS and CTS for Serial 3 plus DTR, DSR, DCD and RI for Serial 1). See section 4.1.6 for details.

The StrongARM can configure Serial 2 as an IrDA port . It should be used in conjunction with the IrDAOn signal (J3), which enables the IrDA transmitter. IrDA transceivers can be panel mounted or placed on a personality board.

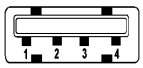
4.5.2 USB

The Bitsy Plus includes signals for USB 1.1 Host and Client ports. The USB Host (downstream) functionality is driven by the SA-1111 companion chip, while the USB Client ("Function" or upstream) port is managed by the SA-1110 processor. The Bitsy Plus can be configured as a self-powered hub, with one Host and one Client port

To create a USB connection, you must wire a standard USB socket as described in the following sections. For each type of connector, pin numbering is as follows:

Pin	USB signal
1	*USB_PWR*
2	*USB -*
3	*USB +*
4	*GND*

USB Host



The Bitsy Plus USB Host port allows you to connect one USB device to the Bitsy Plus. USB mouse and keyboard are the most common client devices, but you can connect any USB function device that has USB drivers installed on the Bitsy Plus.

Use a Type A connector for the host signals on J10 pins 14 and 16 (section 3.3.8). The mating face of such a socket is shown at left. The USB standard also permits directly wiring the USB signals to the target USB device (e.g. USB mouse). To connect more than one USB client device to the Bitsy Plus, use a USB hub.

The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The Bitsy Plus supplies 5 V power through the USB_PWR pin. Make sure to account for power used through USB in your Bitsy power budget (section 5.4.1). It is recommended that you use a power switch.

The Bitsy Plus supports two power control signals on J10. USB_PWR_SENSE is an input that detects over-current conditions. USB_PWR_CTRL an output that controls power to the USB port. See the Bitsy Plus CF Personality Board (ADS p/n 170111-8000) for an example of how to use these signals. Electrical specifications are in section 6.2.8.

USB Client

The Bitsy Plus includes a USB Client (or "Function") port. This interface allows the Bitsy Plus to appear as a client device to USB Host devices such as desktop and laptop computers.

The USB Client signals are available on connector J3, pins 29 and 30. Connect these signals to a USB client Type B socket (mating face shown at left). The USB standard also permits directly wiring the USB signals to the host or to a host connector (e.g. USB mouse).

The Bitsy Plus supports the full USB connection speed (12 Mbit/s), so you must tie a 1.5 kΩ pull-up to the USB+ signal to indicate this capability to host hardware.

USB_PWR is power supplied from the host computer. Since the Bitsy Plus is self-powered (not powered by the USB cable), USB_PWR is not needed as a power input. However, USB_PWR is useful for sensing when a USB cable is connected and for powering the 1.5kΩ pull-up resistor that indicate to the host that the device supports 12Mbps. The Bitsy CF Personality Board reference design (ADS p/n 170111-8000) for an example of such an application.

Revisions 5 and later of the Bitsy Plus add the USB_RECONN signal to J3, pin 33. This signal interrupts power to the 1.5kΩ pull-up, simulating a cable disconnection to the USB host controller. This signal can be used to force the host to re-enumerate the Bitsy Plus (e.g. after wakeup).

4.5.3 SPI Bus

Overview

The SPI Bus (Serial Peripheral Interface) is a full-duplex, synchronous serial protocol developed by Motorola that can support multiple bus masters. The bus consists of a clock line, transmit and receive lines, ground and one or more device selects. Each device on the bus requires its own select line. A key feature of SPI is that data is clocked in both directions at the same time, providing full-duplex data flow.

To clarify direction of the signals, the SPI bus master transmit line (STXD) is also known as MOSI (Master Out, Slave In), while its receive line is known as MISO (Master In, Slave Out). The Slave Select (SS) signal, which enables the slave device's transmitter, is also known as SFRM2 on the Bitsy Plus.

SPI on the Bitsy Plus

The Bitsy Plus has two SPI channels. The StrongARM SA-1110 SPI port is used to communicate with the ADSmartIO controller. The signals for that port are brought out to J4 for ADSmartIO in-system programming, but the port is not otherwise available for external use.

The SA-1111 supplies the second SPI port. The Bitsy Plus uses this port as an SPI bus master to communicate with the touch panel controller. This SPI bus can also communicate with an external device using signals are available on J3.

The Bitsy Plus system controller de-multiplexes the SPI SS line to select either the touch panel controller or the external SPI device. SFRM2 on J3 pin 43 is the external SPI device select. The Bitsy Plus drives the SPI clock and does not support external bus masters.

Electrical specifications for the SPI bus are listed in section 6.2.12. Consult the operating system references for details about how to use the SPI bus for external devices.

Alternate uses of the SPI Port

The SA-1111 SPI port has a great deal of flexibility. If a touch panel is not used, the SA-1111 SPI port can be configured to make use of one or more of the following features:

- Data widths from four to sixteen bits
- 16-entry transmit and receive FIFOs with burst-mode data transfers to/from RAM
- Adjustable FIFO threshold interrupts
- Bit clock speeds up to 1.84 MHz
- Support for Microwire (a National Semiconductor standard) and SSP (Synchronous Serial Port, a TI standard)

Contact ADS Sales of your application will require a driver to make use of these features.

4.5.4 I^2C Bus Master and SMBus

Overview

I^2C (Inter-IC) Bus is a multi-master, "two-wire" synchronous serial bus developed by Philips for communications between integrated circuits (ICs). The bus master addresses devices using the data line and provides a synchronous clock for reading and writing devices. Client devices respond only when queried by the master device. Philips has developed many I^2C devices, but other organizations have adopted I^2C as a convenient means for addressing peripherals in a system.

I^2C on the Bitsy Plus

The ADSmartIO emulates an I^2C bus master using PC6 as SCL and PC7 as SDA. The Bitsy Plus uses the I^2C interface to communicate with the real-time clock (section 4.2). I^2C can also be used to communicate with external devices. PC6 and PC7 are available on J3.

Specifications are listed in section 6.2.6. Consult the ADSmartIO Programmer's Reference for details about how to send and receive I^2C data.

SMBus

SMBus (System Management Bus) is a protocol developed by Intel that is similar to I^2C. Some laptop and desktop computers use SMBus to manage system power using the ACPI standards.[14] A subset of SMBus, the Smart Battery protocol, uses SMBus to communicate with "intelligent" batteries and chargers.[15]

Key differences[16] between I^2C and SMBus include:

- Bus speed:
  The SMBus clock rate must be between 10 kHz and 100 kHz while I^2C can run between DC and 400 kHz.
- Timeout
  SMBus slave devices time out and reset their communication interfaces if there is more than a 35 ms delay in the clock. I^2C doesn't have a timeout.
- Current draw on bus
  SMBus devices must draw between 100 and 350 µA; I^2C devices can draw up to 3 mA.

The Bitsy Plus implementation of I^2C will work with most SMBus devices. The clock rate is compatible, and the ADSmartIO software includes support for the 35 ms timeout. The most likely point of conflict is in the Bitsy Plus I^2C bus current draw (see the pull-up resistor specifications in section 6.2.6). If your configuration will use I^2C as an SMBus controller, contact ADS Sales to discuss the Bitsy Plus configuration you'll require.

4.6 Displays

The Bitsy Plus uses the integrated StrongARM display controller to drive liquid crystal displays (LCDs). Connector J1 supplies the power and data signals needed to drive LCDs, while backlight and touch panel control signals are located on connector J3.

4.6.1 Display Types Supported

ADS has configured the Bitsy Plus for a wide variety of display types and sizes. Consult the ADS support site (section 2.4) for the latest list of displays supported by ADS. If a display isn't on the list, contact ADS Sales for information on ADS' panel configuration service.

The StrongARM controller uses system memory for the display frame buffer, and can drive VGA (640x480) and SVGA (800x600) displays easily. Larger displays will work with the StrongARM, with some constraints imposed by the controller architecture. The ADS Support Forums provide details about the design tradeoffs that are required to support larger displays.[17]

The Bitsy Plus can drive LVDS displays using an ADS adapter circuit.

4.6.2 Panel Voltages

The Bitsy Plus supplies 3.3 V or 5 V power to the LCD display via J1. Select this voltage with JP3 (section 3.2.1). Please observe the cautions listed with the JP3 settings.

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[14] http://www.acpi.info/index.html

[15] http://www.sbs-forum.org/

[16] http://dbserv.maxim-ic.com/appnotes.cfm?appnote_number=356

[17] Currently posted at http://www.applieddata.net/forums/topic.asp?TOPIC_ID=580

4.6.3 Display Signals

StrongARM display signals *LDD0* through *LDD15*--as well as the pixel clock, vertical sync and horizontal sync--are all buffered at a factory-set voltage. See section 6.2.2 for full specifications.

The *PNL_RL* and *PNL_UD* signals are for active (TFT) displays that support changing the scan direction. This feature allows the display to be flipped right-to-left (*RL*) or up-and-down (*UD*) by changing the voltage on these signals. See section 6.2.2 for full specifications.

4.6.4 Creating Display Cables

ADS has designed cables for a wide variety of displays. See the list of supported displays on the ADS support forums. Cable drawings for supported displays are available on request.

While ADS does not provide support to customers to create their own cables, designers with LCD display experience may be able to design their own. For those that do so, a key point to keep in mind is that the SA-1110 LCD interface maps its display controller pins differently based on LCD technology and color palette size. The following table illustrates how they are mapped for some of the more common technologies. Consult the SA-1110 User's Manual for more information.

StrongARM Signal Name	***Color Active***		***Color Passive***			***Mono Passive***			
	16-bit	***12-bit***	***Dual***		***Single***	***Dual***		***Single DPD[18]***	***Single***
LDD0	*B0*	*B0*	*DU0*	*top*	*D0*	*DU0*	*top*	*D0*	*D0*
LDD1	*B1*	*B1*	*DU1*		*D1*	*DU1*		*D1*	*D1*
LDD2	*B2*	*B2*	*DU2*		*D2*	*DU2*		*D2*	*D2*
LDD3	*B3*	*B3*	*DU3*		*D3*	*DU3*		*D3*	*D3*
LDD4	*B4*	*G0*	*DU4*		*D4*	*DL0*	*bottom*	*D4*	*not used*
LDD5	*G0*	*G1*	*DU5*		*D5*	*DL1*		*D5*	
LDD6	*G1*	*G2*	*DU6*		*D6*	*DL2*		*D6*	
LDD7	*G2*	*G3*	*DU7*		*D7*	*DL3*		*D7*	
LDD8	*G3*	*R0*	*DL0*	*bottom*	*not used*				
LDD9	*G4*	*R1*	*DL1*						
LDD10	*G5*	*R2*	*DL2*						
LDD11	*R0*	*R3*	*DL3*						
LDD12	*R1*	*not used*	*DL4*						
LDD13	*R2*		*DL5*						
LDD14	*R3*		*DL6*						
LDD15	*R4*		*DL7*						

4.6.5 Developing Display Drivers

The StrongARM has a bank of registers (LCCR0 through LCCR3) that define the timing for displays. In addition, the operating system must define the region of memory for the frame buffer(s).

ADS provides display timings for supported displays on request. For displays not yet supported, ADS has a panel configuration service to creates panel timings and cable drawings. Contact ADS Sales for further details.

[18] Double pixel data (DPD) mode = 1

4.6.6 Brightness Control (Backlight)

Most LCD displays include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Some LCDs, such as passive transflective displays, can be viewed in daylight without backlighting.

Panel backlights are driven by backlight inverters. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. Fortunately, most backlight inverters include control signals to dim and turn off the backlight.

The Bitsy Plus supplies two signals for backlight control: BacklightPWM (J3.16) and /BacklightOn (J3.18). BacklightPWM is a filtered PWM signal that supplies an analog output voltage to control the intensity of the backlight. The /BacklightOn signal is an open-collector output to turn the backlight on and off. The ADSmartIO controller drives these signals. See section 6.2.2 for electrical specifications.

4.6.7 Contrast Control (Vee and Vcon)

Vee and Vcon are used to control the contrast of passive panels. Many passive panels require a positive or negative bias voltage in the range of fifteen to thirty volts to bias the passive LCD display.

Some displays include a Vee generator and simply require a low-voltage analog signal to control the contrast. The Vcon output is a PWM-controlled output that can be used for this purpose. Electrical specifications for Vee and Vcon are listed in section 6.2.2.

4.6.8 Touch Panel

The Bitsy Plus supports four and five-wire analog resistive touch panels (five-wire control is a factory option). Connect the touch panel to the inputs on connector J3. The touch panel controller can wake the system from sleep (section 5.3.3) Electrical details are listed in section 6.2.3.

4.7 EMI/RFI and ESD Protection

The Bitsy Plus board incorporates a number of industry-leading features that protect it from electrostatic discharge (ESD) and suppress electromagnetic and radio-frequency interference (EMI/RFI). Transient voltage suppressors, EMI fences, filters on I/O lines and termination of high-frequency signals are included standard on all systems. For details, see electrical specifications for subsystems of interest.

4.7.1 Agency Certifications

Many products using ADS single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. Because ADS supplies only the single-board computer and not fully integrated systems, ADS cannot provide meaningful system-level emissions test results.

See the crystal frequencies (section 6.2.11) and electrical specifications for information that may be helpful during agency certifications.

4.7.2 Protecting the Power Supply Inputs

It is the responsibility of the designer or integrator to provide surge protection on the input power lines. This is especially important if the power supply wires will be subject to EMI/RFI or ESD.

5 Power and Power Management

Power management is especially critical in portable and handheld applications where battery power is at a premium. The Bitsy Plus includes advanced power management features, including the low power StrongARM CPU, partitioned power distribution and ability to run from several types of DC power inputs. The Bitsy Plus can also operate as a conventional single-board computer, taking advantage of the inherently low power consumption of the system.

This chapter describes the architecture of the Bitsy Plus power supply, factors affecting power consumption and reference designs to get you started. For information about how much power the Bitsy Plus consumes, consult the electrical specifications in section 6.2.5.

5.1 Determining the Features You Need

Not all designs with the Bitsy Plus need to be optimized for lowest power consumption. Consider the following types of typical system configurations to determine the topics of interest to your application.

Relevant Topics / Features Required	"Line" power (5.3.1)	Control ext power supply (5.3.2)	Sleep/ wakeup button (5.3.3)	Backlight power control (5.3.6)	System battery (5.3.1)	Battery charging (5.3.7 and 5.5.3)	Supercapacitors (5.3.5)	RTC battery (4.2 and 5.5.1)
System is On All the Time	✓							
System Power Supply Turned Off to Shut Down System		✓					✓	
System Should "Turn Off" when not in use	✓	✓	✓	✓				
Battery-Operated, Minimum Power Consumption					✓	✓		
"Pulled-Plug"/Brownout Protection			✓		✓	✓	✓	
Must Preserve Time and Date Under All Circumstances			✓		✓			✓

5.2 Power Management Modes

Handheld and portable systems available today never really turn "off." They make use of power management algorithms that cycle the electronics into "standby" and "sleep" modes, but never fully remove power from the full system.

This section describes the various power management modes of the StrongARM processor and how the Bitsy Plus makes use of them.

5.2.1 StrongARM Power Management Modes

The StrongARM SA-1110 processor supports three operational modes: RUN, IDLE, and SLEEP. RUN mode offers the greatest performance at the highest cost in power consumption. IDLE mode defines operation with reduced power consumption from RUN mode while offering a shorter transition time to RUN than from SLEEP. In IDLE mode, the StrongARM continues to run, while unused peripherals are disabled. SLEEP mode offers the greatest reduction of operating current. The processor core is powered off and only a few peripherals (RTC, I/Os and interrupt control) remain active.

5.2.2 Power Management on the Bitsy Plus

The Bitsy Plus can actively be configured to be in StrongARM RUN or SLEEP modes. IDLE mode is controlled by the operating system and is typically transparent to the application.

In RUN and IDLE modes, the power supplies are in their standard, full-power state and applications run normally on the system. Specific subsystems (as described in section 5.3.2) may be selectively disabled to conserve power during these states.

In SLEEP mode, sometimes called "Suspend" mode, the processor puts the SDRAM in a low-power, self-refresh mode, the processor core shuts off, most peripheral sub-systems are shut down and the power supplies drop into low-power states or turn off entirely (see the diagram in section 5.3.2 for details). In this state, the Bitsy consumes very little power, most of which is dedicated to the maintenance of the RAM (see section 6.2.5 for specifications). The system can be "awakened" and returned to the RUN state by initiating a system wakeup using one of the methods described in section 5.3.3.

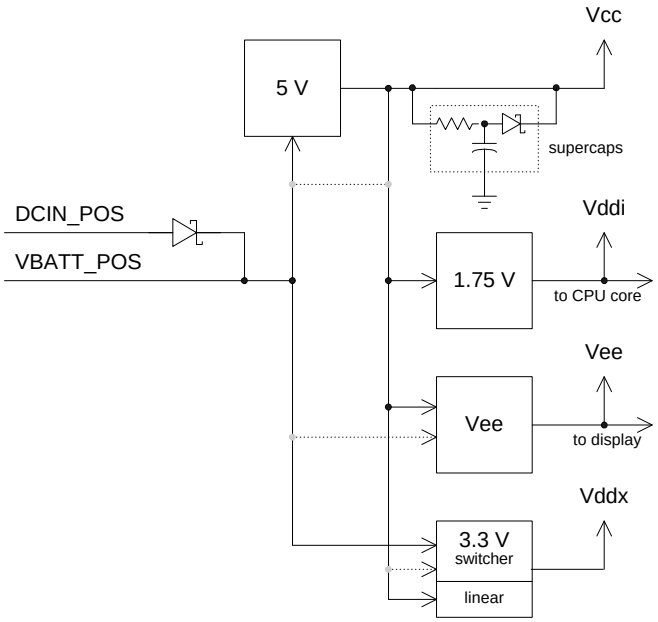
If Main Power (DC_IN or VBATT_POS) drops below the power supply trip point (section 6.2.2), the Bitsy Plus generates and interrupt that the operating system can use to put the system into Sleep mode. The transition time from RUN mode to SLEEP mode is a function of the operating system. System SLEEP can also be initiated programmatically.

5.3 Architectural Overview and Power Management Features

This section provides an overview of the architecture of the Bitsy Plus power supply and a description of the various features of the Bitsy Plus power management systems.

5.3.1 Power Supply Architecture

The Bitsy Plus power supply is laid out as shown in the following diagram. Incoming DC power is regulated to 5 and 3.3 V. Other system voltages are derived from these power supplies.



DC_IN and VBATT voltages are mixed using a diode with a low forward voltage. This allows a battery and DC power supply to be connected at the same time. If only one power supply is used for your system, use the VBATT_POS input. See sections 5.3.7 and 5.5.3 for examples.

Several factory options are available and are indicated by dashed lines in the diagram above. The supercapacitors (section) are a standard factory option. The other options are available for production customers, but are outside the scope of this manual. Contact your ADS sales representative if you believe one or more of these options is required for your application.

Specifications for the Bitsy Plus power supply are listed in section 6.2.4.

5.3.2 Subsystem Partitioning

The Bitsy Plus can selectively turn off power to subsystems on the board. This load-shedding feature can extend battery life and significantly increase the amount of time the supercapacitors will hold up system power. Applications and the operating system determines how selective power management is utilized.

Bitsy Plus systems that can be selectively disabled include the following:

- LCD display (panel power and signal buffers)
- Vee (contrast control)
- Audio output amplifier
- Audio codec and microphone pre-amps
- Serial 1 and 3 RS-232 buffers

- External device 1 (/PE1, J3.42)
- External device 2 (PE2, J3.24)

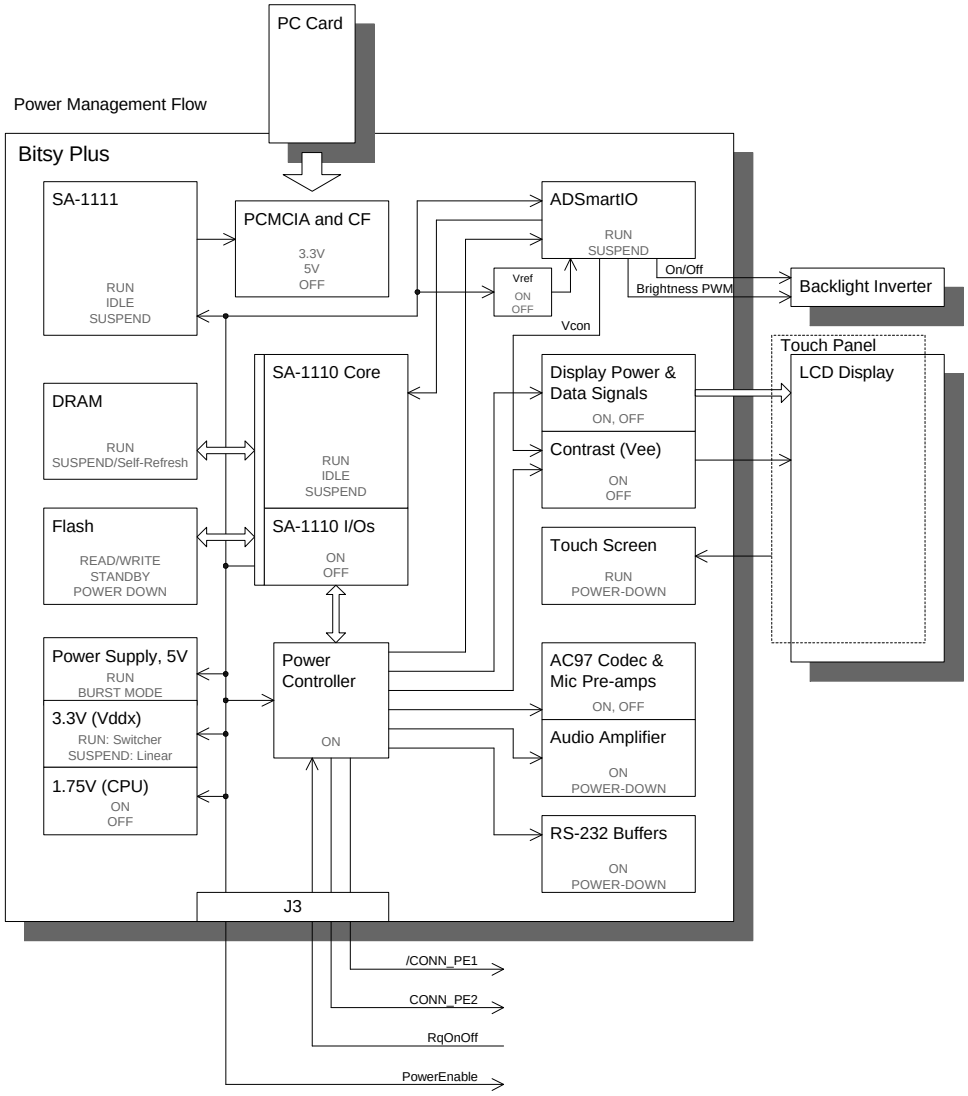
In addition, the Bitsy Plus also controls its core power supplies to support sleep operation:

- Vcc (5 V) supply
- Vddx (3.3 V) Vddi (processor core) supplies

The following diagram illustrates the architecture of the Bitsy Plus power management system. At the heart of the system is a power controller that controls the state of the various power subsystems of the Bitsy Plus. Under control of the StrongARM processor, this controller can manage most of the power distribution of the board. The StrongARM PowerEnable signal controls the rest of the subsystems.[19]

[19] The controller inverts the PowerEnable signal for use with some subsystems. This details is not shown in the diagram.

In the diagram, the power management modes of each of the subsystems is indicated in gray. Arrows indicate the direction of both signal flow and of power management.



5.3.3 System Sleep

This section describes several methods for putting the system into Sleep mode.

Power Failure Interrupt

When the input voltage falls below Vsleep (section 6.2.2), the system generates a in internal power failure interrupt (the DC_GOOD signal goes low). This interrupt gives the operating system early warning of an impending power failure, allowing the system to drop into low-power Sleep mode before power has failed completely.

Systems that have supercapacitors benefit from this feature by going to sleep before they begin drawing down energy stored in the capacitors. This prolongs the amount of time the system can maintain the contents of RAM.

Operating systems may allow the option to ignore power-failure interrupts. This allows systems to run with lower input voltages without going to sleep. However, note that if the system does go to sleep, it will not be able to wake until the input voltage is above Vsleep (see section 5.3.4 for details)

RQOnOff Input

Operating systems and applications can configure the /RQONOFF signal (J3.45) to put the system to sleep. In conjunction with the wakeup function (section 5.3.4, below), the /RQONOFF input can be used as an "on/off" button for some systems. Electrical specifications are listed in section 6.2.7.

Software Control

Applications can put the system to sleep programmatically. Operating systems may also put the system to sleep if the system has not been used for a certain amount of time or for other reasons. In remote, battery-powered applications, software Sleep can be used in conjunction with the Timed Wakeup feature (section 5.3.4) for minimum power consumption.

5.3.4 System Wakeup

This section describes several mechanisms for waking a Bitsy Plus system from Sleep mode. The system will resume operation in Run mode unless the power supply voltage is lower than Vsleep (section 6.2.2). If the input voltage is too low, the system will not wake under any circumstances. This protects the RAM from getting corrupted by an under-voltage condition.

RQOnOff Input

Shorting the /RQONOFF signal (J3.45) to ground will wake the system. The signal is connected to the system controller. Electrical specifications are listed in section 6.2.7.

Touch Panel

The touch panel controller interrupts the processor when touch panel events occur. Before going to sleep, the processor can place the controller in a low-power sleep mode from which the controller generates a wakeup interrupt when a touch event occurs.

Timed Wakeup

The StrongARM can wake up at a predetermined time. This feature is controlled by software.

ADSmartIO

The ADSmartIO controller controls the wakeup signal to the StrongARM. For production applications, ADS can configure the ADSmartIO to wake up the system on specific events. Contact ADS Sales if your application requires a special wakeup event.

5.3.5 Supercapacitors (factory option)

Supercapacitors (sometimes known as "ultracapacitors") are energy storage devices that combine the quick charge/discharge characteristics of capacitors with the higher energy density of batteries. "Supercaps," as they are called, are useful for maintaining power when changing batteries or for riding out power failures.

Supercaps are a factory option for the Bitsy Plus and must be requested when you place your order. Supercaps are the two large cylinders mounted between the PCMCIA header and 50-pin headers J9 and J10.

Charging

There are two important factors related to the charging phase of the capacitors. The first is how long it takes to fully charge the capacitors. The second is the added load on the power supply it takes to charge the capacitors. Both are important to effectively use the supercaps.

Charge time for capacitive circuits is typically measured in "time constants," the product of the charging resistance, R and the capacitance, C. It takes three time constants (3RC) to charge fully-discharged supercaps to 95% of their target voltage. For example, a system with 44 ohm charging impedance and 1.65 F supercaps has a time constant of 73 seconds. Allow at least five minutes to recharge the capacitors after the board has been disconnected from power. Charge time is shorter if the supercaps aren't completely discharged.

The charging current for the supercaps starts out high and diminishes exponentially as the capacitors reach full charge. Make sure to account for this current in your power budget (section 5.4.1). The charge current is calculated as

$$i(t) = \frac{V_t - V_i}{R} e^{-t/RC}$$

where

- V_t is the charging/final voltage of the capacitor (assume 5.0 V unless the capacitor is not charged completely),
- V_i is the initial charge voltage of the capacitor, and
- t is the time in seconds

Use the maximum current (time=0, V_i=0, $i(0)=i_{max}=V_t/R$) in your power budget.

Discharging

When power fails on a system equipped with supercaps, the operating system shuts off all power to the board and puts the system to sleep. When power is restored, the system remains asleep until either the system is awakened (J3.45) or is reset (J10.45).

The amount of time that a system can remain asleep using only supercap power depends primarily on how quickly external power drops off and how quickly the operating system can put the board to sleep.

If the operating system can shut down the system before the power supply drops below the supercap charge level, you will get significantly longer sleep time from your supercaps. You can calculate how much time the system will have to go to sleep based on (1) how quickly your power supply will fall when main power fails and (2) the trip point of the Bitsy Plus power fail circuit (section 6.2.1). When possible, put the system to sleep with software if a power failure condition is expected (e.g. changing a battery).

The supercaps discharge linearly from the constant-current drain during sleep according to the equation

$$t = \frac{(V_i - V_f - 0.2) * C * Eff}{I_{sleep}}$$

where

t	is the duration the system can sleep, in seconds;
V_i	is the initial charge voltage of the capacitor;
V_f	is the supercap voltage at which onboard systems will fail (assume 3.2 V);
C	is the capacitance of the supercaps, in Farads;
Eff	is the efficiency of power delivery; 85-90% is a safe value to use;
I_{sleep}	is the amount of current the system consumes while in sleep mode.

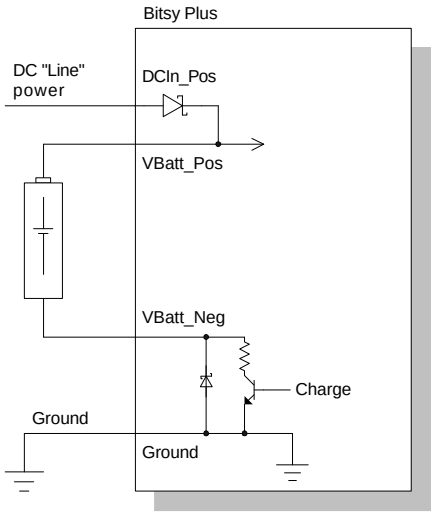
For example, a system with fully charged 1.65 F supercaps and a sleep current of 4 mA can expect to run for up to ten minutes after a power failure. Consult the electrical specifications of section 6.2.4 and power consumption specifications of 6.2.5 for the values to use in your calculations.

5.3.6 Backlight Power

The Bitsy Plus provides software control of Backlight Intensity and On/Off using the ADSmartIO controller. Power for the backlight is not routed through the board, and must be supplied to the backlight separately from the Bitsy Plus. This provides the greater flexibility when selecting backlight inverters for an application. See section 4.6.6 for further details about backlight control.

5.3.7 Battery Trickle Charger (factory option)

The Bitsy Plus includes a trickle charger for basic charging of external batteries. The following diagram illustrates the charging circuit and a standard means of combining it with DC line power.



The Charge signal comes from the ADSmartIO controller (port PB0) and is also available on J3 pin 22 for external use. Writing a logic "1" to PB0 turns on the trickle charging. It is up to the application to manage battery charging.

The diode on the negative terminal of the battery allows the battery to power the Bitsy Plus at any time, but prevents the battery from being charged by a DC voltage on the DCIN_Pos input. The charge current is calculated as follows:

$$I_{charge} = \frac{DCIN\_Pos - (2 * 0.2) - V_{batt}}{R}$$

where

Vbatt is the battery voltage (Vbatt_pos-Vbatt_neg), and

R is the charge resistor (section 6.2.4).

While standard systems include the charging circuit, the charge resistors must be selected for effective charging of specific batteries to be used. Select a resistor value that will provide the desired charge current but not exceed the power rating of the resistor. Since $P=I^2R$,

$$I_{charge,\ max} = \sqrt{P_{ch} / R}$$

where P_{ch} is the maximum power the charge resistor can support. Consult the electrical specifications in section 6.2.2 for the values populated on standard systems.

5.3.8 Power Supply Efficiency

The Bitsy Plus power supply achieves high efficiency through several means. First, it utilizes high-efficiency switching regulators. These regulators use conventional step-down switchers under operating load conditions, but are configured by the system for linear and "burst" mode[20] operation during low-load conditions that occur during system sleep. Additionally, there is only one level of cascaded regulation, reducing the losses that multiply through each stage.

5.4 Designing for Optimal Power Management

Designing a system for optimal power management requires careful attention to many details. This section provides some guidelines and tips for best power management.

5.4.1 Create a Power Budget for Peripherals

Embedded system designers using the Bitsy Plus should have a clear understanding of how power usage will be allocated in the system they design. Designers should create a power budget that takes into account the types of devices that are expected to be used with the Bitsy Plus.

The following lists detail some of the typical external loads that can be placed the Bitsy Plus power supplies. Baseline power consumption of the Bitsy Plus is listed in section 6.2.5.

3.3 V Loads

Typical external loads on the 3.3 V power supply include the following:

- Display
- Personality Board
- CF and some PCMCIA cards

[20] "Burst mode" in this context is a registered trademark of Linear Technology Corporation

5 V Loads

5 V loads come from both onboard and external devices:

External:

- Display
- Backlight
  O*nly if powered by 5 V Bitsy Plus power supply*
- Most PCMCIA cards
- USB devices
- PS/2 keyboard
- Speaker(s)
  Assume 80% efficiency

Onboard:

- 3.3 V Supply
  Multiply by 115% to account for 3.3 V power supply efficiency
- Supercaps
  Use peak inrush current in your budget

Loads on Main Supply

The main power supply (DCIN_Pos or VBatt_Pos) is loaded by the 5 V and 3.3 V supplies as indicated in the diagram of section 5.3.1. Assume 85% efficiency for external loads that cascade through the 5 V supply. Consider these loads when creating your power budget.

5.4.2 Power Loads During Sleep

When designing systems for minimal power consumption during Sleep mode, make sure to consider DC losses to external connections. The following are a few of the ways your system may "leak" when asleep:

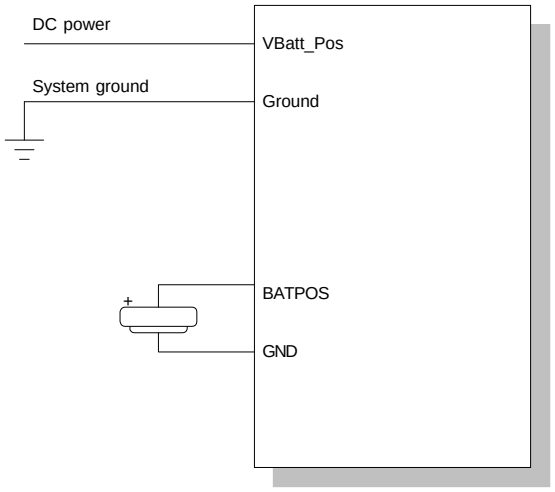
- PCMCIA and CF cards
  Cards in place when the system is asleep can drain power through the Card Detect and Voltage Sense lines. Assume that all four lines ground the Bitsy Plus PCMCIA pull-ups (section 6.2.12) while the card is inserted.
- Digital I/Os
  Review digital I/O connections for potential voltage differences from external connections when the Bitsy Plus is asleep.
- USB
  Depending on how USB devices are powered and how the operating system handles USB, USB devices may draw power during Sleep.

5.5 Power Supply Examples

The following are basic examples of how to configure power supplies for the Bitsy Plus.

5.5.1 Basic DC Supply

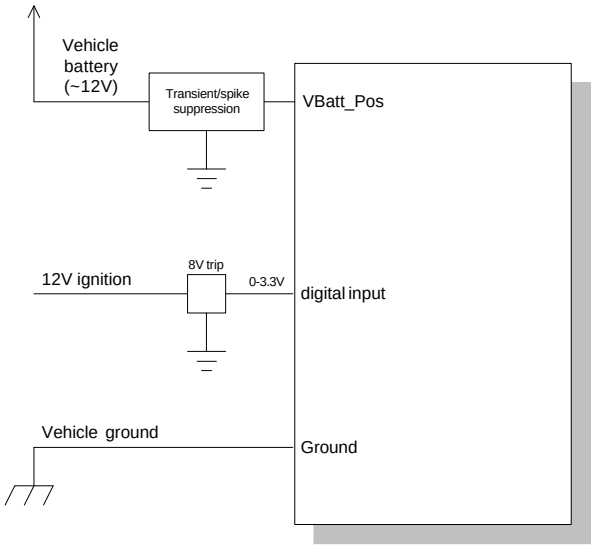
The simplest way to power the Bitsy is to supply DC power to the VBatt_Pos input, as shown below.



This diagram also illustrates how to connect a coin cell to the RTC circuit for systems that require the RTC to be maintained under all power conditions.

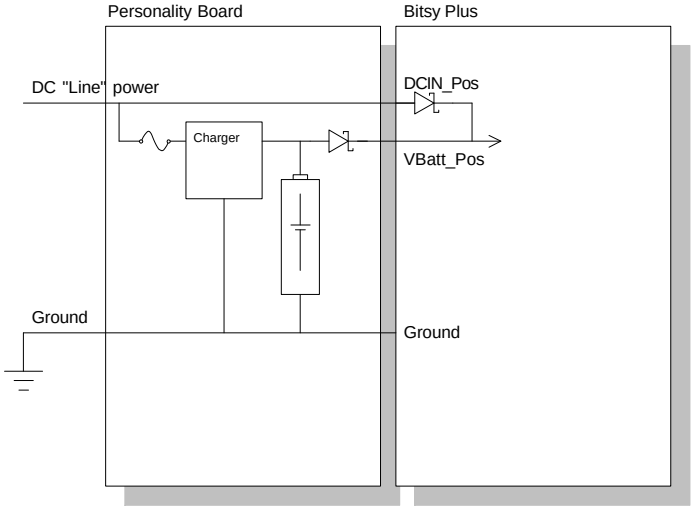
5.5.2 Automotive System

This system connects the Bitsy Plus directly to the vehicle battery, but polls a sense line on the ignition to put the system to sleep when the vehicle is turned off.



5.5.3 Line Power and Battery with External Charger

You may choose to use an off-board battery charger for a specific battery chemistry or voltage. The following diagram illustrates one way to include a charger on your own personality board.



In this example, DC "Line" power may come from a DC power supply, battery or other DC power source.

The Bitsy Plus Personality Board (ADS p/n 170111-8000) includes an external battery charger using a design similar to the one depicted above.

For an illustration of how to use the onboard Bitsy Plus trickle charger in conjunction with line power, see the diagram in section 5.3.7.

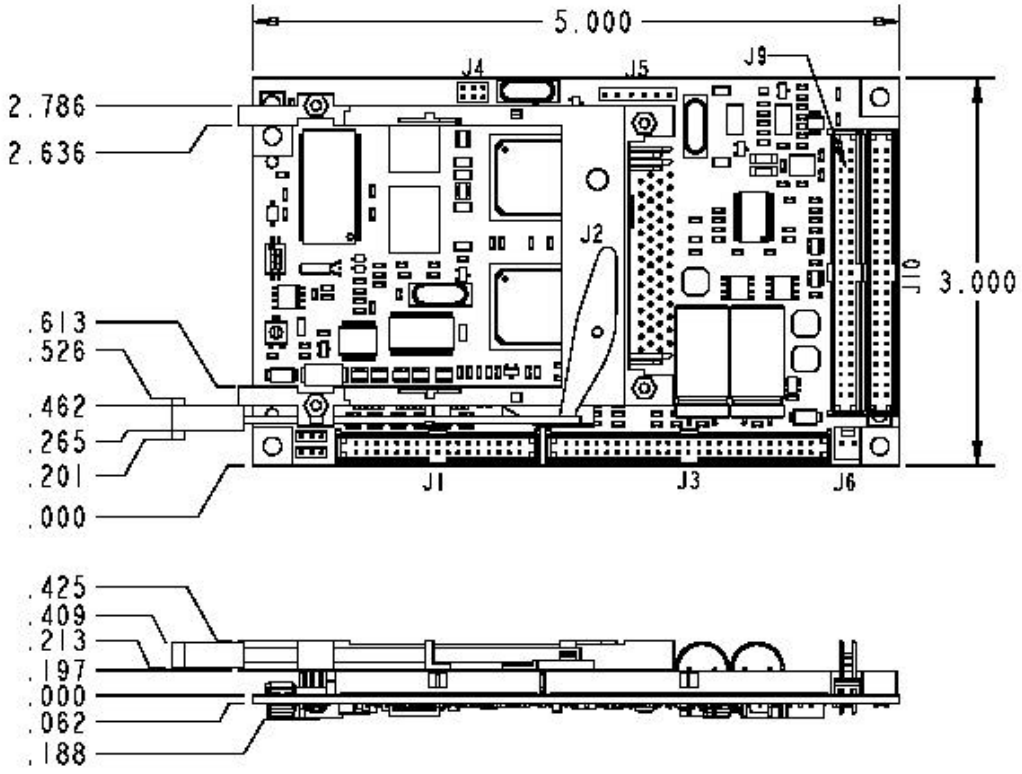
6 System Specifications

6.1 Mechanical Specifications

The Bitsy Plus is 3.0 inches by 5.0 inches in size. This section describes the component dimensions and mounting of the board. Detailed drawings are available on the support forums (section 2.4), and 3D models are available from ADS in electronic format for production customers.

6.1.1 Mechanical Drawing

The following mechanical drawing of the Bitsy Plus specifies the dimensions of the Bitsy Plus, as well as locations of key components on the board. The PCMCIA ejector is integrated into the design and is not removable. All dimensions are in inches. This image is an excerpt from the full mechanical drawings, ADS document number 630114-1000A.



6.1.2 Mounting Holes

Four holes are provided, one on each corner, for mounting. The diameter of the holes is 0.138-in. Mounting holes are plated through and connected to the Bitsy Plus ground plane.

For reliable ground connections, use locking washers (star or split) when securing a Bitsy Plus in an enclosure. Make sure that washers do not extend beyond the limits of the pads provided.

6.1.3 Clearances

The Bitsy Plus has a low profile. It can fit in an enclosure as thin as 0.772 inch (19.6 mm) I.D. Key clearances are as follows:

- Highest component: 0.425 inch (10.8 mm), top
  0.126 inch (3.20 mm), bottom
- Board Thickness: 0.062 inch (1.57 mm)
- Clearance over top/Bottom: 0.05 inch (1.3 mm)

Note: Selection of connectors and wiring harnesses will determine height of final assembly.

6.2 Electrical Specifications

6.2.1 Temperature, Reset, Sleep, Wakeup

Absolute Maximum Ratings

Reset Input (RESET_IN) .....3.6 V (note 1)

Wakeup Input (/RqOnOff) .....5.5 V (note2)

Symbol	Parameter	Min	Typ.	Max	Units
Temperature					
Trun	operating temperature	-40		+85	°C
Reset_In (J10.45)					
Vrst	trigger voltage (Note 3)		2.7		V
Vprst	pull-up voltage		Vddx		V
Rprst	pull-up resistance		47		kΩ
Sleep (5.3.3)					
Vsleep	Sleep trigger voltage (Note 4)	5.4		5.8	V
Vsleep,hyst	Sleep trigger release hysteresis (Note 5)	0.06		0.25	V
Wakeup: RqOnOff (J3.45)					
trq	wakeup pulse duration (Note 6)	100			ms
Vprq	pull-up voltage		Vddx		V
Rprq	pull-up resistance		11		kΩ

Notes:

1. The reset controller can support operating voltages up to 10 VDC. However, such high voltages on Vddx through the pull-up resistor may damage the system.
2. The /RqOnOff signal is connected to the system controller, which determines this rating (see section 6.2.7).
3. Short \Reset_In to GND to reset system
4. This is the voltage at VBATT_POS at which the DC_GOOD signal (4.3.7) changes from high to low, which can trigger the system to go into Sleep mode. Sleep trigger at DCIN_POS is Vsleep+Vdin (6.2.4).
5. **Important!** Once Vsleep has been triggered, the input voltage must rise at least Vsleep,hyst above Vsleep before the voltage detector will restore the DC_GOOD signal. Make sure that your input voltage is designed to always run above Vsleep+Vsleep,hyst, or systems that go to sleep may not be able to wake again.
6. Short /RqOnOff to GND to for at least trq to wake up system. A low-level voltage on /RqOnOff initiates wakeup.

6.2.2 Display

LCD display panels have a wide range of voltage and data requirements. The Bitsy Plus has a number of adjustable voltages to support these requirements, as well as controls for brightness (backlight) and contrast (passive panels only). See section 4.6 for further details.

Symbol	Parameter	Min	Typ.	Max	Units
LCD (4.6.2)					
V pnl	Display power supply (note 7)	3.3		5.0	V
P pnl_pwr	Display power (note 8)			2	W
V pnl_data	Panel data voltage (note 9)	3.3	3.3	5.0	V
Scan direction (active displays) (4.6.3)					
R pnl_rl	Pull-up/down resistance		4.7		kΩ
R pnl_ud	Pull-up/down resistance		4.7		kΩ
V pnl_rl	(note 10)	0	V pnl	V pnl	V
V pnl_ud	(note 11)	0	V pnl	V pnl	V
Contrast Control (passive displays) (3.2.2, 4.6.7)					
Vee(-)	Contrast adjust, R_L=5kΩ, JP4: 1-2	-30		-15	V
Vee(+)	Contrast adjust, R_L=5kΩ, JP4: 2-3	15		30	V
Vcon	Low-voltage contrast adjust (note 13)	0		Vddx	V
Brightness Control (backlight, 4.6.6)					
R backlightOn	Pull-up (factory option, note 12)		10		kΩ
V backlightOn	Pull-up installed (note 12)		5		V
	No pull-up			30	V
V backlightPWM	PWM (note 14)	0		3.3	V
R backlightPWM	PWM series resistance (note 14)		1.2		kΩ

Notes:

7. JP3 selects the display voltage.
8. Total power available depends on system power budget.
9. Systems are configured at the factory with buffers for 3.3 or 5 V panel data. R289 selects 5 V power for the buffers while R288 selects 3.3 V power (they're located under the opening for the PCMCIA header about 1cm from the right, ejector corner of the board). 5 V displays with Vih <= 0.6•Vpnl_pwr (3.0 V) will work reliably with 3.3 V data.
10. PNL_RL is pulled up with R87 or pulled down with R22.
11. PNL_UD is pulled up with R79 or pulled down with R17.
12. A pull-up resistor (R116) can be installed on the BacklightOn signal as a factory option. If the pull-up is not installed, maximum voltage is limited by the transistor ratings.
13. Vcon is the low-voltage PWM signal used to control Vee. It can be used directly with some passive displays to control contrast.
14. The backlight on/off and PWM outputs are driven by the ADSmartIO controller

6.2.3 Touch Panel Controller

The Bitsy Plus uses touch panel controllers from Burr Brown. It uses the ADS7846 to support four-wire analog-resistive touch panels and the ADS7845 to support five-wire panels. The system is factory-configured for use with four-wire panels. All touch-panel signals are ESD and RF protected. The touch panel controller is powered during sleep mode and can generate an interrupt to wake the system.

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	Supply voltage		Vddx		V
---	A/D sample resolution		12		bit

6.2.4 Power Supply

Absolute Maximum Ratings

Supply Voltage (DCIN_POS)..... 18 V

Symbol	Parameter		Min	Typ.	Max	Units
System Power						
VBATT_POS	Bitsy Plus supply voltage (note 15)		5	12	15	V
Vdin	Diode drop from DCIN_POS to VBATT_POS at 130 mA			0.35	0.4	V
VDDI	Processor core voltage (6.2.10)		1.65	1.75	1.85	V
VDDX	3.3 V onboard supply	Run	3.1	3.3	3.5	V
		Sleep		3.15		V
VCC	5.0 V onboard supply		4.75	5.0	5.25	V
I (Vcc)	5 V available for display, PCMCIA, USB, J9.15, J10.48, etc. (Note 15)	Run			500	mA
		Sleep				
I (Vddx)	3.3 V available for display, PCMCIA, J9.23, J10.47, etc. (note 17)	Run			700	mA
		Sleep			100	mA
Supercapacitor Option (section 5.3.3)						
C	Capacitance			1.65		F
Vcap	Charge voltage			Vcc		V
Rcap	Series charge resistance			44		Ω
tc	Charging time from full discharge		5			min
RTC Backup Power (4.2)						
V BATPOS	real-time clock battery backup		2.2	3.0	3.6	V
I BATPOS	RTC current (note 18)			300	500	nA
Battery Trickle Charger (section 5.3.7)						
Rch	Charger series resistance			37.5		Ω
Pch	Charge resistor power rating				0.25	W

Notes:

15. The system can operate down to the minimum voltage shown, but the DC_GOOD signal may cause the system to go to sleep when running at that voltage. See *Power Failure Interrupt* in section 5.3.3 for details. The power failure feature can be overridden, but DC_GOOD must be valid for the system to wake up from Sleep mode.
16. LTC 1771 "Burst" mode, used when the Bitsy Plus is in Sleep mode, is more efficient at low currents. However, it is electrically noisier and can cause significantly greater EMI/RFI at higher current draws.
17. During Sleep mode, Vddx is powered by a linear regulator, which draws from the 5V supply.
18. Vddx=0V, Vbatpos=3.2 V (source: DS1307 data sheet)

6.2.5 Power Consumption

The following table lists typical power consumption for the Bitsy Plus with varying input voltage and activity levels. Run mode efficiency of the power supply decreases slightly with higher input voltage.

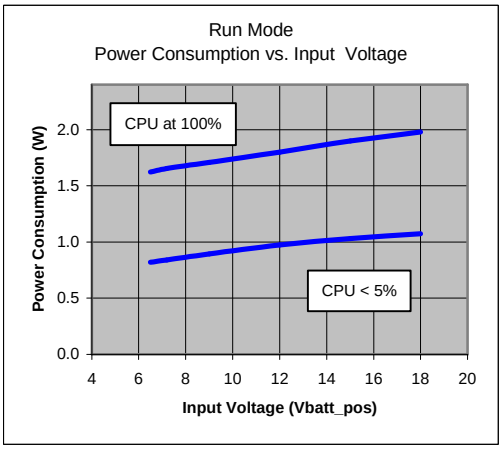
Power consumption varies based on peripheral connections, components populated on the system and the LCD panel connected. Input voltage, temperature and the level of processor activity affect power consumption to a lesser extent.

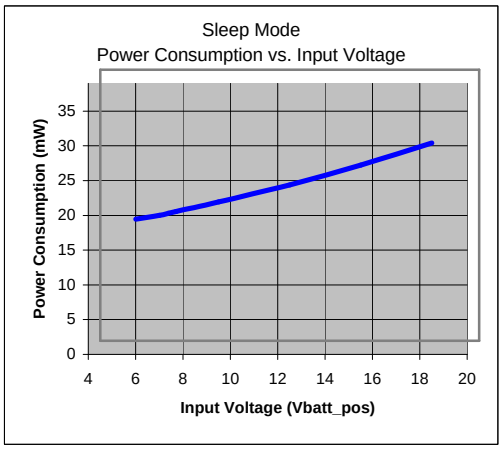
LCD displays and backlights add significantly to the total power consumption of a system. ADS Development systems include the Sharp LQ64D343 5V TFT VGA display, which draws about one watt, and the Taiyo-Yuden LS520 backlight inverter, which draws about six watts at full intensity.

Test Condition	Input Voltage (Vbatt_pos) 6.5 V	9 V	12 V	15 V	Units
Sleep mode	18	20	22	25	mW
CPU idle (note 19)	820	890	970	1000	mW
CPU at max (note 20)	1630	1700	1800	1900	mW

Notes: Power consumption was measured under the following conditions:

19. Fully populated 64 MiB Bitsy Plus with no peripheral connections. System running only the Windows CE desktop (predominantly in Idle mode; <5% CPU utilization)
20. Fully populated 64 MiB Bitsy Plus with no peripheral connections. Full (95-100%) processor utilization achieved by running multiple instances of a graphical application





6.2.6 ADSmartIO Controller

The ADSmartIO Controller is a second RISC microcontroller on the Bitsy Plus designed to handle I/O functions autonomously. The Bitsy Plus communicates with the ADSmartIO controller using the SA-1110 SPI bus. On the Bitsy Plus, ADSmartIO is implemented with the Atmel AVR 8535 microcontroller, which has 512 bytes EEPROM.

Absolute Maximum Ratings

Input voltage, any pin ..... 3.8 V

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	ADSmartIO supply voltage		3.3		V
Rs	Series resistance (note 21)		1		kΩ
Vprot	(note 21)				V
Digital Outputs (4.3.3)					
Vol				0.5	V
Voh		2.3	3.3		V
I sink	(see notes 21, 22)			20	mA
I source	(see notes 21, 22)			12	mA
Digital Inputs (4.3.3)					
Vih		0.6			Vdd
Vil				0.3	Vdd
R	Software-selectable pull-ups to 3.3 V (see note 23)	35		120	kΩ
A/D Inputs (4.3.4)					
n	resolution (note 24)		8	10	bit
Rin			100		MΩ
Vref	A/D reference voltage (note 25)		2.5		V
Ivref	Current drain from ref voltage			100	uA
Vin	valid A/D input voltage range	0		Vref	V
I (Vref)	J10.43			100	µA
Temperature Sensing (4.3.5)					
Rth	external thermistor resistance @ 25C		33		kΩ
Vt	thermistor excitation voltage		Vref		V
Rtl	lower voltage divider		47		kΩ
I2C Bus (4.5.4, note 26)					
	Bus clock		50		kHz
	input buffer size			32	byte
	packet size			32	byte
Vi/o	I/O voltages	see digital I/Os, above			V
Rbus	pull-up on SDA, SCK		4.7		kΩ
Vbus			3.3		V

Notes:

21. Row and column I/Os have series resistance and overvoltage protection to ground. The series resistance limits the dc current that any one pin can source or sink.
22. SMTIO0-3 are directly connected to I/O controller without external protection.
23. Control pull-up resistors by writing to bits of IO port when the port is configured as a digital input (bit mask 1=enable, 0=disable).
24. Digital noise on the board may degrade analog performance under some conditions.
25. Vref turns off when the system is in Sleep mode (section 5.3.2).
26. Specifications based on ADSmartIO release 1010 rev 2 (ADS release #700114-10102)

6.2.7 System Controller with Digital I/Os

A Xilinx XC3064 CPLD on the Bitsy Plus manages the RqOnOff, CONN_PE1/PE2(5.3.2) and "EIOn" digital I/O signals. It is programmed at the factory using the JTAG interface (3.3.5).

The EIOn digital I/O signals go directly to the pins of J3 (3.3.3) and J10 (3.3.8) without any series resistance or ESD protection. **It is the responsibility of the integrator to provide protection for these lines suitable to the application for which they are being used.**

Absolute Maximum Ratings

Input voltage, digital I/O pins .....-0.5 to 5.5 V

Output current, continuous,
digital I/O pins .....-100 to 100 mA

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	Supply voltage		3.3		V
Digital Outputs					
Vol		0		0.4	V
Voh		2.4			V
Digital Inputs					
Vil		0		0.8	V
Vih		2.0		3.5	V

6.2.8 USB

The Bitsy Plus supports USB operation as described in section 4.5.2. The USB_PWR_SENSE and USB_PWR_CTRL lines are SA-1111 control lines. See section 6.2.12 for their electrical characteristics.

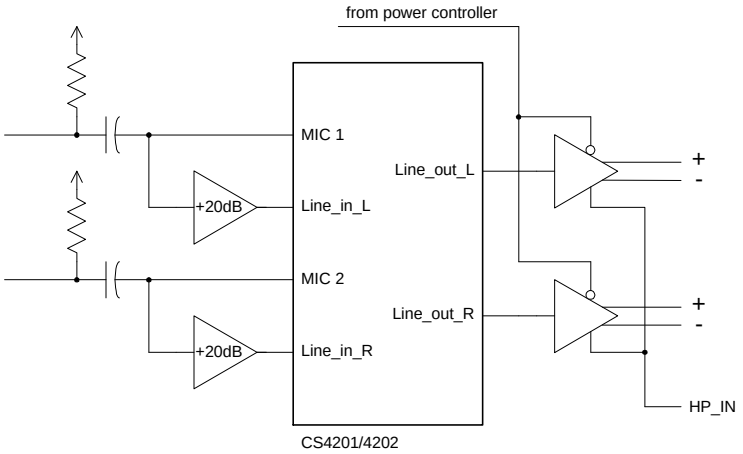
Symbol	Parameter	Min	Typ.	Max	Units
Host Port					
R_pwr_sense	USB_PWR_SENSE Pull-up to Vddx		47		kΩ

6.2.9 Audio

For its audio sub-system the Bitsy Plus uses the Crystal CS4201 or CS4202, AC'97 stereo codecs with dual audio input and output channels. The Bitsy Plus adds an output power amplifier (National LM4863LQ) and a microphone pre-amp with power for electret microphones.

The output amplifier supports differential and single-ended modes. When the HP_IN signal is greater than V(HP_IN), the amplifier is in single-ended mode; when lower, it is in differential mode.

The following diagram illustrates the relationship of the Bitsy Plus signal amplifiers to the codec:



The Bitsy Plus microphone circuitry can be factory configured to support "line in" inputs (1 Vrms with no electret pull-ups) and different input gain and filtering. If a special configuration needed for your project, consult ADS Sales with information about your requirements.

Absolute Maximum Ratings

Vin_mic ..... 5 Vdc

Symbol	Parameter	Min	Typ.	Max	Units
DVdd	codec digital supply voltage		3.3		V
Avdd	codec analog supply voltage		5.0		V
fso	sample rate, output		48		kHz
fsi	sample rate, input (note 27)	8		44.1	kHz
Audio Input					
Vin_mic	signal input voltage		100		mV_{rms}
Gain_mic	pre-amp gain		20		dB
fo_mic	pre-amp low-pass cutoff (note 28)		3.4		kHz
Rin_mic	input impedance		12.5		kΩ
Cin_mic	DC blocking capacitor		1		µF
Vmicpwr	microphone power (MIC_L/R+)		5		V
Rmicpwr	microphone power, series resistance			3.2	kΩ
Audio Output					
Rl	speaker load	4	8		Ω
Vout	Zspkr=4Ω, differential mode			3.7	V_{rms}
Vdc	DC bias, differential mode		0.5		Avdd
Pspkr	output power, ea. channel (note 29)				
	differential, THD+N 1%, Rl 4Ω		1.0	2.2	W
	differential, THD+N 10%, Rl 4Ω		1.0	2.7	W
	differential, THD+N 1%, Rl 32Ω		1.0	0.34	W
	single-ended, THD+N 0.5%, Rl 32Ω		75	85	mW
	single-ended, THD+N 1%, Rl 8Ω			340	mW
	single-ended, THD+N 10%, Rl 8Ω			440	mW
R HP_IN	pull-up to Vcc			100	kΩ
V HP_IN	threshold voltage		4		V

Notes:

27. The output sample rate is fixed, but the input sample rate can be set to 8, 11.025, 22.05 or 44.1 kHz.
28. Pre-amp anti-aliasing filter rolls off at 3dB/octave (first-order filter)
29. Typical values are guaranteed to National Semiconductor's AOQL (Average Outgoing Quality Level) Operating above typical values for a sustained period of time may result in thermal shutdown of the amplifier.

6.2.10 SA-1110 Processor

The StrongARM SA-1110 core uses system voltage Vddi (6.2.4) to achieve lower power consumption at high clock rates. It uses voltage Vddx to power its interface I/Os.

Absolute Maximum Ratings

Input voltage, digital I/O pins ..... 3.6 V

Symbol	Parameter	Min	Typ.	Max	Units
Digital Outputs					
Vol			0		V_{ddx}
Voh			1.0		V_{ddx}
Io		-2		2	mA
Digital Inputs					
Vil				0.2	V_{ddx}
Vih		0.8			V_{ddx}

6.2.11 Crystal Frequencies

Agencies certifying the Bitsy Plus for compliance for radio-frequency emissions typically need to know the frequencies of onboard oscillators. The following table lists the frequencies of all crystals on the Bitsy Plus.

Note that the frequency of the StrongARM crystal X4 is multiplied internally by 4n, where n is a value from 4 to 14, to achieve the processor core frequency. The system bus runs at half the processor's core frequency.

Crystal	Device	Typ.	Units
X1	RTC	32.768	kHz
X2	ADSmartIO microcontroller	3.6864	MHz
X3	StrongARM RTC	32.768	kHz
X4	Strong ARM core	3.6864	MHz
X5	Codec	24.576	MHz

6.2.12 SA-1111 Companion Chip

The SA-1111 is a companion to the StrongARM SA-1110. It provides a number of features that supplement the core processor. These include a USB Host Controller, PCMCIA/CF control logic and buffers, interface to an AC'97 codec, DMA controllers and an interrupt controller, among others.

On the Bitsy, the CompactFlash (CF) port can be used as a digital expansion bus. Signals for PCMCIA, CF and the expansion bus are broken out into a separate section, below.

Absolute Maximum Ratings

Input voltage, digital I/O pins ..... 3.8 V

Input voltage, CF port I/O pins..... 5.5 V

Symbol	Parameter	Min	Typ.	Max	Units
V_{ddx}	SA-1111 I/O voltage		3.3		V
V_{ccb}	CARDBVcc: CF port voltage (note 30)	3.3	5.0	5.0	V
Digital Outputs					
Vol			0		V_{ddx}
Voh			1.0		V_{ddx}
Digital Inputs					
Vil	Vddx=3.3 V			0.2	V_{ddx}
Vih	Vddx=3.3 V	0.8			V_{ddx}
SPI Bus (section 4.5.3)					
	Bit rate		460	1840	kHz

Notes:

30. The CF port voltage is selected programmatically with the SA-1111. The socket is keyed for 5V-tolerant CF cards.

PCMCIA, CompactFlash Port and Expansion Bus

The CompactFlash bus can be used as a digital expansion port on the Bitsy Plus. The following are specifications for the CF port used as an expansion bus.

Symbol	Parameter	Min	Typ.	Max	Units
I 3.3V	3.3 V socket current (Note 31)		2		W
I 5V	5 V socket current (Note 31)		2.5		W
Rp pcmcia	Card detect (1 & 2) and voltage sense (VS1 & 2) pull-ups (Note 32)		100		kΩ
Vp pcmcia	Card detect and voltage sense pull-up voltage (Note 33)	Vddx	Vcc	Vcc	V
Digital Outputs					
Vol			0		V_{ccb}
Voh			1.0		V_{ccb}
I sink					mA
I source				4	mA
Digital Inputs					
Vil	V_{ccb}=3.3 V			0.325	V_{ccb}
	V_{ccb}=5.0 V			0.8	V
Vih	V_{ccb}=3.3 V	0.475			V_{ccb}
	V_{ccb}=5.0 V	2.4			V

Symbol	Parameter	Min	Typ.	Max	Units
Timing (Note 34)					
t mem	system memory clock		9.7		us
t setup1	address setup to command, first access	2		97	t mem
t setup2	address setup to command, second access	1		64	t mem
t access	nRD/WR duration, first access	3		97	t mem

Notes:

31. Total power available depends on system power budget (5.4.1).
32. Each card inserted in a PCMCIA or CF slot can drain up to 1 mW when the system is in Sleep mode (4 * Vcc^2/Rpcmcia).
33. The PCMCIA/CF voltage is software-selectable. External implementations of the CF bus (i.e. on a Personality Board) can hard-wire the voltage to Vddx or to Vcc.
34. The SA-1110 MECR register independently sets timings for the attribute, IO and memory spaces of the CF bus in 32 steps. Values shown assume 206 MHz CPU clock. Min values are with Fast bit=1, max values are with Fast bit=0.

7 Board Revision History

7.1 Identifying the board revision

The product revision number of the Bitsy Plus is etched on the underside of the printed circuit board. That number is 170114-1000x, where "x" is the board revision.

7.2 Revision History

7.2.1 Revision 2

Initial release. If you are using a Bitsy Plus as a replacement for the Bitsy, please note these changes from the Bitsy (rev C):

New Features

AC'97 stereo codec with improved signal to noise ratio

Burr-Brown touch-panel controller. A five-wire controller can be installed as a factory option.

Supports wakeup from touch screen.

Real-time clock circuit with micro power sleep

Option to populate supercapacitors

VCON signal on display connector, J1 (low-voltage contrast control of some passive displays)

Some subsystems on the Bitsy Plus can be powered off selectively. Two power enable signals are available to manage power of off-board peripherals.

Support for synchronous flash

External interrupt /EXT_IRQ3

SPI bus master (SA-1111)

I2C master functionality (ADSmartIO)

Enhancements

The power supply has been redesigned for improved efficiency and higher input voltage range

Improved Vee generator for passive panel support

Additional ground and power connections on J3 and J10

Improved analog performance for audio system

EIOn digital I/Os can source and sink significantly more current (section 6.2.7)

Changes

DIP switch S1 has two positions instead of four

Voltage “3.3V” is now the same as “VDDX”

Voltages Vddx and Vcc are always on.

Touch panel connector J8 removed. Signals are available on J3.

Signals on J3 change as follows:

Pin	From	To
4	*AGCSTAT*	*GND*
6	*CODEC_OFL*	*GND*
8	*AMP_SDWN*	*VCC*
10	*QMUTE*	*VCC*
21	*SPK+*	*WIPER*
22	*SPK-*	*CHARGE*
23	*MICGND*	*GND*
24	*MICSIG*	*PE2*
31	*SW2*	*GND*
32	*+30V*	*HP_IN*
33	*SW3*	*n/c*
34	*+30V_GND*	*GND or n/c*
35	*DATAI*	*SRXD*
37	*DATAO*	*STXD*
39	*BCLK*	*SCLK2*
42	*VDDI*	*/PE1*
43	*WS*	*SFRM2*
46	*DCIN_NEG*	*GND*
47	*GPIO27_CLK*	*GND*
48	*12V_IN*	*DCIN_POS*

Signals on J10 change as follows:

Pin	From	To
35	*ANIN0*	*/EXT_IRQ3*
37	*ANIN1*	*VDDX*
39	*ANIN2*	*MIC_GND*
41	*ANIN3*	*MIC_GND*
46	*/SHDN_RS232*	*VCC*

DIP switch signals SW2 and SW3 on connector J3 have been eliminated

JP4 is now the Vee selector. The panel data voltage is factory-selected with R288 or R289

JP1, JP2 and JP5 (formerly Vee settings) have been removed

JP4 has been changed from flat panel voltage select to Vee polarity select

The BATPOS input no longer powers the system in sleep mode. It only powers the RTC

The "30V" output has been removed

UCB1200 codec and I/O chip has been removed. Digital I/O functions (EIO0-9)are handled by a programmable logic device. The mono microphone and speaker are no longer available, nor are the four analog input channels that the UCB1200 formerly provided. A/D inputs are still available on the ADSmartIO.

Option to pull /BacklightOn signal up to 12V_IN (J3.48) is no longer available (this can be done on the personality board).

3.3V pull-up on /IRDAON signal removed

/EXT_IRQ1 and /EXT_IRQ2 interrupts are mapped to different SA-1111 ports

/EXT_IRQ2 doesn't have pull-up or pull-down

7.2.2 Revision 3

Internal release

7.2.3 Revision 4

Internal release

7.2.4 Revision 5

New Features

USB_Reconn signal added at J3 pin 33 (formerly n/c) (SA-1110 GP12) (4.5.2)

Can turn off ADSmartIO analog voltage reference (Vref) as part of subsystem partitioning

Production option to bypass audio amplifier

ADSmartIO now can monitor the DC_GOOD signal (VBATT_NEG is a production option).

Enhancements

Expanded backlight PWM voltage range from 3.3 V to 5 V (option for 3.3 V)

Codec reset control (SA-1110 GP11)

Reduced sleep mode current

Improved touch panel operation (lower noise)

Improved audio codec operation through additional power and ground partitioning

Height of tallest component on bottom side of board reduced from 0.185 inches (4.70 mm) to 0.126 inches (3.20 mm)

Changes

Flash reset now controlled by system reset. Resolves condition under which system will sometimes not reboot from hard reset.

PCMCIA power control updated to allow full cut-off of power

PCMCIA 3.3V power control enable signal has inverse polarity

RqOnOff signal management now passed through CPLD and handled by ADSmartIO.

System can wake up after a touch screen event

7.2.5 Revision A

Enhancements

Temperature sensor input has 2x improved resolution across industrial temperature range.

Reduced sleep current

Adds support for CS4202 audio codec

Improved Vddx performance with 5V-only systems

Changes

ADSmartIO voltage reference turns off when system is asleep

R_{tl} (thermistor base resistor) changed from 3.3kΩ to 47kΩ to improve temperature resolution.