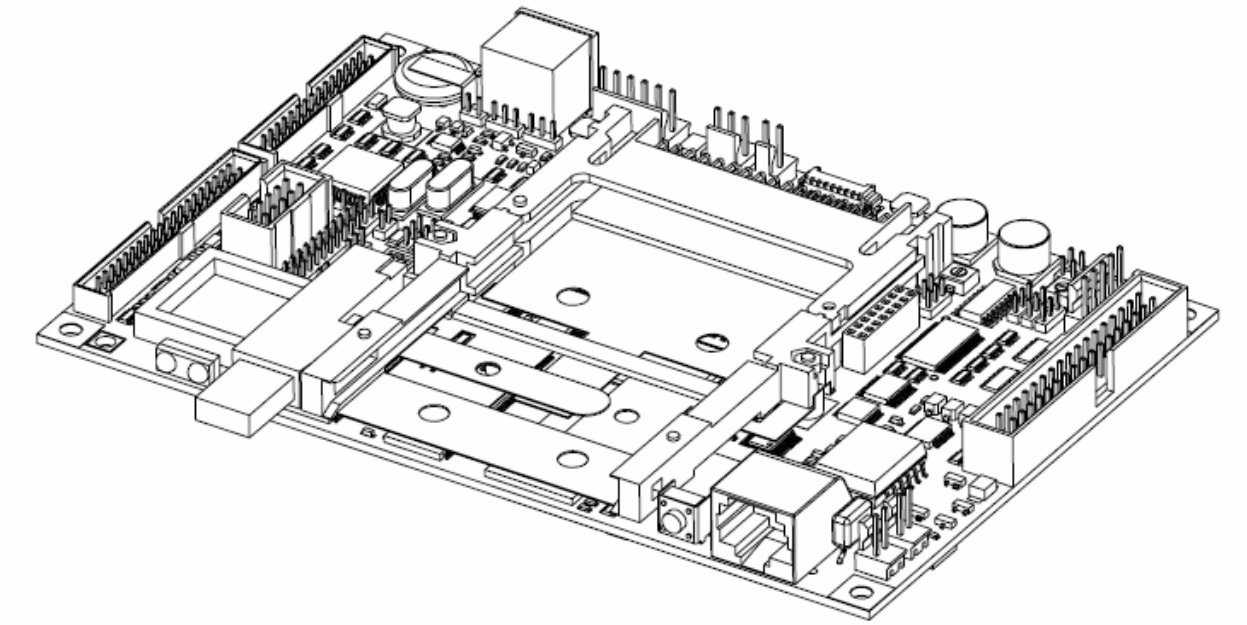
Applieddata.net
Embedded Computer Systems

# GCX Graphics ClientX
# User's Manual

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## About the Cover Image

The cover image shows a fully populated Rev B GCX with PCMCIA ejector, RTC battery and IrDA transceiver installed. The boot ROM socket shown in the diagram is a factory option.

## Printing this Manual

This manual has been designed for printing on both sides of an 8.5x11 inch paper, but can be printed single-sided as well. It has also been optimized for use in electronic form with active cross-reference links for quick access to information.

## Revision History

The following list summarizes the changes that have been made between released revisions of the manual.

| REV | DESCRIPTION | BY |
|---|---|---|
| 1 | Preliminary release | 1/14/05 ak |
| 2 | Second preliminary release (major revision) | 8/17/05 ak |

# Table of Contents

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# 1 Introduction

## *1.1 Overview*

The Graphics ClientX (GCX) is a complete single board computer featuring the PXA255 XScale RISC microprocessor. The GCX is designed to meet the needs of embedded and graphical systems developers and provides a forward upgrade path from the ADS Graphics Client Plus.

This manual applies to the most current revision of the GCX listed in Chapter 7, the Revision History.

## *1.2 Features*

### 1.2.1 Processor

- PXA255 32-bit XScale Applications Processor
- 400 MHz CPU clock, typical
- Voltage and frequency scaling

### 1.2.2 Power Supply

- 5 V main power
- System backup and real-time clock power inputs

### 1.2.3 Memory

- 64 MiB synchronous DRAM [1] [2]
- 32 MiB flash RAM [3]
- PCMCIA, Type I and II, 3.3 and 5 V

### 1.2.4 Communications

- Three Serial Ports
  - Serial 1: EIA/TIA-232, 3.3V logic (5-wire), EIA/TIA-422/485 or J1708
  - Serial 2: EIA/TIA-232, 3.3V logic (5-wire) or IrDA
  - Serial 3: EIA/TIA-232 or 3.3V logic (9-wire)
- 10/100BT Ethernet, RJ45
- 1 Mbps CAN Bus Controller
- PCMCIA

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[1] The GCX supports 16, 32 and 128 MiB SDRAM for volume production orders.

[2] MiB is the IEC abbreviation for mebibyte = $2^{20}$ byte = 1 048 576 byte. The kibi and mebi abbreviations are based on the 1998 IEC standard for binary multiples. For further reading, see the US NIST web site, http://physics.nist.gov/cuu/Units/binary.html

[3] The GCX supports 8, 16 and 32 MiB of synchronous flash memory and 16, 32 and 64 MiB of and asynchronous flash. These memory options are available for volume production orders.

### 1.2.5 User Interface and Display

- PXA255 display controller
- Logic-level, digital flat panel interface
- Backlight intensity and on/off control signals
- Software-controlled VEE generator for passive LCD contrast control (factory option)
- Four-wire analog-resistive touch panel interface (five-wire for volume production orders)
- PS/2 keyboard port

### 1.2.6 Discrete I/O

- 20 ADSmartIO™ ports configurable for digital I/O and/or up to 8x8 matrix keypad
- 14 additional general-purpose digital I/Os
- Three A/D inputs

### 1.2.7 Audio Interface

- Twenty-bit AC '97 Codec
- Microphone input
- 700mW speaker output or stereo headphone output (factory option)

## 1.3 Block Diagram

The following diagram illustrates the system organization of the GCX. Arrows indicate direction of control and not necessarily signal flow.

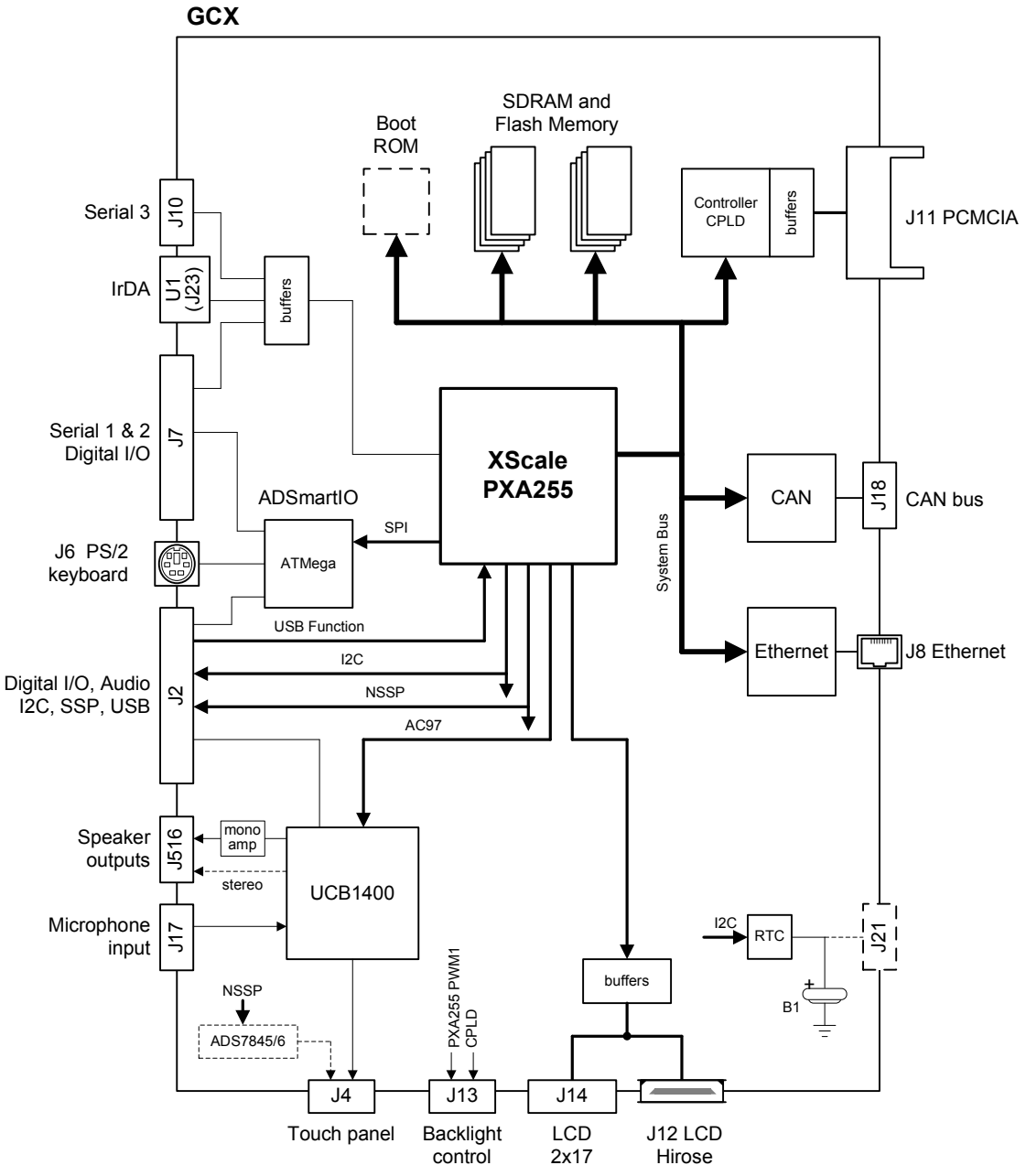


**Figure 1 GCX Functional Block Diagram**

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# 2 Getting Started

## 2.1 Development Systems

GCX boards are shipped as development systems designed to get the developer up and running quickly.

***To use the system, simply plug power supply into the mini DIN-8 receptacle on the system.***

If the screen does not display anything after five to ten seconds, check the *Frequently Asked Questions*, below. Most operating systems cold boot within twenty seconds.

### 2.1.1 System Components

A typical development system is shown at right (system at right illustrates a BitsyX development system). It consists of the following components:

- GCX single-board computer
- Flat panel display and cable
- Backlight inverter and cable
- Touch screen and cable
- 120/240 VAC power adapter
- Plexiglas mounting
- Developer's Cable Kit including
  - Serial Port DB9 adapter (ADS cable #610110-4004)
  - DB9F/F null modem cable
- Operating system of your choice
- User's Guide (this document and operating system guide)

Please make sure you have received ***all*** the components before you begin your development.

## 2.2 Frequently Asked Questions

The following are some of the most commonly asked questions for development systems:

**Q: When I plug in power, my screen is white and nothing comes up on it.**

A: Check the connector seating. The flat panel connector may have come loose in shipping. Press it firmly into the panel and reapply power to your system.

**Q: When I plug in power, the LED doesn't turn on.**

A: Your system may still be booting. The LED is software controlled and is not necessarily turned on at boot.

**Q: Do I have to turn off the system before I insert a PCMCIA card?**

A: No. The GCX supports hot-swapping of PCMCIA cards. Consult the operating system documentation for details.

**Q: Do I need to observe any ESD precautions when working with the system?**

A: Yes. Where possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the board or touching any components on the board.

**Q: What do I need to start developing my application for the system?**

A: You will need a flash ATA card (16 MiB or larger, 32 MiB recommended) and the cables supplied with your system to interface your development station to the system. For further direction, consult the ADS guide for the installed operating system.

**Q: Who can I call if I need help developing my application?**

A: ADS provides technical support to get your development system running. For customers who establish a business relationship with ADS, we provide support to develop applications and drivers.

**Q: Is there online support?**

A: Yes. Information about the GCX hardware and software is available on the ADS support site at http://www.applieddata.net/support. See section 2.4 for further details.

**Q: Can I upgrade the version of the operating system?**

A: Yes. ADS provides regular operating system updates on its developers' web site. For operating systems not maintained by ADS, contact the operating system vendor.

**Q: I would like to interface to a different display panel. How can I do this?**

A: ADS may have already interfaced to the panel you are interested in. Consult ADS for availability.

## 2.3 Organization of this Manual

The manual organizes information in five key sections:

| | |
|---|---|
| **Introduction** | Provides an overview of the functionality and organization of the GCX, as well as how to use this manual. |
| **Hardware Reference** | Describes the configuration settings and pinouts for all connectors and jumpers on the GCX. |
| **Feature Reference** | Gives details about the various subsystems of the GCX. |
| **Power Management** | Provides key information about power management, tips for system integration and electrical and mechanical interface specifications. |
| **Specifications** | Electrical and mechanical interface specifications. |

To locate the information you need, try the following:

1. Browse the *Table of Contents.* Section titles include connector designators and their function.
2. Follow cross-references between sections.
3. View and search this manual in PDF format

## 2.4 Errata, Addenda and Further Information

Errata and addenda to this manual are posted on the ADS support forums along with the latest release of the manual. Consult the support forums any time you need further information or feel information in this manual is in error. You may access the forums from the ADS support site,

**http://www.applieddata.net/support**

In addition to manuals, the support forums include downloads, troubleshooting guides, operating system updates and answers to hundreds of questions about developing applications for ADS products. You may also post questions you have about ADS products on the forums.

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# 3 Hardware Reference

This section gives an overview of the hardware features of the GCX. This overview includes a description of the switches, jumper settings, connectors and connector pinouts.

## *3.1 Identifying Connectors*

The section describes how to locate connectors on the board and how to determine how each header is numbered.

### 3.1.1 Locating Connectors

The following diagram illustrates the location of key components on the GCX. For example, the PS/2 socket is located in square A2 and the reset button is in D5. Component listings elsewhere in this chapter refer to this diagram.

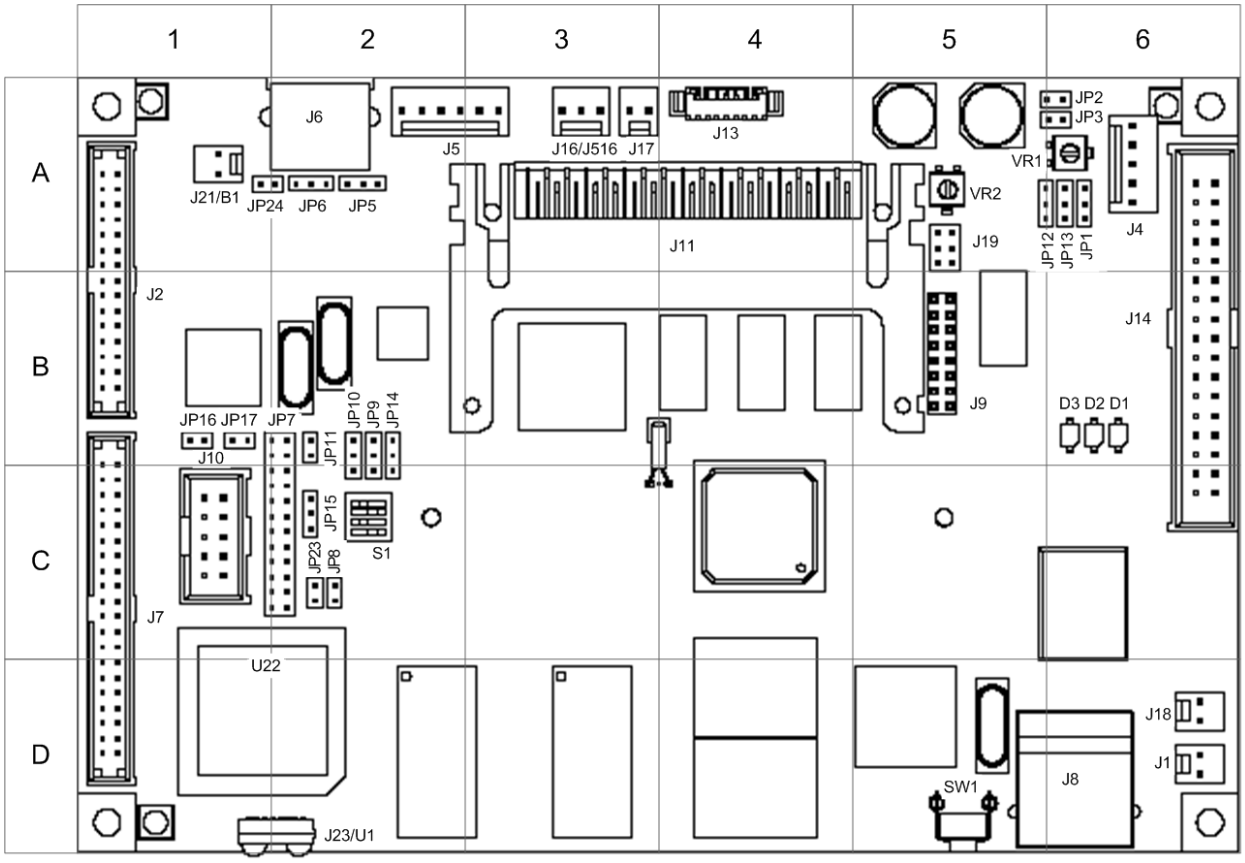
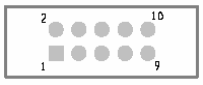



**Figure 2 GCX Connector Locator**

### 3.1.2 Determining Pin Numbers

The pins of headers and connectors on ADS products are numbered sequentially. Double-row headers place even pins on one side and odd pins on the other. The diagram at right indicates how pins are numbered, as seen from the component side[4] of the board.




[4] The "component side" of the GCX is the one on which the PCMCIA ejector is installed. As a factory option, some through-hole connectors may be installed on the "bottom side" of the GCX.

To locate pin 1 of a connector or jumper, try the following:

1. Look for a visible number or marking on the board that indicates connector pin numbering. A notch or dot usually indicates pin 1.

2. Look at the underside of the board. The square pad is pin 1.

3. Download the mechanical drawing of the GCX from the ADS Support site (section 2.4). The square or indicated pad on each connector is pin 1.

## *3.2 Switches, Controls and Indicators*

This section describes various switches, controls and indicators on the GCX board. The location indicated for each item refers to the grid diagram of the GCX in section 3.1.1.

### 3.2.1 S1: DIP Switch

Location on board: C2

S1 is a four-position DIP switch. When in the "ON" position, switches are closed and connect to ground. Otherwise they are pulled up. The DIP switches connect to the system controller.

Most GCX bootloaders reserve these switches for their use. Consult the operating system manual for details.

### 3.2.2 SW1: Reset Switch

Location on board: D5

SW1 is the reset button for the GCX. This switch issues a hardware reset to the PXA255 and system peripherals. Press this button to restart the GCX without cycling power. Most operating systems clear the contents of DRAM when a hardware reset occurs. You can hold the GCX in reset by pressing and holding this button.

### 3.2.3 LED Indicators

The GCX has several onboard light-emitting diodes (LEDs) to indicate system operation. Some are software-controllable, while others indicate the status of specific functions.

#### *Software-Controllable LEDs*

Location on board: B6

Three LEDs are controlled by the CPU (section 4.1.5) and are used to indicate boot and operating system status. These LEDs can often be used by applications to indicate operational status.

| Designator | Color | Signal | Controlled by |
|---|---|---|---|
| *D3* | *Green* | *LED0* | *PXA GP20* |
| *D2* | *Amber* | *LED1* | *PXA GP19* |
| *D1* | *Red* | *LED2* | *PXA GP21* |

The LEDs are driven by the same buffers as the display driver data lines, so will be off when the display buffers are disabled. The driver voltage for the buffers is selected by JP13.

#### *Ethernet LEDs*

Location on board: D6 (Ethernet socket J8)

Two LEDs integrated into Ethernet socket J8 indicate when a valid Ethernet connection has been made and when there is activity on the bus.

### 3.2.4 IrDA Transceiver

Location on board: D1-D2

U1 is an IrDA transceiver that converts Serial 2 electrical signals to infrared light pulses for IrDA communications. For volume production orders, U1 can be replaced with a socket (J23) for cabling to an external transceiver. See section 4.5.2 for further details.

### 3.2.5 VR1: Vee Contrast Adjustment (factory option)

Location on board: A6

Vee is the contrast adjustment voltage required for most passive LCD displays. VR1 and a PWM signal set the output voltage for Vee. See JP12 and section 4.8.2 for further details.

### 3.2.6 VR2: Vcon Contrast Adjustment (factory option)

Location on board: A5

Vcon is used to adjust the contrast for some passive LCD displays. See section 4.8.2 and Note 14 of section 6.4.4 for further details.

## *3.3 Jumper Settings*

Jumpers on the GCX select a variety of operational modes. All use 2mm shorting blocks (shunts) to select settings. Turn off power to the GCX before changing the position of a shunt.

The location indicated for each item refers to the grid diagram of the GCX in section 3.1.1

### 3.3.1 JP1: LCD Display Power

Type: 3-post header, 2mm
Location on board: A6

This jumper selects the supply voltage for the LCD display. The voltage selected here is passed to the *PNL_PWR* pins on J14 (3.4.13) and J12 (3.4.11).

| Jumper setting | Voltage Selected |
|---|---|
| *1-2* | *Vddx (3.3 V)* |
| *2-3* | *Vcc (5.0 V)* |

WARNING! Make sure you have selected the correct voltage before connecting the panel. Flat panels can be irreparably damaged by incorrect voltages.

IMPORTANT: This shunt is populated at the factory to match the voltage of the signal buffer circuits populated on the board. While the buffers may perform adequately at a different voltage than what was set at the factory, ADS cannot guarantee long-term performance.

### 3.3.2 JP2: LCD RL Signal

Type: 2-post header, 2mm
Location on board: A6

This jumper determines the voltage for the PNL_RL signal on J14 and J12. On some active-matrix LCD displays, the PNL_RL signal flips the displayed image right-to-left.

| Jumper setting | Connects RL to… |
|---|---|
| *1-2* | *GND* |
| *n/c* | *PNL_PWR* |

### 3.3.3 JP3: LCD UD Signal

Type: 2-post header, 2mm
Location on board: A6

This jumper determines the voltage for the PNL_UD signal on J14 and J12. On some active-matrix LCD displays, the PNL_UD signal flips the displayed image bottom-to-top.

| Jumper setting | Connects UD to… |
|---|---|
| *1-2* | *GND* |
| *n/c* | *PNL_PWR* |

### 3.3.4 JP5: Source of Sleep Mode Power

Type: 3-post header, 2mm
Location on board: A2

This jumper selects the source of power to back up the GCX when it is in sleep mode. See chapter 5 for further details.

| Jumper setting | Voltage Selected |
|---|---|
| *1-2* | *Vperm (J5 pin 6)* |
| *2-3* | *Vcc (5.0 V, J5 pin 1)* |

### 3.3.5 JP6: Source of 3.3 V Power (Vddx)

Type: 3-post header, 2mm
Location on board: A2

This jumper selects the source of 3.3 V power, Vddx, for the system.

Standard production systems include an onboard 3.3 V regulator, but the GCX will also run from an external 3.3 V supply (+3.3V_IN from J5, pin 3). See section 6.2 for further details about related production options.

| Jumper setting | Vddx is supplied by… |
|---|---|
| *1-2* | *external source* |
| *2-3* | *onboard regulator* |

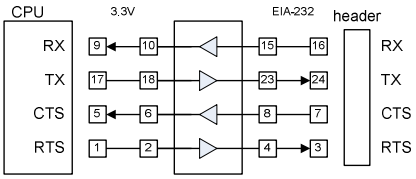
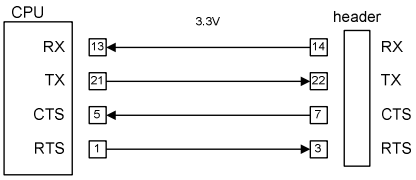
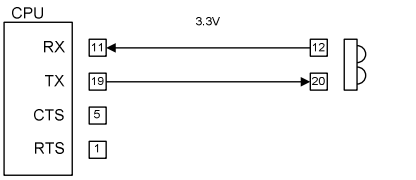
### 3.3.6 JP7: Serial 2 Mode Select

Type: 2x12 header, unshrouded 2mm
Location on board: B2-C2

This header selects the communication mode of PXA255 Serial Port 2.

The operating system must configure the processor for the target serial mode. The table below lists the standard voltages to expect on the transmit line of the port when the transmitter is idle.

Important: When using Serial 2 as IrDA, make sure that the operating system configures the port as IrDA. Otherwise, the transmitter may be enabled continuously, which can drain significant amounts of power and may overheat and damage the IrDA transmitter.

| Serial 2 Mode | Jumper Settings | Resulting Circuit | Tx $V_{idle}$ |
|---|---|---|---|
| *EIA/TIA-232* |  *1-2, 3-4, 5-6, 7-8, 9-10, 15-16, 17-18 23-24* |  | *-6 V* |
| *3.3 V logic* |  *1-3, 5-7, 13-14, 21-22* |  | *3.3 V* |
| *IrDA* |  *11-12, 19-20* |  | *0 V* |

### 3.3.7 JP8-11, JP14-15: Serial Port 1 Mode Select

Type: 3-post headers, 2mm
Location on board: B2-C2

Serial port 1 can be field-configured for operation in RS-232, RS-422 and RS-485 modes. It can also be factory-configured for J1708 or 3.3 V logic operation for volume production orders (see section 6.2 for details).

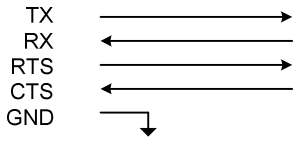
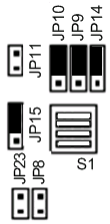
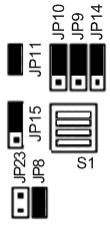
Jumpers JP6, JP7 and JP10 through JP13 select between RS-232 and RS-485/422 mode and set the duplex mode of RS-485/422.

RS-422 and RS-485 are differential serial protocols with the same voltage characteristics. RS-422 is a point-to-point protocol while RS-485 turns off the transmitter when not in use, allowing multi-

drop installations. Each can be configured in half- or full-duplex mode. The GCX supports RS-422 by leaving the transmitter enabled all the time.

In half-duplex mode, TX+/RX+ and TX-/RX- are shorted together. Half-duplex devices can see their own transmissions. Connect to either the + or – connection on J7, but make sure to observe correct polarity.

Headers shaded gray in the following table are not relevant to the mode listed, but are shown for reference.

| Serial 1 Mode | Jumper Settings | Standard Signals |
|---|---|---|
| *EIA-232* |  |  |
| *RS-485/422 Full Duplex* |  |  |
| *RS-485 Half Duplex, J1708* |  |  |

## 3.3.8 JP12: Vee Control (factory option)

Type: 3-post header, 2mm
Location on board: A5

Jumper JP12 selects how Vee is adjusted. If the shunt set for manual operation, VR1 (3.2.5) controls the Vee output. Setting the shunt to software-controlled operation adds a connection to the Vee PWM, which allows software to adjust the Vee output voltage. In software-controlled mode, VR1 is still used to calibrate the standard Vee output (usually at room-temperature).

| Jumper setting | Vee adjustment |
|---|---|
| *1-2* | *Software-controlled + VR1* |
| *2-3* | *Manual (VR1 only)* |

### 3.3.9 JP13: LCD Display Data Voltage

Type: 3-post header, 2mm
Location on board: A6

This jumper selects the voltage for the data signals to the LCD display.

Important: These jumpers are set at the factory to match the panel and drivers shipped with the system. You may damage the panel or panel drivers if you change this jumper setting.

See section 6.2 for details about production options available to support different display data voltages.

Tip: Most 5 V panels will run correctly with 3.3 V data.

| Jumper setting | Data to display is… |
|---|---|
| *1-2* | *3.3 V (Vddx)* |
| *2-3* | *5.0 V (Vcc)* |

### 3.3.10 JP16: Serial 3 DCD-DTR Loopback

Type: 2-post header, 2mm
Location on board: B1

This jumper connects together the DCD and DTR signals on J10.

Note: These loopback shunts are a holdover from the Graphics Client Plus design, when the DTR, DSR and DCD signals were not connected. Leave this and jumper JP17 unconnected for normal serial port operation.

| Jumper setting | Function |
|---|---|
| *none* | *normal 9-wire operation* |
| *1-2* | *Shorts together J10 pins 1 (DCD) and 7 (DTR)* |

### 3.3.11 JP17: Serial 3 DSR-DTR Loopback

Type: 2-post header, 2mm
Location on board: B1

This jumper connects together the DSR and DTR signals on J10.

Note: These loopback shunts are a holdover from the Graphics Client Plus design, when the DTR, DSR and DCD signals were not connected. Leave this and jumper JP16 unconnected for normal serial port operation.

| Jumper setting | Function |
|---|---|
| *none* | *normal 9-wire operation* |
| *1-2* | *Shorts together J10 pins 2 (DSR) and 7 (DTR)* |

### 3.3.12 J19: Vee Polarity (factory option)

Type: 2x3-post header, 2mm
Location on board: A5

This jumper selects the polarity of Vee, the contrast control voltage for passive LCD displays. Vee is controlled with a PWM signal from the ADSmartIO. See section 4.8.2 for further details

| Jumper setting | Function |
|---|---|
| *none*  | *No Vee output* |
| *2-4*  | *Positive Vee* |
| *3-4*  | *Vbacklight from J5.4* |
| *4-6*  | *Negative Vee* |

### 3.3.13 JP23: Serial 1 RS-485 Terminator

Type: 2-post header, 2mm
Location on board: B1

Install this jumper to make the GCX (Serial 1) the last device in an RS-485 network. Shorting the pins of this header places a 120 Ω termination resistor across the RS-485 RX lines.

| Jumper setting | RS-485 Terminator… |
|---|---|
| *1-2* | *installed* |
| *n/c* | *not installed* |

### 3.3.14 JP24: Use Onboard Power Supply for RTC

Type: 2-pin header, 2mm
Location on board: A1-A2

This shunt allows the real-time clock (RTC) circuit to be powered by the Vddx power supply.

WARNING! This shunt should only be installed only by the factory. Installing this shunt may cause damage to the onboard or external RTC battery if installed inappropriately.

| Jumper setting | Function |
|---|---|
| *none* | *RTC powered externally (J21) or by onboard battery* |
| *1-2* | *Connects Vddx (3.3 V) to RTC backup power input* |

## 3.4 Signal Headers

The following tables describe the electrical signals available on the connectors of the GCX. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions and references to related chapters.

The location indicated for each item refers to the grid diagram of the GCX in section 3.1.1 For details about how to determine pin numbers of a header, see section 3.1. For precision measurements of the location of the connectors on the GCX, refer to section 6.1.1.

Legend:

| | |
|---|---|
| n/c | Not connected |
| GND | GCX ground plane |
| (3.4) | Reference section for signals |

Signal Types

| | |
|---|---|
| I | signal is an input to the system |
| O | signal is an output from the system |
| IO | signal may be input or output |
| P | power and ground |
| A | analog signal |
| OCI | open-collector/open-drain input |
| OC | open-collector/open-drain output |

### 3.4.1 J1: Contact Closure Detect

Board connector: 2-pin header. 0.100-in spacing, Molex 22-23-2021

Location on board: D6

External input. Short these pins together to generate an interrupt on the CPU. Most ADS operating system ports use this "On/Off Request" input to wake the system and to put it to sleep.

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | */RqOnOff* | *OCI* | *CPU wakeup* |
| *2* | *GND* | *P* | *ground* |

### 3.4.2 J2: I/O, Analog Inputs, USB Function Port, NSSP, $I^2C$

Board Connector: 2x15 header, 2 mm spacing, Samtec STMM-115-02-G-D
Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: Samtec ESQT series (e.g. ESQT-115-02-F-D-500)

Location on board: A1-B1

| Pin | Name | Pin | Type | Description |
|---|---|---|---|---|
| *1* | *UCB_IO0* | | *IO* | |
| *3* | *UCB_IO1* | | *IO* | |
| *5* | *UCB_IO2* | | *IO* | |
| *7* | *UCB_IO3* | | *IO* | |
| *9* | *UCB_IO4* | | *IO* | *UCB1400 Digital I/Os (4.6.1, 6.4.5)* |
| | *UCB_IO9* | *2* | *IO* | |
| | *UCB_IO8* | *4* | *IO* | |
| | *UCB_IO7* | *6* | *IO* | |
| | *UCB_IO6* | *8* | *IO* | |
| | *UCB_IO5* | *10* | *IO* | |

| Pin | Name | Pin | Type | Description | |
|---|---|---|---|---|---|
| *11* | *ANIN0* | | *AI* | *UCB1400 Analog Inputs (4.6.2)* | |
| *13* | *ANIN1* | | *AI* | | |
| *15* | *ANIN2* | | *AI* | | |
| *17* | *ANIN3* | | *AI* | | |
| | *I2C_SCK* | *12* | *IO* | *$I^2C$ (4.5.7)* | |
| | *I2C_SDA* | *14* | *IO* | | |
| | *SMTIO2* | *16* | *IO* | *PB2* | *ADSmartIO (4.3.6)* |
| | *SMTIO3* | *18* | *IO* | *PB3* | |
| | *SMTIO4* | *20* | *IO* | *PD0* | |
| | *SMTIO5* | *22* | *IO* | *PD1* | |
| | */EXT_IRQ* | *24* | *I* | *External Interrupt* | |
| *19* | *NSSP RXD* | | *I* | *PXA255 NSSP Port (4.5.3)* | |
| *21* | *NSSP TXD* | | *O* | | |
| *23* | *NSSP SFRM* | | *O* | | |
| *25* | *NSSP SCLK* | | *O* | | |
| | *USB_VCC* | *26* | *PI* | *USB Function Port (4.5.3)* | |
| *27* | *USB_GND* | | *P* | | |
| | *USB_UDC-* | *28* | *IO* | | |
| | *USB_UDC+* | *30* | *IO* | | |
| *29* | *GND* | | *P* | *ground* | |

### 3.4.3 J4: Touch Panel

Board Connector: 1x4 header, 0.100 inch spacing, Molex 22-23-2041
Board Connector: 1x5 header, 0.100 inch spacing, Molex 22-23-2051 (factory option)
Location on board: D6

J4 connects to a four-wire analog-resistive touch panel. For volume production orders, the GCX can also be configured to drive 5-wire touch panels.

| Pin | Name | Type | Description | | |
|---|---|---|---|---|---|
| | | | *4-wire* | *5-wire* | |
| *1* | *TSMX* | *AIO* | *left* | *LL* | *Touch screen* |
| *2* | *TSPX* | *AIO* | *right* | *UL* | |
| *3* | *TSPY* | *AIO* | *bottom* | *UR* | |
| *4* | *TSMY* | *AIO* | *top* | *LR* | |
| *5* | *WIPER* | *AI* | *n/a* | *WIPER* | *5-wire option* |

### 3.4.4 J5: Input Power Connector

Board Connector: 1x6 Molex #22-23-2061, 0.1 inch spacing
Location on board: A2

J2 supplies power to the GCX. +5V_IN is the main power supply. See section 5.2.1 for an overview of how the GCX power supply is structured.

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *+5V_IN* | *PI* | *5V input power* |
| *2* | *GND_IN* | *PI* | *Ground* |
| *3* | *+3.3V_IN* | *PI* | *3.3V input power* [5] |
| *4* | *Vbacklight_IN* | *PI* | *Backlight and Vee power (5.2.1)* |
| *5* | *POWERON* | *O* | *Output for power supply management; low when system is asleep or off (5.2.1, 5.2.2)* |
| *6* | *VPERM* | *PI* | *"Permanent voltage" (5.2.1)* |

### 3.4.5 J6: PS/2 Keyboard

Board Connector: Mini DIN-6 socket housing, Singatron 2MJ-0004A110
Recommended mating connector: PS/2 mini DIN-6 keyboard plug

Location on board: A2

Socket J6 supplies power and communication signals for a PS/2 keyboard. The shell of the socket is electrically connected to the board mounting holes (chassis ground).

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *SIGPS2* | *IO* | *PS/2 keyboard data* |
| *2* | *n/c* | | |
| *3* | *GND* | *P* | *ground* |
| *4* | *VCC* | *PO* | *5 V, fused at 350mA* |
| *5* | *CLKPS2* | *IO* | *PS/2 keyboard clock* |
| *6* | *n/c* | | |
| | *shield/case* | | *connected to board mounting holes* |

[5] The onboard 3.3V regulator can be removed in cost-sensitive applications. This option is available for only volume production orders (see 6.2).

### 3.4.6 J7: ADSmartIO, Serial 1 and 2, EIA-422/485, I/O

Board Connector: 2x20 header, 2 mm spacing, Samtec STMM-120-02-G-D
Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: Samtec ESQT series (e.g. ESQT-120-02-F-D-500)

Location on board: C1-D1

| Pin | Name | Pin | Type | Description | |
|---|---|---|---|---|---|
| *1* | *ROW0* | | *IO* | *PC7* | *ADSmartIO Keypad rows or digital I/O (4.3)* |
| *3* | *ROW1* | | *IO* | *PC6* | |
| *5* | *ROW2* | | *IO* | *PC5* | |
| *7* | *ROW3* | | *IO* | *PC4* | |
| *9* | *ROW4* | | *IO* | *PC3* | |
| *11* | *ROW5* | | *IO* | *PC2* | |
| *13* | *ROW6* | | *IO* | *PC1* | |
| *15* | *ROW7* | | *IO* | *PC0* | |
| | *RXD2* | *2* | *I* | *Serial 2, EIA-232 (4.5.1)* | |
| | *TXD2* | *4* | *O* | | |
| | *CTS2* | *6* | *I* | | |
| | *RTS2* | *8* | *O* | | |
| | *GNDCOM2* | *10* | *P* | | |
| | *RXD1* | *12* | *I* | *Serial 1, EIA-232 (4.5.1)* | |
| | *TXD1* | *14* | *O* | | |
| | *CTS1* | *16* | *I* | | |
| | *RTS1* | *18* | *O* | | |
| | *GNDCOM1* | *20* | *P* | | |
| *17* | *COL0* | | *IO* | *PA0* | *ADSmartIO Keypad columns, digital I/Os or A/Ds (4.3)* |
| *19* | *COL1* | | *IO* | *PA1* | |
| *21* | *COL2* | | *IO* | *PA2* | |
| *23* | *COL3* | | *IO* | *PA3* | |
| *25* | *COL4* | | *IO* | *PA4* | |
| *27* | *COL5* | | *IO* | *PA5* | |
| *29* | *COL6* | | *IO* | *PA6* | |
| *31* | *COL7* | | *IO* | *PA7* | |
| | *RX422+* | *22* | *I* | *Serial 1, EIA-422/485 (4.5.1)* | |
| | *RX422-* | *24* | *I* | | |
| | *TX422+* | *26* | *O* | | |
| | *TX422-* | *28* | *O* | | |
| | *GNDRS422* | *30* | *P* | | |
| | *GPIO12* | *32* | *IO* | *PXA255 GPIOs (4.1.5, 4.6.1)* | |
| | *GPIO9* | *34* | *IO* | | |
| | *GPIO8* | *36* | *IO* | | |
| | *GPIO6* | *38* | *IO* | | |
| *33* | *VREF* | | *AO* | *ADSmartIO A/D reference voltage (4.3)* | |
| *35* | *VCC* | | *PO* | *5 V* | |
| *37* | *VDDX* | | *PO* | *3.3 V* | |
| *39* | *GND* | | *P* | *ground* | |
| | | *40* | *P* | | |

### 3.4.7 J8: Ethernet

Board Connector: RJ-45 socket, Amp 555167-1
Recommended mating cable: RJ-45 Ethernet cable, 8P4C (8 position, 4 contact)

Location on board: D6

This header provides the signals for connecting to a 10/100 Ethernet network.

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *TD+* | *AO* | *Transmit* |
| *2* | *TD-* | *AO* | |
| *3* | *RD+* | *AI* | *Receive* |
| *4* | *n/c* | | *n/c* |
| *5* | *n/c* | | |
| *6* | *RD-* | *AI* | *Receive* |
| *7* | *n/c* | | *n/c* |
| *8* | *n/c* | | |
| | *shield* | *P* | *Ground* |

### 3.4.8 J9: Manufacturing and Test Connector

Board Connector: 2x8 receptacle, 2mm spacing, Samtec SQT-108-01-L-D
Location on board: B5

This header is used during manufacturing to program the boot flash, onboard logic and ADSmartIO firmware. These JTAG and SPI signals are intended only for factory use and are not otherwise supported. In the table below, pins are grouped by function.

| Pin | Name | Pin | Type | Description |
|---|---|---|---|---|
| *1* | *TRST* | | | *JTAG* |
| | *TMS* | *2* | *I* | |
| | *TDI* | *4* | *I* | |
| *5* | *TCLK* | | | |
| | *TDO* | *8* | *O* | |
| *9* | *FWE* | | | |
| | *FRDY* | *10* | | |
| | *VDDX* | *6* | *PO* | *3.3 V* |
| *3* | *GND* | | *P* | *ground* |
| *7* | *GND* | | *P* | |
| | *VCC* | *12* | | *5 V* |
| *11* | *MISO* | | *O* | *ADSMARTIO SPI for in-system programming* |
| *13* | *SCLK* | | *I* | |
| *15* | *PRG* | | *I* | |
| | *MOSI* | *14* | *I* | |
| | *GND* | *16* | *P* | *ground* |

### 3.4.9 J10: Serial 3

Board Connector: 2x5 header, 0.100-in spacing, Amp 103308-1

Location on board: C1

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *DCD3* | *I* | *Data Carrier Detect* |
| *2* | *DSR3* | *I* | *Data Set Ready* |
| *3* | *RXD3* | *I* | *Receive data* |
| *4* | *RTS3* | *O* | *Ready To Send (or RTR Ready to Receive)* |
| *5* | *TXD3* | *O* | *Transmit data* |
| *6* | *CTS3* | *I* | *Clear To Send* |
| *7* | *DTR3* | *O* | *Data Terminal Ready* |
| *8* | *RIB3* | *I* | *Ring Indicator* |
| *9* | *GND_COM3* | *P* | *Serial 3 ground* |
| *10* | *n/c* | - | |

### 3.4.10 J11: PCMCIA

Board connector: AMP 535655-2
Optional ejector: AMP 146019-1, secured with #2-56 screws and 0.187-inch standoffs

Location on board: A3-D5

The 68-pin PCMCIA socket conforms to the PCMCIA standard, revision 2.1, for 5 V-tolerant Type II cards. The socket can also run at 3.3 V. The socket is normally de-energized; the operating system is responsible for turning on the socket when a card is inserted and turning it off when the card is removed.

Vpp (pins 18 and 52), which is 12 V in older PCMCIA implementations, is left unconnected in this implementation. Pin 69, pin 70 and the ejector are electrically connected to the same plane as the board mounting holes.

See section 6.2 for details about ejector hardware as a factory option See section 6.4.16 for electrical specifications.

### 3.4.11 J12: LCD Display (Hirose)

Board Connector: 31-pin Hirose DF9B-31P-1V
Location on board: B6, underside of board

This header can be used to directly connect to some active Sharp TFT displays and products that are compatible with them. The signals on this connector are a subset of the signals on J14. See section 3.4.11 for more detailed descriptions of the signals.

| Pin | Name (16bpp) | Pin | Type | Description |
|---|---|---|---|---|
| *1* | *GND* | | *O* | *ground* |
| | *PNL_PIXCLK* | *2* | *O* | *Pixel clock* |
| *3* | *PNL_HSYNC* | | *O* | *Horizontal sync* |
| | *PNL_VSYNC* | *4* | *O* | *Vertical sync* |
| *5* | *GND* | | *O* | *ground* |
| | *PNL_RED0* | *6* | *O* | *Red data* |
| *7* | *PNL_RED1* | | *O* | |
| | *PNL_RED2* | *8* | *O* | |
| *9* | *PNL_RED3* | | *O* | |
| | *PNL_RED4* | *10* | *O* | |
| *11* | *PNL_RED5* | | *O* | |
| | *GND* | *12* | *O* | *ground* |
| *13* | *PNL_GREEN0* | | *O* | *Green data* |
| | *PNL_GREEN1* | *14* | *O* | |
| *15* | *PNL_GREEN2* | | *O* | |
| | *PNL_GREEN3* | *16* | *O* | |
| *17* | *PNL_GREEN4* | | *O* | |
| | *PNL_GREEN5* | *18* | *O* | |
| *19* | *GND* | | *O* | *ground* |
| | *PNL_BLUE0* | *20* | *O* | *Blue data* |
| *21* | *PNL_BLUE1* | | *O* | |
| | *PNL_BLUE2* | *22* | *O* | |
| *23* | *PNL_BLUE3* | | *O* | |
| | *PNL_BLUE4* | *24* | *O* | |
| *25* | *PNL_BLUE5* | | *O* | |
| | *GND* | *26* | *O* | *ground* |
| *27* | *PNL_LBIAS* | | *O* | *Data enable* |
| | *PNL_PWR* | *28* | *O* | *Panel power (JP1)* |
| *29* | | | *O* | |
| | *PNL_RL* | *30* | *O* | *Horizontal Mode Select (JP2)* |
| *31* | *PNL_UD* | | *O* | *Vertical Mode Select (JP3)* |

### 3.4.12 J13: Backlight Inverter

Board Connector: 7-pin Molex 53261-0790
Location on board: A2-A3

See the "Brightness Control (Backlight)" paragraph in section 4.8.2 for additional details about these signals..

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *Vbacklight* | *PO* | *Power supply for backlight inverter from J5 pin 4* |
| *2* | | | |
| *3* | *GND* | *P* | *ground* |
| *4* | | | |
| *5* | *BacklightOn* | *OC* | *On/off control for backlight inverter (4.8.2)* |
| *6* | *BacklightPWM* | *AO* | *Brightness control for backlight inverter (4.8.2)* |
| *7* | *GND* | *P* | *ground* |

### 3.4.13 J14: LCD Display (34-pin)

Board Connector: 2x17 header, 0.1-inch spacing, TST-117-01-G-D
Recommended Mating Cable: Samtec HCSD Series

Location on board: A6-B6

The following table describes the signals on the LCD interface connector. Signal names shown are for TFT active matrix color LCDs at 16 bpp (bit-per-pixel). For other color depths and LCD technologies, consult the table in section 4.8.2. Signals from the XScale are buffered and EMI filtered before reaching J14. See section 4.8 for further details about displays.

| Pin | PXA255 Signal Name | Color Active TFT Display at 16bpp | |
|---|---|---|---|
| | | ADS Signal Name | Description |
| *1* | | *PNL_VEE* | *$V_{EE}$ (contrast) (VR1, J19, 4.8.2)* |
| *2* | | *GND* | *ground* |
| *3* | *PCLK* | *PNL_PIXCLK* | *Pixel Clock* |
| *4* | *LCLK* | *PNL_HSYNC* | *Horizontal Sync.* |
| *5* | *FCLK* | *PNL_VSYNC* | *Vertical Sync.* |
| *6* | | *GND* | *ground* |
| *7* | *LDD15* | *PNL_RED0* | *Red data* |
| *8* | *LDD11* | *PNL_RED1* | |
| *9* | *LDD12* | *PNL_RED2* | |
| *10* | *LDD13* | *PNL_RED3* | |
| *11* | *LDD14* | *PNL_RED4* | |
| *12* | *LDD15* | *PNL_RED5* | |
| *13* | | *GND* | *ground* |
| *14* | *LDD5* | *PNL_GREEN0* | *Green data* |
| *15* | *LDD6* | *PNL_GREEN1* | |
| *16* | *LDD7* | *PNL_GREEN2* | |
| *17* | *LDD8* | *PNL_GREEN3* | |
| *18* | *LDD9* | *PNL_GREEN4* | |
| *19* | *LDD10* | *PNL_GREEN5* | |
| *20* | | *GND* | *ground* |

| | | | |
|---|---|---|---|
| *21* | *LDD4* | *PNL_BLUE0* | *Blue data* |
| *22* | *LDD0* | *PNL_BLUE1* | |
| *23* | *LDD1* | *PNL_BLUE2* | |
| *24* | *LDD2* | *PNL_BLUE3* | |
| *25* | *LDD3* | *PNL_BLUE4* | |
| *26* | *LDD4* | *PNL_BLUE5* | |
| *27* | | *GND* | *ground* |
| *28* | *LBIAS* | *PNL_LBIAS* | *Data enable* |
| *29* | | *PNL_PWR* | *Vcc (5 V) or 3.3 V (JP1)* |
| *30* | | | |
| *31* | | *PNL_RL* | *Horizontal Mode Select (JP2)* |
| *32* | | *PNL_UD* | *Vertical Mode Select (JP3)* |
| *33* | *PANEL_ENABLE* | *PNL_ENA* | *Panel enable signal* |
| *34* | | *VCON* | *Contrast control (VR2, 4.8.2)* |

### 3.4.14 J17: Microphone

Board Connector: 1x2 header, 0.1 inch spacing, Molex 22-23-2021
Location on board: A3

This connector allows for connection to an electret microphone. See section 4.4.1 for details.

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *MICGND* | *AP* | *Microphone input (-)* |
| *2* | *MICSIG* | *AI* | *Microphone input (+)* |

### 3.4.15 J18: CAN Bus

Board Connector: 1x2 header, 0.1 inch spacing, Molex 22-23-2021
Location on board: D7

The signals for CAN bus 1 are also available on header J15.

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *CANHIGH* | *IO* | *CAN bus1 (4.5.6)* |
| *2* | *CANLOW* | *IO* | |

### 3.4.16 J21: RTC Battery Connector (factory option)

Board Connector: 1x2 header, 0.1 inch spacing, Molex 22-23-2021
Location on board: A1

For volume production orders, this header can replace RTC battery. See section 4.2 for details.

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *RTC_VBAT* | *PI* | *RTC battery (+)* |
| *2* | *GND* | *P* | *RTC battery (-)* |

### 3.4.17 J23: Remote IrDA Connector (optional)

Board Connector: 8-pin header, 1.25mm, keyed, Molex #53261-0890
Recommended Mating Connector: Molex 51021-0800 or
Quadrangle Products kit #RT51021-0800-18

Location on board: D1-D2

Header J23 can replace IrDA transceiver U1, allowing off-board placement of an IrDA transceiver. See section 4.5.1 for details.

| Pin | Name | Type | Description | TFDU6101E (U1) pin |
|---|---|---|---|---|
| *1* | *IR_ANODE* | *PO* | *IrDA transmitter power (5 V)* | *1* |
| *2* | *n/c* | | *n/c* | |
| *3* | *IR_TXD* | *O* | *IrDA transmit data* | *3* |
| *4* | *IF_RXD* | *I* | *IrDA receive data* | *4* |
| *5* | */IRDAON* | *O* | *IrDA transceiver control signal* | *5* |
| *6* | *IR_VCC* | *PO* | *IrDA receiver power (5 V)* | *6* |
| *7* | *n/c* | | *n/c* | |
| *8* | *GND* | *P* | *ground* | *8* |

### 3.4.18 J516: Audio Output

The GCX can drive either a single speaker or stereo headphones. The speaker output is standard.

#### *Speaker Output*

Board Connector: 1x2 header, 0.1 inch spacing, Molex 22-23-2021

This header can be connected directly to a speaker. See section 4.4.2 for details.

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *SPK-* | *AO* | *Mono speaker output (4.4.2)* |
| *2* | *SPK+* | *AO* | |

#### *Stereo Headphones (factory option)*

Board Connector: 1x3 header, 0.1 inch spacing, Molex 22-23-2031Location on board: A3

This header supplies output signals suitable for driving stereo headphones. See section 4.4.2 for further details.

| Pin | Name | Type | Description |
|---|---|---|---|
| *1* | *SPK-* | *AO* | *Common* |
| *2* | *SPK_R* | *AO* | *Right channel* |
| *3* | *SPK_L* | *AO* | *Left channel* |

# 4 Feature Reference

This chapter provides details about the architecture and many features of the GCX, and how they can fit together to create a system that meets your application needs.

## *4.1 System Architecture*

### 4.1.1 Boot Code

The GCX uses the first block of onboard flash to store the boot code. At the factory, boot code is loaded using the JTAG interface (J9). Most ADS GCX boot loaders are field-upgradeable using a PCMCIA flash card.

The GCX can be used in security-conscious applications where a removable boot ROM is required. The boot ROM resides in socket U22 (location D1-D2 on the board). See section 6.2 for details about this and other volume production options.

### 4.1.2 Synchronous DRAM

One bank of synchronous DRAM (SDRAM) can be populated for a system total of 16, 32, 64 or 128 MiB of RAM[6]. The data bus width is 32 bit.

The memory clock speed is one half the CPU core clock speed. Typical memory bus operation is at 99.5 MHz.

The self-refreshed RAM consumes most of the system sleep current. Sleep current increases in direct proportion to the amount of RAM installed.

### 4.1.3 Non-Volatile Memory

There are several ways to store data on the GCX that will survive a power failure. Some devices can only be accessed through operating system drivers, and not all are available for application data storage.

#### *Flash Memory*

Flash memory is the primary site for non-volatile data storage. The GCX includes a bank of flash memory for non-volatile data storage. The board supports 8, 16 or 32 MiB of installed flash. The data bus width is 32 bit.

ADS systems store the operating system, applications and system configuration settings in the onboard flash. Most operating systems configure a portion of the flash as a flash disk, which acts like a hard disk drive.

#### *ADSmartIO EEPROM*

The ADSmartIO controller includes 256 bytes or more of EEPROM storage. ADS reserves a portion of this memory for future use. Drivers may not be available for all operating systems.

#### *CompactFlash and PCMCIA/ATA Cards*

CF and ATA cards provide removable storage in a wide variety of capacities. These cards can be cost-effective means to expand system storage capacity for user applications that provide access to the PCMCIA slot. You may use CompactFlash cards on the GCX when they are in inserted into a PCMCIA adapter sleeve.

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[6] 128 MiB SDRAM was not yet commercially available as of April 2003.

### *RTC NVRAM*

The real-time clock chip includes 56 bytes of non-volatile RAM. The RAM is maintained as long as main or backup power is provided to the chip. Built-in drivers may not be available to access this feature, but the RAM can be accessed using the $I^2C$ driver. Contact ADS Sales if your application requires this feature.

## 4.1.4 Interrupts

The GCX includes several sources for external interrupts. The following table summarizes these sources and the devices to which they are connected.

| Interrupt Signal | Pin | IRQ Handler |
|---|---|---|
| *XScale GPIOs* [7] | *J7* | *XScale CPU* |
| */EXT_IRQ* | *J2.24* | *Controller CPLD* |
| *CARDAIRQ* | *J11.16* | *Controller CPLD* |

Your operating system will determine which interrupt sources are supported.

## 4.1.5 PXA255 GPIO Cross-Reference

The following table describes how the GCX utilizes the XScale GPIO lines (*GPn*). They are offered for reference purposes only. Most operating systems make this information transparent to developers.

| *GPIO* | Signal Name | Type | Function (connector, section) |
|---|---|---|---|
| *0* | *WAKE_UP* | *I* | *Debounced RqOnOff (3.4.1, 6.4.3)* |
| *1* | *IRQ_CPLD* | *I* | *CPLD interrupt* |
| *2* | *CTS2* | *I* | *Serial 2 CTS (4.5.1)* |
| *3* | */USB_DET* | *I* | *USB function port, detect connection* |
| *4* | *TS_IRQ* | *I* | *Touch panel interrupt* |
| *5* | *USB_RECONN* | *O* | *USB function port, disconnect/reconnect* |
| *6* | *GPIO6* | *IO* | *Digital IO (J7, 3.4.6)* |
| *7* | */CARDAVS1* | *I* | *PCMCIA Voltage Sense 1* |
| *8* | *GPIO8* | *IO* | *Digital IO (J7, 3.4.6)* |
| *9* | *GPIO9* | *IO* | *Digital IO (J7, 3.4.6)* |
| *10* | */CARDAVS2* | *I* | *PCMCIA Voltage Sense 2* |
| *11* | *CLK3.68MHZ* | *O* | *CPLD clock* |
| *12* | *GPIO12* | *IO* | *Digital IO (J7, 3.4.6)* |
| *13* | *PANEL_ENABLE* | *O* | *LCD display power enable* |
| *14* | *IRQ_UCB* | *I* | *UCB1400 interrupt* |
| *15* | */CS1* | *O* | *Asynchronous flash chip select* |
| *16* | *PXA_VEE_PWM* | *O* | *PWM0 control of Vee voltage* |
| *17* | *PXA_BL_PWM* | *O* | *PWM1 backlight brightness control* |
| *18* | *RDY* | *O* | *Variable latency access CPU ready* |
| *19* | *LED1* | *O* | *Onboard LED outputs* |
| *20* | *LED0* | *O* | |
| *21* | *LED2* | *O* | |
| *22* | *ADCSYNC* | | *UCB1400 A/D synchronization* |
| *23* | *SCLK-C* | *O* | *SPI to touch panel controller* |
| *24* | *SFRM-C* | *O* | |

[7] Important! The PXA255 has restrictive constraints concerning timing of successive interrupts. While you may configure one or more XScale GPIOs as interrupt sources, it's possible to create a condition under which interrupts in rapid succession can cause the processor to lock up.

| *GPIO* | Signal Name | Type | Function (connector, section) |
|---|---|---|---|
| *25* | *TXD-C* | *O* | |
| *26* | *RXD-C* | *I* | |
| *27* | */RESETAVR* | *O* | *Reset ADSmartIO controller* |
| *28* | *BITCLK* | | *AC '97 Codec* |
| *29* | *SDATA_IN* | | |
| *30* | *SDATA_OUT* | | |
| *31* | *SYNC* | | |
| *32* | *RTS2* | *O* | *Serial 2 RTS (4.5.1)* |
| *33* | *n/c* | | *unused* |
| *34* | *RXD3* | *I* | *Serial 3 Full-featured UART (4.5.1)* |
| *35* | *CTS3* | *I* | |
| *36* | *DCD3* | *I* | |
| *37* | *DSR3* | *I* | |
| *38* | *RIB3* | *I* | |
| *39* | *TXD3* | *O* | |
| *40* | *DTR3* | *O* | |
| *41* | *RTS3* | *O* | |
| *42* | *RXD1* | *I* | *Serial 1 Bluetooth UART 4.5.1)* |
| *43* | *TXD1* | *O* | |
| *44* | *CTS1* | *I* | |
| *45* | *RTS1* | *O* | |
| *46* | *RXD2* | *I* | *Serial 2/Infrared (4.5.1)* |
| *47* | *TXD2* | *O* | |
| *48* | */POE* | | *PCMCIA/CF Card interface* |
| *49* | */PWE* | | |
| *50* | */PIOR* | | |
| *51* | */PIOW* | | |
| *52* | */PCE1* | | |
| *53* | */PCE2* | | |
| *54* | *PSKTSEL* | | |
| *55* | */PREG* | | |
| *56* | */PWAIT* | | |
| *57* | */IOIS16* | | |
| *58* | *LDD0* | *O* | *LCD display (4.8)* |
| *59* | *LDD1* | *O* | |
| *60* | *LDD2* | *O* | |
| *61* | *LDD3* | *O* | |
| *62* | *LDD4* | *O* | |
| *63* | *LDD5* | *O* | |
| *64* | *LDD6* | *O* | |
| *65* | *LDD7* | *O* | |
| *66* | *LDD8* | *O* | |
| *67* | *LDD9* | *O* | |
| *68* | *LDD10* | *O* | |
| *69* | *LDD11* | *O* | |
| *70* | *LDD12* | *O* | |
| *71* | *LDD13* | *O* | |
| *72* | *LDD14* | *O* | |
| *73* | *LDD15* | *O* | |
| *74* | *VSYNC/FCLK* | *O* | *LCD control signals (4.8)* |
| *75* | *HSYNC/LCLK* | *O* | |

| *GPIO* | Signal Name | Type | Function (connector, section) |
|---|---|---|---|
| *76* | *PCLK* | *O* | |
| *77* | *LBIAS* | *O* | |
| *78* | */CS_CPLD* | *O* | *Controller CPLD chip select* |
| *79* | *n/c* | *O* | *unused* |
| *80* | */CS_ETH* | *O* | *Ethernet chip select* |

## 4.2 Real-Time Clock (RTC)

The GCX uses the DS1307 real-time clock chip to maintain the system date and time when the system is powered down.

The operating system typically reads the RTC on boot and wakeup, and sets the RTC when the system time or date is changed. The system communicates with the RTC on the $I^2C$ bus (section 4.5.7).

The RTC is powered by a long-life 3 V battery. For volume production orders, the battery can be removed from the GCX and the RTC can be powered via the power input on J21. See section 6.4.1 for electrical specifications.

## 4.3 ADSmartIO

ADSmartIO™ is a RISC microcontroller on the GCX that is programmed with ADS firmware. This device provides additional I/O functionality for specialized tasks. Your application software can configure the standard ADSmartIO for a variety of functions, such as digital I/O, PWM, A/D, $I^2C$, keypad scan and PS/2 keyboard operation.

### 4.3.1 Overview

The ADSmartIO controller has four, eight-pin I/O ports named PA, PB, PC and PD. Some of these ports' pins are used internally, while others are available for user applications. See the signal cross-reference in section 4.3.6 for details.

Generally, ADSmartIO ports are referenced by port and pin number (e.g. PA2), but I/O signals may go by several names based on its functionality. See the connector pinouts to cross-reference ADSmartIO signal names.

Electrical specifications for the ADSmartIO are listed in section 6.4.3. The *ADSmartIO Programmer's Reference* (ADS document 110110-4004) gives information about how to use the ADSmartIO features.

### 4.3.2 ADSmartIO Features

The following are some of the functions that the ADSmartIO can perform. The functions actually implemented depend on the firmware loaded on your system:

- General purpose digital I/O and A/D
- Keypad scan (section 4.3.5)
- PS/2 keyboard input
- Wakeup via RQONOFF signal (section 5.2.2)
- Reset CPU

### 4.3.3 Digital I/Os

All available ports on the ADSmartIO controller can be individually configured as inputs or outputs. If you write a "1" to an I/O port when it is configured as an input, it enables a pull-up resistor. Electrical specifications are listed in section 6.4.7. Other digital I/Os are listed in section 4.6.1.

### 4.3.4 Analog Inputs (A/D)

Each of the Port A I/Os (PA0-PA7) includes an analog-to-digital (A/D) converter. The converters give full-scale readings when the voltage at the pin is equal to voltage reference Vref (e.g. V=Vref•reading/1023). Not all ports are available for external A/D use; see section 4.3.6 for port assignments. The A/D inputs on the GCX go through voltage dividers before reaching the pins. See the electrical specifications listed in section 6.4.7 for details.

### 4.3.5 Keypad Scan

The ADSmartIO can scan a matrix keypad up to four by five keys in size. Matrix keypads are simpler and cost less than full keyboards and can be easily customized for your application. You can also create a keypad matrix from a collection of normally-open switches.

When configured to scan a keypad, the ADSmartIO configures the ROWn lines as inputs with software pull-ups enabled and configures the COLn lines as outputs set to "1"(high). For the scan, the keypad scanner sets successive COLn outputs to "0"(low), then looks for a "0" on one of the ROWn inputs. The scanner re-reads the pressed key after a delay to debounce the key press.

Unused row and column lines can be used for general purpose I/O or A/D.

The following diagram illustrates how to connect a 3x3 keypad matrix. The pull-ups are the software-activated internal resistors of the ADSmartIO, while the series resistors are part of the GCX.

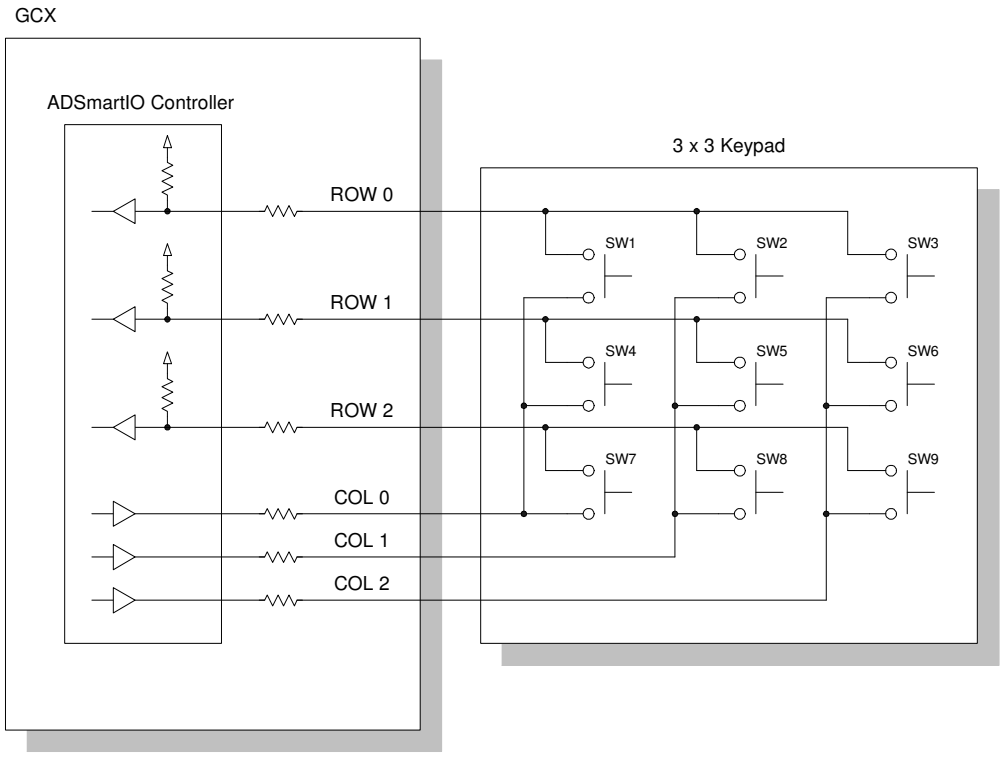



**Figure 3 Using a 3x3 Keypad with ADSmartIO**

### 4.3.6 ADSmartIO Signal Cross-Reference

The ADSmartIO microcontroller serves many functions in the GCX. The following table illustrates how the microcontroller ports are utilized for ADSmartIO functionality on the GCX.

Entries in parentheses indicate indirect connections to the listed pin (e.g. through voltage dividers or additional circuits). Signals with conventional protection circuits are considered directly connected. I=input, O=output.

| Port | | Type | Function | |
|---|---|---|---|---|
| *PA0* | *J7.17* | *IO* | *Keypad columns, digital I/O or A/D* | |
| *PA1* | *J7.19* | *IO* | | |
| *PA2* | *J7.21* | *IO* | | |
| *PA3* | *J7.23* | *IO* | | |
| *PA4* | *J7.25* | *IO* | | |
| *PA5* | *J7.27* | *IO* | | |
| *PA6* | *J7.29* | *IO* | | |
| *PA7* | *J7.31* | *IO* | | |
| *PB0* | - | | *unused* | |
| *PB1* | - | | | |
| *PB2* | *J2.16* | *IO* | *SMTIO2 digital I/O* | |
| *PB3* | *J2.18* | *IO* | *SMTIO3 digital I/O* | |
| *PB4* | - | | *FRM* | *SPI communication with PXA255* |
| *PB5* | - | | *RX (MOSI)* | |
| *PB6* | - | | *TX (MISO)* | |
| *PB7* | - | | *SCLK* | |
| *PC0* | *J7.15* | *IO* | *Keypad rows or digital I/O* | |
| *PC1* | *J7.13* | *IO* | | |
| *PC2* | *J7.11* | *IO* | | |
| *PC3* | *J7.9* | *IO* | | |
| *PC4* | *J7.7* | *IO* | | |
| *PC5* | *J7.5* | *IO* | | |
| *PC6* | *J7.3* | *IO* | | |
| *PC7* | *J7.1* | *IO* | | |
| *PD0* | *J2.20* | *IO* | *SMTIO4 digital I/O* | |
| *PD1* | *J2.22* | *IO* | *SMTIO5 digital I/O* | |
| *PD2* | *J6.5* | *IO* | *PS/2 Clock* | |
| *PD3* | - | | *IRQSSP* | |
| *PD4* | - | | *unused* | |
| *PD5* | - | | | |
| *PD6* | *J6.1* | *IO* | *PS/2 Data* | |
| *PD7* | - | | *unused* | |

## 4.4 Audio

The GCX uses the UCB 1400, an AC '97 codec, for stereo audio input and output. Electrical specifications and architecture of the audio system are listed in section 6.4.13.

### 4.4.1 Microphone Input

The GCX supports the connection of an electret microphone to the MICSIG and MICGND inputs on J17. The audio signal runs through a DC blocking capacitor before reaching the codec. The codec includes a software-controlled amplifier that can control input gain.

When connecting external electret microphones to the GCX, use the MICGND analog ground for best signal-to-noise ratio. The GCX includes pull-ups to power electrets microphones. Section 6.4.13 includes electrical specifications and a block diagram of the audio input system.

### 4.4.2 Audio Outputs: Speakers and Headphones

The GCX supplies a single-channel, differential-drive audio output suitable for driving a bridge-tied speaker. The GCX can also drive stereo headphones (single-ended-drive speakers) as a factory option. Audio outputs are on header J516. Section 6.4.13 includes electrical specifications and a block diagram of the audio output system.

#### *Connecting Speakers*

When using the GCX to drive speakers, short the HP_IN signal to ground. This places the output amplifier in differential mode. Connect speakers to the SPKR_L and SPKR_R outputs on J516.

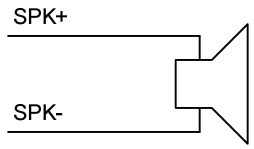



**Figure 4 Connecting a Speaker**

#### *Connecting Headphones (Factory Option)*

As a factory option, the GCX can drive stereo headphones. When this option is installed, header J516 is a three-pin connector.

Standard headphones use a plug wired as shown below. Three rings on the plug provide right and left channels and a common return. Mono headphones do not include the center ring. The mating headphone jacks include spring contacts to make an electrical connection with the headphone and to mechanically hold the plug in place

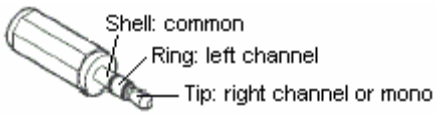



**Figure 5 Typical Headphone Jack**

The following diagram illustrates one way to make use of the headphone output. The user plugs stereo standard headphones into a 1/8-inch socket, which is cabled to GCX header J516.

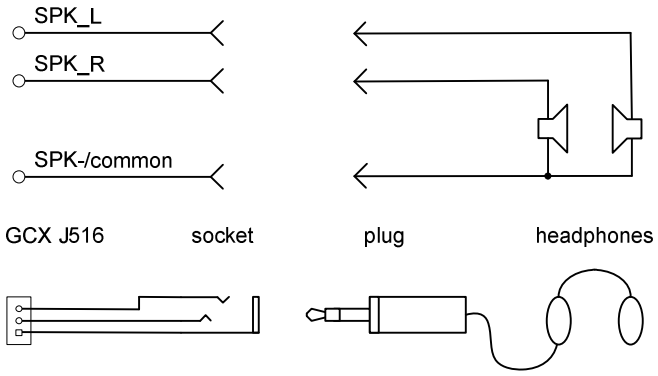



**Figure 6 Connecting Stereo Headphones (factory option)**

## 4.5 Data Communications

The GCX has several built-in channels for communication with peripheral and peer devices. These include EIA/TIA-232, -422 and -485; J1708; logic-level serial; IrDA; USB client port; Ethernet; CAN bus and $I^2C$.

### 4.5.1 Serial Ports

The GCX has three serial ports driven by the XScale processor. These asynchronous serial ports can be configured in the field for a variety of operational modes, as shown below. A few additional options are available to volume production orders (see section 6.2 for details).

| Port | # signals | Headers | Standard | Production options |
|---|---|---|---|---|
| 1 | 5 | J7, JP8-11, JP14-15 | EIA/TIA-232, EIA/TIA-422/485 | J1708, 3.3 V logic |
| 2 | 5 | J7, JP7 | EIA/TIA-232, IrDA, 3.3 V logic | header J23 for IrDA |
| 3 | 9 | J10, JP16-17 | EIA/TIA-232 | 3.3 V logic |

#### *XScale UART*

The XScale processor supplies three standard serial ports. The "Bluetooth UART" is Serial 1 on the GCX; the "IrDA UART" is GCX Serial 2; and the "Full-featured" UART" is GCX Serial 3.

The Serial 2 CTS and RTS serial handshaking signals are XScale GPIO lines that must be controlled by the software drivers when Serial 2 is operated as EIA/TIA-232 or 3.3 V logic.

Ports that are configured for 3.3 V logic operation connect directly to the XScale and should be treated electrically as GPIOs. See section 6.4.14 for GPIO electrical specifications and 6.4.9 for serial port specifications.

### 4.5.2 IrDA

The GCX supports IrDA (the Infrared Data Associations wireless communication standard) through a combination of hardware and software.

IrDA hardware consists of infrared transceiver U1, an enable line and the power circuitry needed to supply the bursts of power that drive the infrared LEDs. The software consists of a driver that

enables the transceiver with the IrDAOn signal and sets up the PXA255 to shorten the Serial 2 data bit pulses to match the IrDA standard.

The IrDA transceiver is normally mounted on the board (3.2.4), but for volume production orders, header J23 can replace the transceiver for cabling to another location. Electrical specifications are listed in section 6.4.9.

### 4.5.3 Synchronous Serial

The GCX acts as master on a number of internal and external synchronous serial buses. The following table describes how the buses are used on standard production GCX systems:

| SSP Bus | Use on GCX |
|---|---|
| *PXA255 NSSP* | *External device (header J2) or five-wire touch panel controller* |
| *PXA255 SSP* | *ADSmartIO controller* |

#### *Overview of Synchronous Serial Ports*

Several synchronous serial port standards share the same simple architecture: a clock line, transmit and receive lines, ground and one or more device selects. Each device on the bus requires its own select line. Buses may be full or half duplex, clocking data one or both directions at the same time, respectively. The standard selected defines which devices are bus masters and which are slaves.

To clarify direction of the data signals, the SPI bus master transmit line (STXD) is also known as MOSI (Master Out, Slave In), while its receive line is known as MISO (Master In, Slave Out). The Slave Select (SS) signal, which enables the slave device's transmitter, is also known as SFRM2 on the BitsyX.

#### *SSP on the GCX*

The GCX has two SSP channels, both driven by the XScale PXA255. The SSP port communicates with the ADSmartIO controller. The signals for that port are brought out to header J9 for ADSmartIO in-system programming at the factory, but the port is not otherwise supported for application use.

The second channel is the PXA255 NSSP port. The GCX offers the NSSP port on header J2 for communication with an off-board device. As a factory option, the NSSP port may instead be used an SPI bus master to communicate with a five-wire touch panel controller.

The PXA255 NSSP port can be software-configured to make use of one or more of the following features:

- Data widths from four to sixteen bits
- 16-entry transmit and receive FIFOs with burst-mode data transfers to/from RAM
- Adjustable FIFO threshold interrupts
- Bit clock speeds up to 1.84 MHz (up to 13Mbps with slave clock input and DMA)
- Support for Motorola's SPI, National Semiconductor's Microwire and Texas Instruments' SSP (Synchronous Serial Protocol).

Electrical specifications for the NSSP port are listed in section 6.4.14. Consult the operating system references for details about how to use the NSSP port for external devices.

### 4.5.4 USB

The GCX includes signals for a USB 1.1 Function port. The USB Function signals are on header J2 and are connected to the PXA255.

To create a USB connection, you must wire a standard USB socket as described in the following sections. For each type of connector, pin numbering is as follows:

| Pin | USB signal |
|---|---|
| *1* | *USB_PWR* |
| *2* | *USB -* |
| *3* | *USB +* |
| *4* | *GND* |

#### *USB Function Port*


The GCX includes a USB Function (or "Client") port. This interface allows the GCX to appear as a client device to USB Host devices such as desktop and laptop computers.

The USB Function signals are available on connector J2 (section 3.4.2). Connect these signals to a USB client Type B socket (mating face shown at left). The USB standard also permits directly wiring the USB signals to the host or to a host connector (e.g. USB mouse).

The PXA255 supports the full USB connection speed (12 Mbit/s). It indicates this to the host device with a 1.5 kΩ pull-up on the USB+ signal.

USB_VCC is power supplied from the host computer. Since the GCX is self-powered (not powered by the USB host), USB_VCC is not needed as a power input. However, USB_VCC tells the GCX when a USB cable is connected, so include it when connecting the USB signals to the GCX.

The GCX includes the capability to simulate a Function port cable disconnection. This feature can be used to force the host to re-enumerate the GCX (e.g. after wakeup).

### 4.5.5 Ethernet

The GCX includes a 10/100 BT Ethernet controller with an RJ-45 socket (J8).

Ethernet details and electrical specifications are listed in section 6.4.11.

### 4.5.6 CAN Bus

CAN bus (Controller Area Network) is a protocol developed for the automotive industry that is increasingly being used in industrial control and automation applications. The GCX includes a CAN controller suitable for connection to a wide range of CAN networks.

The CAN signals are available on header J18. Details and electrical specifications are listed in section 6.4.12.

## 4.5.7 I²C Bus Master

I²C (Inter-IC) Bus is a multi-master, "two-wire" synchronous serial bus developed by Philips for communications between integrated circuits (ICs). The bus master addresses devices using the data line and provides a synchronous clock for reading and writing devices. Client devices respond only when queried by the master device. Philips has developed many I²C devices, but other organizations (e.g. Maxim) have adopted I²C as a convenient means for addressing peripherals in a system.

### *I²C on the GCX*

The GCX uses the XScale I²C interface to communicate with the real-time clock (section 4.2) and the CPU core voltage controller. Applications can also use I²C to communicate with external peripherals.

The following diagram illustrates the I²C architecture on GCX. Parts are shown populated as they are found on standard production systems.

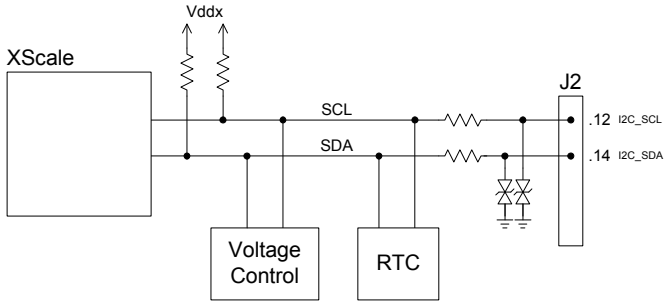



**Figure 7 The GCX I²C Bus**The XScale controls all I²C peripherals on the GCX. Its I²C signals are routed to header J2 via low-impedance resistors. Specifications are listed in section 6.4.17.

### *I²C Device Addresses*

The following are the bus addresses of the I²C devices included on standard GCX systems:

| | |
|---|---|
| 0x20 | Voltage controller |
| 0x68 | Real-time clock |

Select external I²C devices with addresses that will not conflict with the onboard devices. Onboard devices are typically controlled by operating system drivers and should not be addressed directly.

### *Managing Independent I²C Buses*

I²C was designed for use in closely integrated systems. However, some embedded applications may require that components on the GCX or external I²C bus be turned off to conserve power. In such cases, your system may need to use transistors to isolate the buses.

The following diagram illustrates how to isolate the GCX from an external I²C bus when the GCX powered off (external I²C bus remains powered). Choose the control signal and type and direction of transistor based on the requirements of your application.

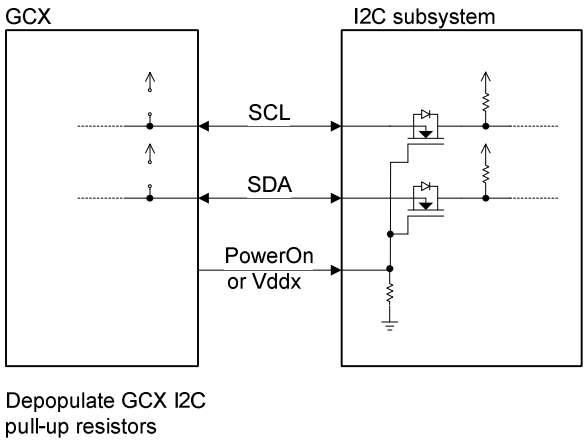



**Figure 8 Isolating GCX from an Active I²C Bus When Powered Off**

This isolation is not needed if the I²C subsystem turns off with the GCX, or when the GCX is in sleep mode.

It is also possible to use a variation of this circuit to bridge I²C buses of different voltages. See the Philips I²C standard for details.

## *4.6 Discrete Signals*

This section summarizes the discrete signals on the GCX that can be used for measurement or control.

### 4.6.1 Digital IOs

The GCX has a number of subsystems that provide digital control lines for application use. These are often referred to as digital I/Os (inputs/outputs), as most can be software-configured as inputs or outputs.

The following table summarizes the digital I/Os available on the GCX. The Ref column indicates reference sections for their use.

| Type | # lines | Source | Header | Ref | Details |
|---|---|---|---|---|---|
| 3.3V logic, I/O | 4 | PXA255 | J7 | 6.4.14 | low current |
| 3.3V logic, I/O | 10 | UCB1400 | J2 | 6.4.5 | low current |
| 3.3V logic, I/O | 4 | ADSmartIO | J2 | 4.3.3, 6.4.7 | software-configurable pull-ups available |
| | 16 | | J7 | | |

### 4.6.2 Analog Inputs

The GCX has two subsystems that perform analog-to-digital (A/D) conversions. These A/D inputs are typically used for low-speed, uncalibrated applications (e.g. user input, ballpark voltage measurement, etc) as the noise margins on the GCX A/Ds are not suited for most instrumentation applications. For precision A/D readings, consider taking averages of several readings, performing two-point calibrations or using an external A/D converter (e.g. over SSP).

The following table summarizes the A/D inputs available on the GCX. The Ref column indicates reference sections for their use.

| Range | # lines | Rin | Source | Header | Ref | Details |
|---|---|---|---|---|---|---|
| 0–10 V | 4 | 1.3 kΩ | UCB1400 | J2 | 6.4.5 | |
| 0–10.8 V | up to 8 | 43.2 kΩ | ADSmartIO | J7 | 4.3.4, 6.4.7 | PA channels |

### 4.6.3 Analog Outputs (PWM)

The GCX has two analog outputs. These are pulse-width modulated (PWM), low-pass filtered digital I/Os used to control LCD backlighting and contrast (section 4.8.2).

## *4.7 Touch Panel*

The standard GCX supports four-wire analog resistive touch panels, while five-wire panels are an option for volume production orders. Connect the touch panel to the inputs on connector J4. The touch panel controller can wake the system from sleep (section 5.2.3) Electrical details are listed in section 6.4.5.

## 4.8 Display Controller

The GCX uses XScale display controller to drive active and passive liquid crystal displays (LCDs). This section describes both the controller architecture, display signals and backlight and contrast control.

### 4.8.1 The XScale Display Controller

The XScale controller uses system memory for the display frame buffer. It can drive VGA (640x480) and SVGA (800x600) displays easily. Larger displays will work with the XScale, with some constraints imposed by the controller architecture. The ADS Support Forums provide details about the design tradeoffs that are required to support larger displays.[8]

Key features of the XScale controller include

- Frame buffer is in system DRAM
- Dual 16 x 8-byte display data FIFOs

### 4.8.2 Using the LCD Display Signals

This section describes the features of the GCX used to control LCD displays. LCD display signals are found on headers J12 and J14.

#### *Panel Voltages*

The GCX supplies 3.3 V or 5 V power to the LCD display. Select this voltage with JP1 (3.3.1). Please observe the cautions listed with the JP1 settings.

Additional voltages for backlight and contrast are described in sections below.

#### *LCD Signals*

The LCD signals are driven by the XScale controller. The signals are named using the XScale conventions (LDDn). *LDD0* through *LDD15*—as well as the pixel clock, vertical sync and horizontal sync—are all buffered at a factory-set voltage. See section 6.4.4 for full specifications.

The *PNL_RL* and *PNL_UD* signals are for active (TFT) displays that support changing the scan direction. This feature allows the display to be flipped right-to-left (*RL*) or up-and-down (*UD*) by changing the voltage on these signals. See section 6.4.4 for full specifications.

[8] At the time of writing, additional details about the XScale display controller are posted at http://www.applieddata.net/forums/topic.asp?topic_id=990

## Creating LCD Display Cables

ADS has designed cables for a wide variety of displays. See the list of supported displays on the ADS support forums. Cable drawings for supported displays are available on request.

While ADS does not provide support to customers to create their own cables, designers with LCD display experience may be able to design their own. For those that do so, a key point to keep in mind is that the PXA255 LCD interface maps its display controller pins differently based on LCD technology and color palette size. The following table illustrates how they are mapped for some of the more common technologies. Consult the PXA255 User's Manual for more information.

| XScale [9] Signal Name | Color Active | | Color Passive | | | Mono Passive | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 16-bit | 12-bit | Dual | | Single | Dual | | Single DPD[10] | Single |
| LDD0 | B0 | B0 | DU0 | top | D0 | DU0 | top | D0 | D0 |
| LDD1 | B1 | B1 | DU1 | | D1 | DU1 | | D1 | D1 |
| LDD2 | B2 | B2 | DU2 | | D2 | DU2 | | D2 | D2 |
| LDD3 | B3 | B3 | DU3 | | D3 | DU3 | | D3 | D3 |
| LDD4 | B4 | | DU4 | | D4 | DL0 | bottom | D4 | not used |
| LDD5 | G0 | G0 | DU5 | | D5 | DL1 | | D5 | |
| LDD6 | G1 | G1 | DU6 | | D6 | DL2 | | D6 | |
| LDD7 | G2 | G2 | DU7 | | D7 | DL3 | | D7 | |
| LDD8 | G3 | G3 | DL0 | bottom | not used | | | | |
| LDD9 | G4 | | DL1 | | | | | | |
| LDD10 | G5 | | DL2 | | | | | | |
| LDD11 | R0 | R0 | DL3 | | | | | | |
| LDD12 | R1 | R1 | DL4 | | | | | | |
| LDD13 | R2 | R2 | DL5 | | | | | | |
| LDD14 | R3 | R3 | DL6 | | | | | | |
| LDD15 | R4 | | DL7 | | | | | | |
| PCLK | PCLK | | PCLK | | | | | | |
| LCLK | HSYNC | | LCLK | | | | | | |
| FCLK | VSYNC | | FCLK | | | | | | |
| LBIAS | DE | | LBIAS | | | | | | |

## Brightness Control (Backlight)

Most LCD displays include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Some LCDs, such as passive transflective displays, can be viewed in daylight without backlighting. Smaller displays sometimes use LED backlighting.

CCFL panel backlights are driven by backlight inverters. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. Fortunately, most backlight inverters include control signals to dim and turn off the backlight.

The GCX supplies two signals for backlight control: BacklightPWM and /BacklightOn. The signals are found on header J13. BacklightPWM is a filtered PWM signal from the PXA255 that supplies an analog output voltage to control the intensity of the backlight. The /BacklightOn

[9] Intel. PXA255 Processor: Developer's Manual. Order number 278693-001, March 2003. pp. 7-20 to 7-22.

[10] Double pixel data (DPD) mode = 1

signal is an open-collector output to turn the backlight on and off. See section 6.4.4 for electrical specifications.

#### *Contrast Control (Vee and Vcon)*

Most passive panels require a positive or negative voltage in the range of 15-30 volts to bias the passive LCD display. The GCX includes the Vee and Vcon factory option to address this need.

The GCX Vee generator generates positive or negative voltages up to thirty volts. Some factory configuration is usually needed to match the requirements of specific displays.

The Vcon output is a low-voltage, PWM-controlled analog output that can control contrast of displays that have their own onboard Vee generator.

Electrical specifications for Vee and Vcon are listed in section 6.4.4.

### 4.8.3 Developing Display Drivers

ADS provides display timings for supported displays on request. For displays not yet supported, ADS has a panel configuration service to creates panel timings and cable drawings. Contact ADS Sales for further details.

## *4.9 EMI/RFI and ESD Protection*

The GCX board incorporates a number of standard features that protect it from electrostatic discharge (ESD) and suppress electromagnetic and radio-frequency interference (EMI/RFI). Transient voltage suppressors, EMI fences, filters on I/O lines and termination of high-frequency signals are included standard on all systems. For details, see electrical specifications for subsystems of interest.

### 4.9.1 Agency Certifications

Many products using ADS single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. Because ADS supplies only the single-board computer and not fully integrated systems, ADS cannot provide meaningful system-level emissions test results.

The crystal frequencies (section 6.4.15) and electrical specifications listed in Chapter 6 may provide helpful information for agency certifications.

### 4.9.2 Protecting the Power Supply Inputs

It is the responsibility of the designer or integrator to provide surge protection on the input power lines. This is especially important if the power supply wires will be subject to EMI/RFI or ESD.

# 5 Power and Power Management

This chapter describes the architecture of the GCX power supply, factors affecting power consumption and reference designs to get you started. For information about how much power the GCX consumes, consult the electrical specifications in section 6.4.2.

## *5.1 Power Management Modes*

This section describes the various power management modes of the XScale processor and how the GCX makes use of them.

### 5.1.1 XScale Power Management Modes

The XScale PXA255 processor supports four operational modes: Turbo, Run, Idle, and Sleep.

- Sleep mode uses the least amount of electrical power. The processor core is powered off and only a few processor peripherals (RTC, I/Os and interrupt control) remain active. The transition back to Run mode may take a few hundred milliseconds, as clocks must stabilize and hardware that was powered off must be reinitialized.
- Idle mode reduces power consumption by pausing the processor core clock. Processor peripherals remain enabled. This mode is used for brief periods of inactivity and offers a quick transition back to Run mode.
- Run mode is the typical mode used when applications are running. It offers the best MIPS/mW (performance vs. power) performance when running applications from RAM.
- Turbo mode runs the processor core at up to three times the Run mode speed. Since external memory fetches are still performed at the memory bus frequency, Turbo mode is best used when running the application entirely from cache.

Most handheld and portable systems available today never really turn "off." They make use of power management algorithms that cycle the electronics into "idle" and "sleep" modes, but never fully remove power from the full system.

### 5.1.2 Power Management on the GCX

The GCX can actively be configured to be in XScale Run, Turbo or Sleep modes. Idle mode is controlled by the operating system or application and is typically transparent to the application.

In Turbo, Run and Idle modes, the power supplies are in their standard, full-power state and applications run normally on the system. The operating system is responsible for adjusting the core voltage (Vddi) for optimal power consumption in each mode.

In Sleep mode, sometimes called "Suspend" mode, the processor puts the SDRAM in a low-power, self-refresh mode, the processor core shuts off, most peripheral sub-systems are shut down and the power supplies drop into low-power states or turn off entirely. In this state, most of the power that the GCX consumes is from maintenance of the RAM (see section 6.4.2 for specifications). The system can be "awakened" and returned to the Run state by initiating a system wakeup using one of the methods described in section 5.2.2.

## 5.2 Architectural Overview and Power Management Features

This section provides an overview of the architecture of the GCX power supply and a description of the various features of the GCX power management systems.

### 5.2.1 Power Supply Architecture

The GCX power supply is organized as shown in the following diagram.

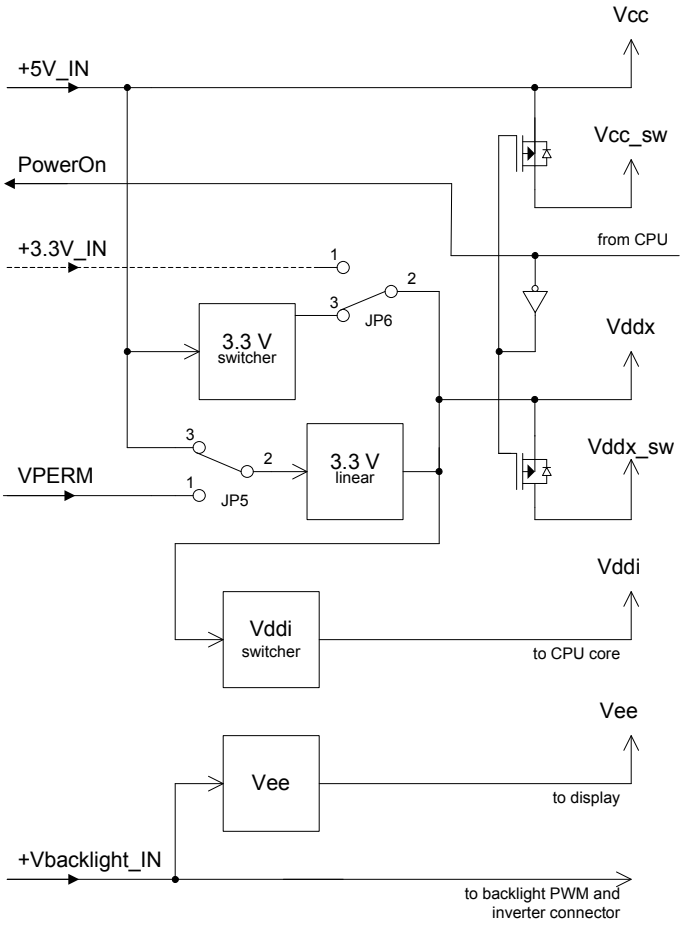



**Figure 9 The GCX Power Supply**

Both Vcc (5 V) and Vddx (3.3 V) have switched counterparts that are turned off when the board is in Sleep mode. Vcc_sw and Vddx_sw are used internally, while Vcc and Vddx are available to external peripherals on header J7.

Vddi is a variable-voltage power supply controlled by the XScale $I^2C$ bus (4.5.7, 6.4.1). This voltage scaling feature allows the operating system to manage power consumption over the full range of CPU clock rates.

Options available to volume production customers are indicated by dashed lines in the diagram above, but are otherwise outside the scope of this manual. Contact your ADS sales representative if you believe one or more of these options is required for your order.

Specifications for the GCX power supply are listed in section 6.4.1.System Sleep

This section describes several methods for putting the system into Sleep mode. Section 5.2.3 describes how to return the system to Run mode.

#### *Software Control*

Applications can put the system to sleep programmatically. Operating systems may also put the system to sleep. In remote, battery-powered applications, software Sleep can be used in conjunction with the Timed Wakeup feature (section 5.2.3) for minimum power consumption.

#### *RqOnOff Input*

Operating systems and applications can configure the /RQONOFF signal to put the system to sleep. In conjunction with the wakeup function (below), the RQONOFF input can be used as an "on/off" button for some systems. Electrical specifications are listed in section 6.4.3.

### 5.2.3 System Wakeup

This section describes several mechanisms for waking an GCX system that has been placed in Sleep mode (section 5.2.2). The system will resume operation in Run mode unless the power supply voltage is lower than Vsleep (section 6.4.3). If the input voltage is too low, the system will not wake under any circumstances. This protects the RAM from getting corrupted by an under-voltage condition.

#### *RqOnOff Input*

Shorting the /RQONOFF signal to ground will wake the system. The signal is connected to the CPU (GPIO0, 4.1.5). Electrical specifications are listed in section 6.4.8.

#### *Timed Wakeup*

The XScale can wake up at a predetermined time. This feature is controlled by software.

### 5.2.4 Backlight Power

The GCX provides software control of Backlight Intensity and On/Off. Power for the backlight is routed through the board from header J5 out to J13. This provides the greater flexibility when selecting backlight inverters for an application. See section 4.8.2 for further details about backlight control.

### 5.2.5 Power Supply Efficiency

The GCX power supply achieves high efficiency through several means. First, it utilizes high-efficiency switching regulators. These regulators use conventional step-down switchers under operating load conditions, but are configured by the system for linear and "burst" mode[11] operation during low-load conditions that occur during system sleep. Additionally, there is only one level of cascaded regulation, reducing the losses that multiply through each stage.

[11] "Burst mode" in this context is a registered trademark of Linear Technology Corporation

## 5.3 Designing for Optimal Power Management

Designing a system for optimal power management requires careful attention to many details. This section provides some guidelines and tips for best power management.

### 5.3.1 Create a Power Budget for Peripherals

Embedded system designers using the GCX should have a clear understanding of how power usage will be allocated in the system they design. Designers should create a power budget that takes into account the types of devices that are expected to be used with the GCX.

The following lists detail some of the typical external loads that can be placed the GCX power supplies. Baseline power consumption of the GCX is listed in section 6.4.2.

#### *3.3 V Loads*

Typical external loads on the 3.3 V power supply include the following:

- Display
- Some PCMCIA cards

#### *5 V Loads*

5 V loads come from both onboard and external devices. Typical loads include the following:

External:

- Display
- Most PCMCIA cards
- PS/2 keyboard
- Speaker(s)
  *Assume 80% efficiency*

Onboard:

- 3.3 V Supply
  *Multiply by 115% to account for 3.3 V power supply efficiency*

### 5.3.2 Power Loads During Sleep

When designing systems for minimal power consumption during Sleep mode, make sure to consider DC losses to external connections. The following are a few of the ways your system may "leak" when asleep:

- PCMCIA cards
  Cards in place when the system is asleep can drain power through the Card Detect and Voltage Sense lines. Assume that all four lines ground the GCX PCMCIA pull-ups (section 6.4.16) while the card is inserted.
- Digital I/Os
  Review digital I/O connections for potential voltage differences from external connections when the GCX is asleep.

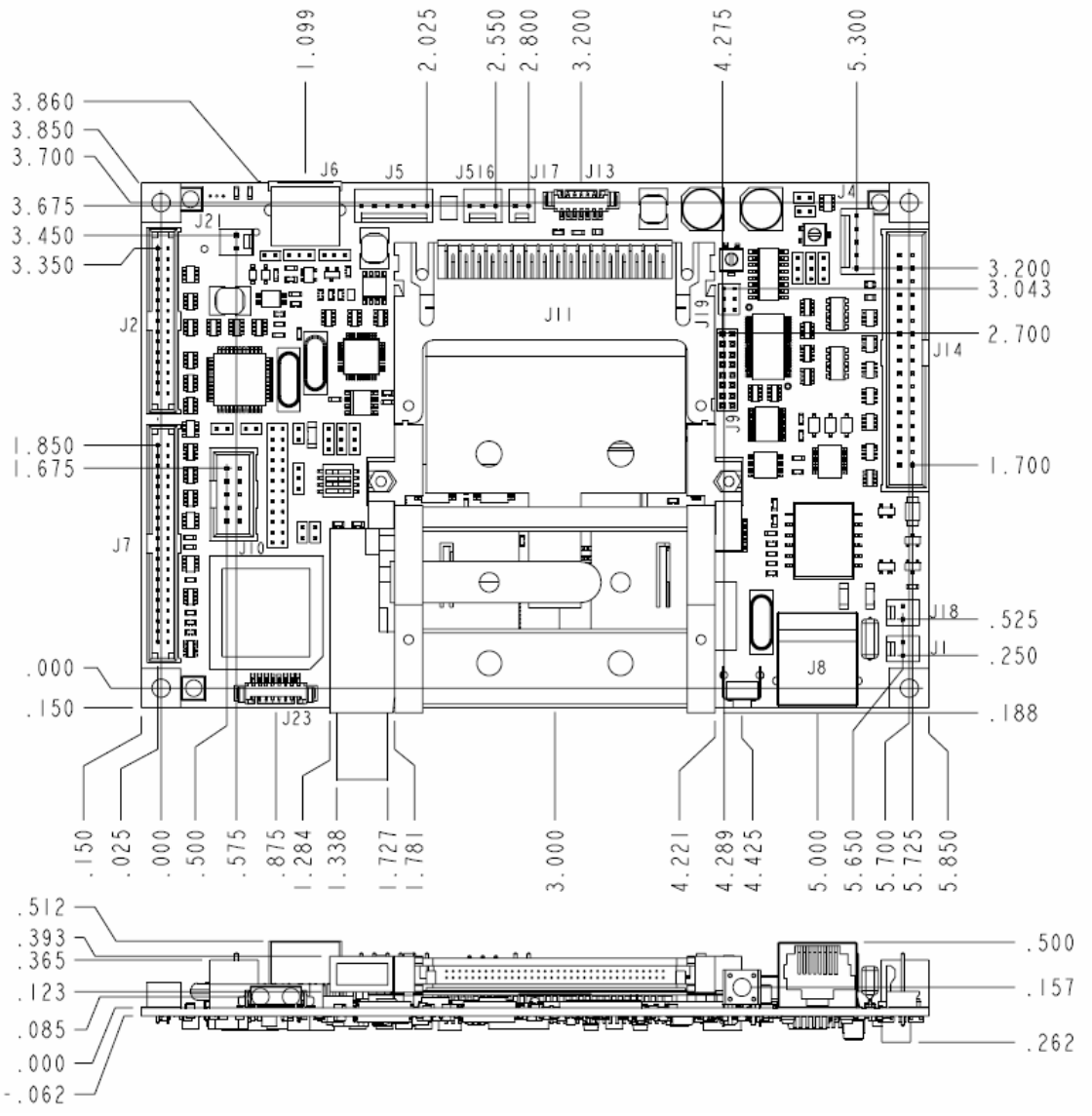
# 6 System Specifications

## *6.1 Mechanical Specifications*

The GCX is 4.0 inches by 6.0 inches in size. This section describes the component dimensions and mounting of the board. Detailed drawings are available on the support forums (section 2.4), and 3D models are available from ADS in electronic format for production customers.

### 6.1.1 Mechanical Drawing

The following mechanical drawing specifies the dimensions of the GCX, as well as locations of key components on the board. The PCMCIA ejector can be detached from the board header and is a volume production option. All dimensions are in inches. This image is an excerpt from the full mechanical drawings, ADS document number 630116-1000B.



### 6.1.2 Mounting Holes

Four holes are provided, one on each corner, for mounting. The diameter of the holes is 0.138-in. Mounting holes are plated through and connected to the GCX ground plane.

For reliable ground connections, use locking washers (star or split) when securing a GCX in an enclosure. Make sure that washers do not extend beyond the limits of the pads provided.

### 6.1.3 Clearances

The GCX has a low profile. It can fit in an enclosure with inside dimensions as thin as 0.936 inch (23.8 mm). Key clearances are as follows:

- Highest component: 0.512 inch (13.0 mm), top
  0.262 inch (6.7 mm), bottom
- Board thickness: 0.062 inch (1.6 mm)
- Clearance over top and bottom: 0.05 inch (1.3 mm), each

Note: Selection of connectors and wiring harnesses will determine height of final assembly.

## *6.2 Volume Production Options*

The GCX has a number of production options detailed throughout this manual. This section describes options that most significantly affect the mechanical design of the board.

These options are generally available only for volume production orders. Non-recurring configuration charges may apply.

### Install PCMCIA Ejector

Systems can be shipped with a PCMCIA ejector.

### Boot ROM

Standard GCX systems boot from the system flash. However, some applications (e.g. the gaming industry) require a removable boot ROM.

### Five-Wire Touch Panel Controller

Standard GCX systems are built with four-wire .touch panel controllers. GCX systems can be built for use with five-wire touch panels.

### Display Support

While the GCX can support many displays without modification, ADS may need to tune the GCX to support the LCD you have chosen for your application. ADS may have to produce the AGX with one ore more of the following changes:

- 5 V Display Data Buffers

  Standard systems use 3.3 V buffers on the display data lines. Some LCD displays require a higher data voltage for reliable operation.
- Different Backlight Control Voltage

  The backlight PWM voltage can be set to 3.3 V, 5 V or to Vbacklight. In addition, the filter capacitor on the PWM output can be removed. See specifications section 6.4.4 and Note 17 for added details.
- Vcon or Vee Power Supply

  Passive displays have varying voltage requirements. ADS can populate the Vee or Vcon circuits to match your display. You may also choose to configure the board for manual control of Vee or Vcon.

### Remove 3.3V Regulator

For cost-sensitive applications, the 3.3 V regulator can be removed. JP6 must be set to use an external 3.3V supply.

### Serial 1: J1708 or 3.3 V Logic Level

See section 4.5.1 for details.

### Serial 2: Header J23 for IrDA

See section 4.5.1 for details.

### Serial 3: 3.3 V Logic Level

See section 4.5.1 for details.

### Mating Headers on Underside of Board

Through-hole signal headers can be mounted on the underside of the GCX. This allows the GCX to sit on top of another board.

Note that added configuration charges may apply for the creation of alternate test fixtures.

Important! When the headers are placed on the underside of the board, the pin numbers will not correspond to the signals as described in this manual. Lay out the mating board with this in mind.

### Connector Plating

ADS can populate headers with other platings as required.

## *6.3 Environmental Specifications*

The GCX is designed to work under a wide range of environmental conditions.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Temperature | | | | | |
| Trun | operating temperature | -40 | | +85 | °C |

## 6.4 Electrical Specifications

This section describes the electrical specifications of the GCX.

### 6.4.1 Power Supply

The GCX is powered from a 5 V DC supply and generates additional voltages for onboard logic. The 5 V and 3.3 V supplies are available on the GCX output connectors and are limited to the current draws specified below.

The system time is maintained by a DS1307 real-time clock and powered by a long-life battery (Panasonic BR1225-1HC or equivalent; located at D5-D6 on the top side of the GCX).

| Symbol | Parameter | | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| System Power | | | | | | |
| 5V_IN | 5.0 V power input, +/-5% | | 4.75 | 5.0 | 5.25 | V |
| VDDI | Processor core voltage (6.4.14) | | 0.85 | 1.0 | 1.3 | V |
| VDDX | 3.3 V onboard supply, +/-5% | Run | 3.1 | 3.3 | 3.5 | V |
| | | Sleep | | 3.15 | | V |
| I (Vddx) | 3.3 V available for display, PCMCIA, external peripherals, etc. (Note 1) | Run | | | 700 | mA |
| | | Sleep | | | 100 | mA |
| I (Vcc) | 5 V available for display and external peripherals (note 2) | | | | 1000 | mA |
| RTC Backup Power (4.2) | | | | | | |
| V BATPOS | real-time clock battery backup | | 2.2 | 3.0 | 3.6 | V |
| I BATPOS | RTC current (note 3) | | | 300 | 500 | nA |

Notes:

1. During Sleep mode, Vddx is powered by a linear regulator, which is powered by the voltage selected by JP5 (3.3.4).
2. In addition to the limits of the external 5V_IN power supply, the 5 V output is limited by the trace widths on the printed wiring board.
3. Vddx=0V, Vbatpos=3.2 V (source: DS1307 data sheet)

### 6.4.2 Power Consumption

The following table lists typical power consumption for the GCX at varying activity levels.

Power consumption varies based on peripheral connections, components populated on the system and the LCD panel connected. Factors that affect power consumption to a lesser extent include input voltage, temperature and the level of processor activity.

LCD displays and backlights add significantly to the total power consumption of a system. ADS development systems include the Sharp LQ64D343 5V TFT VGA display, which draws about 1 W, and the Taiyo-Yuden LS520 backlight inverter, which draws about 6 W at full intensity.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| I sleep | Sleep mode current (note 4) | | 7.5 | | mA |
| P idle | Idle mode power (note 5) | | 1.6 | | W |
| P run | Run mode power (note 6) | | 2.1 | 3 | W |

Notes: Power consumption was measured on a fully populated 64 MiB GCX with no peripheral connections under the following conditions:

4. System in Sleep mode, Vsleep=5.0V (JP5, 3.3.4)
5. System running only the Windows CE desktop (predominantly in Idle mode; <5% CPU utilization)
6. Typical measurement indicates full utilization (95-100%) of processor core, achieved by running multiple instances of a graphical application under Windows CE

### 6.4.3 Sleep and Wakeup

The GCX supports a low-power Sleep mode that is triggered by software, from a power fault or with the RqOnOff . "Wake" the GCX by shorting the RqOnOff signal to ground.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Sleep (5.2.2) | | | | | |
| Vsleep | Sleep trigger voltage (Note 7) | | 4.5 | | V |
| Vsleep,hyst | Sleep trigger release hysteresis (Note 8) | 0.06 | | 0.25 | V |
| Wakeup: RqOnOff (5.2.3) | | | | | |
| trq | wakeup pulse duration (Note 9) | 100 | | | ms |
| Vprq | pull-up voltage | | Vddx | | V |
| Rprq | pull-up resistance | | 47 | | kΩ |
| Vih,max | maximum input voltage | | | 3.3 | V |
| Vil | trigger voltage | | | 0.9 | V |

Notes:

7. This is the voltage of VPERM (selected by JP5) at which the DC_GOOD signal (4.3.6) changes from high to low, which can trigger the system to go into Sleep mode. DC_GOOD is connected to the system controller.
8. **Important!** Once Vsleep has been triggered, the input voltage must rise at least Vsleep,hyst above Vsleep before the voltage detector will restore the DC_GOOD signal. Make sure that your input voltage is designed to always run above Vsleep+Vsleep,hyst, or systems that go to sleep may not be able to wake again.
9. Short /RqOnOff to GND to for at least trq to wake up system. A low-level voltage on /RqOnOff initiates wakeup.

### 6.4.4 Display

LCD display panels have a wide range of voltage and data requirements. The GCX has a number of adjustable voltages to support these requirements, as well as controls for brightness (backlight) and contrast (passive panels only). See section 4.8 for further details.

Standard production GCXs use the PXA255's graphics controller.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| LCD (4.8.2) | | | | | |
| Pnl_pwr | LCD voltage (note 10) | 3.3 | | 5.0 | V |
| P pnl_pwr | LCD power (note 11) | | | 2 | W |
| V pnl_data | LCD data voltage (note 12) | 3.3 | 3.3 | 5.0 | V |
| Scan Direction (active displays) (3.3.2, 3.3.3, 4.8.2) | | | | | |
| R pnl_scan | Pull-up resistance | | 4.7 | | kΩ |
| V pnl_scan | Pull-up voltage | 0 | Pnl_pwr | Pnl_pwr | V |
| Contrast Control (passive displays) (3.2.5, 3.3.14, 4.8.2, note 14) | | | | | |
| Vee(-) | $R_L$=5kΩ, J19: 1-2 (note 13) | -30 | | -15 | V |
| Vee(+) | $R_L$=5kΩ, J19: 2-3 (note 13) | 15 | | 30 | V |
| Vcon | Low-voltage contrast adjust (note 14) | 0 | | 1.4 | V |
| Brightness Control (backlight, 4.8.2) | | | | | |
| Vbacklight | Backlight and Vee supply (note 13) | 5 | 12 | 18 | V |
| R backlightOn | Pull-up | | 10 | | kΩ |
| V backlightOn | With pull-up (note 15) | | | 12 | V |
| | No pull-up (note 16) | | | 30 | V |
| V backlightPWM | PWM (note 17) | 0 | | 5 | V |
| R backlightPWM | PWM series resistance (note 18) | | 2.2 | | kΩ |

Notes:

10. Jumper JP1 (3.3.1) selects the display voltage.
11. Total power available depends on system power budget.
12. Systems are configured at the factory with buffers for 3.3 or 5 V panel data. Jumper JP3 (3.3.6) selects the voltage for those buffers. 5 V displays with Vih <= 0.6•Vpnl_pwr (3.0 V) will work reliably with 3.3 V data. 3.3 V buffers can be run at 5 V for test purposes, but if your application requires 5 V data, contact ADS Sales to ensure the correct buffers are used for your display.
13. The onboard Vee power supply is powered by Vbacklight. Vee specifications shown are for Vbacklight at 5 V. The Vee power supply can generate more power when Vbacklight is a higher voltage.
14. Vcon is the filtered, low-voltage PWM signal used to control Vee. It can be used directly with some passive displays to control contrast. Vcon and Vee are controlled by PXA255 PWM0. Vcon is the 3.3 V PWM signal RC filtered with a 43% (1k/750Ω )voltage divider. As a factory production option, Vcon can be controlled by variable resistor VR2 (3.2.6), giving an output range of 0 to PNL_PWR. For factory options, see section 6.2.
15. The BacklightOn signal is an open-collector output managed by the system controller CPLD.
16. As an option for volume production orders, the pull-up resistor can be removed for use with an external pull-up resistor. The maximum voltage rating of the transistor is listed.
17. The standard configuration for BacklightPWM signal is as an open collector output with a 5 V pull-up. Supply the "Vbacklight" voltage at power header J5, pin 4. For volume production orders, the PWM output can be configured as 3.3 V, 5 V or Vbacklight open-collector output, with or without an output filter capacitor. For other factory options, see section 6.2.
18. The backlight PWM output is driven by PXA255 PWM1.

### 6.4.5 UCB1400

The UCB1400 drives the audio subsystem, the analog-resistive touch panels, analog inputs and ten digital I/Os. See section 6.4.13 for audio specifications.

**Absolute Maximum Ratings**

Input voltage, any pin.....5.5 V

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Vdd | Supply voltage | | Vddx | | V |
| Touch Panel | | | | | |
| | A/D sample resolution | | 10 | | bit |
| Digital Outputs (4.6.1) | | | | | |
| Vol | Iol=2mA | | | 0.4 | V |
| Voh | Ioh=-2mA | 2.8 | | | V |
| Digital Inputs (4.6.1) | | | | | |
| Vil | | | | 0.8 | V |
| Vih | | 2.0 | | | V |
| A/D Inputs (4.6.2) | | | | | |
| n | resolution | | 10 | | bit |
| Rin | input impedance (note 19) | | 1.3 | | kΩ |
| Vin | A/D input voltage | 0 | 10 | | V |
| Vref | A/D reference voltage | | 1.65 | | V |

Notes:

19. UCB1400 analog inputs include a 75% voltage divider with 332Ω in series and 1kΩ to ground.

### 6.4.6 Five-Wire Touch Panel Controller (factory option)

Standard GCX systems use the UCB1400 to drive the touch panel. For volume production orders, it is also possible to install touch panel controllers from Texas Instruments. In this case, the GCX uses the ADS7846 to support four-wire analog-resistive touch panels and the ADS7845 to support five-wire panels.

All touch-panel signals are ESD and RF protected.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| ADS7845 and ADS7846 | | | | | |
| Vdd | Supply voltage | | Vddx | | V |
| | A/D sample resolution | | 12 | | bit |

## 6.4.7 ADSmartIO Controller

The ADSmartIO Controller is a second RISC microcontroller on the GCX designed to handle I/O functions autonomously. The GCX communicates with the ADSmartIO controller via the system controller CPLD. On the GCX, ADSmartIO is implemented with the Atmel ATmega8535L microcontroller, which has 512 bytes EEPROM.

### Absolute Maximum Ratings

Input voltage, any pin .....3.8 V

Input voltage, A/D inputs PA5-PA7 (note 23) .....15 V

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Vdd | ADSmartIO supply voltage | | 3.3 | | V |
| Rs | Series resistance (note 20) | 33 | 1k | | Ω |
| Vprot | (note 20) | | | | V |
| Digital Outputs (4.3.3) | | | | | |
| Vol | | | | 0.5 | V |
| Voh | | 2.3 | 3.3 | | V |
| I sink | (see note 20) | | | 20 | mA |
| I source | (see note 20) | | | 12 | mA |
| Digital Inputs (4.3.3) | | | | | |
| Vil | | | | 1.0 | V |
| Vih | | 2.0 | | | V |
| R | Software-selectable pull-ups to 3.3 V (see note 21) | 35 | | 120 | kΩ |
| A/D Inputs (4.3.4, 4.6.2) | | | | | |
| n | resolution (note 22) | | 8 | 10 | bit |
| Rin | input impedance (note 23) | | 43.2 | | kΩ |
| Vin | A/D input voltage range (note 23) | 0 | | 10.8 | V |
| Vref | A/D reference voltage (note 24) | | 2.5 | | V |
| Ivref | Current drain from ref voltage | | | 100 | uA |
| I (Vref) | J10.43 | | | 100 | μA |

Notes:

20. Row and column I/Os have series resistance and over-voltage protection to ground. The series resistance limits the dc current that any one pin can source or sink. SMTIO2 and 3 (PB2 and PB3) have 33 ohm series resistance, so can source or sink the maximum current supported by the ATmega microcontroller.
21. Control pull-up resistors by writing to bits of IO port when the port is configured as a digital input (bit mask 1=enable, 0=disable).
22. Digital noise on the board may degrade analog performance under some conditions.
23. ADSmartIO A/D inputs include an input voltage divider of 33.2k series with 10k to ground.
24. Vref is usually turned off when the system is in Sleep mode (section 5.2.2).
25. Specifications based on ADSmartIO release 1010 rev 2 (ADS release #700114-10102)

### 6.4.8 System Controller

A Xilinx XCR3064XL CPLD on the GCX provides system logic for chip selects, power management, interrupt decoding, clock generation, PCMCIA logic and other system control functions. It is programmed at the factory using the JTAG interface (3.4.8).

**Absolute Maximum Ratings**

Input voltage, digital I/O pins..... -0.5 to 5.5 V

Output current, continuous,
digital I/O pins ..... -100 to 100 mA

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Vdd | Supply voltage | | 3.3 | | V |
| Digital Outputs | | | | | |
| Vol | Iol=8mA | | | 0.4 | V |
| Voh | Ioh=-8mA | 2.4 | | | V |
| Digital Inputs | | | | | |
| Vil | Low-level input voltage | 0 | | 0.8 | V |
| Vih | High-level input voltage | 2.0 | | 5.5 | V |

### 6.4.9 Serial Ports

The GCX supports several serial ports as described in section 4.5.1. Serial ports 1 through 3 are controlled by the XScale processor.

EIA-232 signals are generated using charge pump devices (e.g. Sipex SP3232 and SP3243). Signals 422/485/J1708 are buffered with the Maxim MAX491. IrDA signals from the XScale are converted to IrDA using a Vishay TFDU6100 infrared transceiver.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| | Logic voltage, serial ports | | 3.3 | | V |
| IrDA (4.5.2) | | | | | |
| VccRxIrda | Receiver voltage | | 3.3 | | V |
| RvccRxIrda | Receiver power series resistance | | 10 | | Ω |
| VccTxIrda | Transmitter voltage | | 3.3 | | V |
| RvccTxIrda | Transmitter power series resistance | | 3.6 | | Ω |
| PtxIrda | Transmitter power | | 330 | 630 | mA |

### 6.4.10 USB

The GCX supports USB operation as described in section 4.5.4. See section 6.4.14 (PXA255) for USB function port specifications.

### 6.4.11 Ethernet

The GCX uses an SMSC LAN91C111 10/100 BT Ethernet controller. The MAC (Media Access Control) address is stored in a serial EEPROM connected to the controller.

### 6.4.12 CAN Bus

The GCX uses two SJA1000T CAN controllers with Intel 82C251 CAN transceivers for its CAN bus capabilities.

## 6.4.13 Audio

For its audio sub-system the GCX uses the Phillips USB1400, an AC '97 stereo codec with dual audio input and output channels. Specifications for other features of the UCB1400 are listed in section 6.4.5.

The standard GCX includes a power amplifier (Texas Instruments TPA301DR) to drive a single, bridge-tied output speaker. As a factory option, the amplifier can be removed and the signals rerouted to support the single-ended, stereo headphone output driver of the UCB1400. The mono and stereo options are illustrated in the following diagrams:

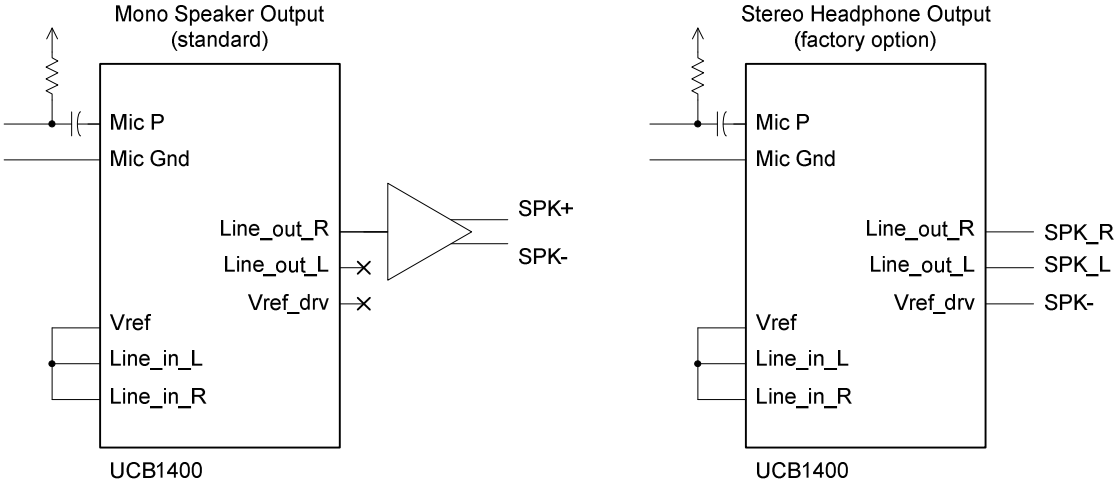



**Figure 10 GCX with Mono Speaker Amp (left) and Stereo Headphone Option (right)**

### Absolute Maximum Ratings

Vin_mic .....3.3 Vdc

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| DVdd | digital supply voltage | | 3.3 | | V |
| Avdd | analog supply voltage | | 3.3 | | V |
| fs | codec sampling rate (note 26) | 8 | | 48 | kHz |
| Audio Input | | | | | |
| Gain_mic | pre-amp gain (note 27) | 0 | | 42.5 | dB |
| Rin_mic | input impedance | | 10 | | kΩ |
| Cin_mic | DC blocking capacitor | | 1 | | µF |
| Vmicpwr | microphone power | | 3.3 | | V |
| Rmicpwr | microphone power, series resistance | | | 6.9 | kΩ |
| Audio Output, Mono Amplifier | | | | | |
| Avdd | analog supply voltage | | 3.3 | | V |
| Rl | speaker load | 8 | | | Ω |
| Po | Output power, THD=1%, f=1kHz | | 250 | | mW |
| Av | Amplifier gain | | 1 | | V/V |
| Vpp | Output voltage swing | | | 2.3 | Vpp |
| Vod | Differential output voltage, amplifier enabled, Rl=8Ω | | 5 | 20 | mV |
| THD+N | Total harmonic distortion plus noise Rl=8Ω, Po=250mW, f=20Hz-4kHz | | -38 | | dB |

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Audio Output, Stereo Headphones (factory option) | | | | | |
| Rl | speaker load | 16 | 32 | | Ω |
| Po | Output power, Rl=32Ω | | 25 | | mW |
| Cl | Load capacitance | | | 30 | pF |
| (THD+N)/S | Ratio of total harmonic distortion plus noise to signal, F=48kHz, Rl=32Ω | | -40 | | dB |

Notes:

26. The UCB1400 supports sample rates of 8, 11.025,12, 16, 22.05, 24, 32, 44.1 and 48kHz. The codec can sample input and output streams at independent rates.
27. The UCB1400 includes a programmable gain amplifier that can .be set in increments of 1.5 dB.

### 6.4.14 PXA255 Processor

The XScale PXA255 core can change system voltage Vddi (6.4.1) dynamically to achieve lower power consumption at high clock rates. It uses voltage Vddx to power its interface I/Os. The digital I/Os include series resistance and ESD protection.

Serial ports configured for 3.3 V logic operation run directly to the processor (section 4.5.1). These lines should be treated as digital I/Os and protected for over-current and over-voltage accordingly.

**Absolute Maximum Ratings**

Input voltage, digital I/O pins.....3.6 V

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Digital Outputs | | | | | |
| Vol | | | 0 | | V |
| Voh | | | 3.3 | | V |
| Io | | -2 | | 2 | mA |
| Digital Inputs | | | | | |
| Vil | | | | 0.2 | $V_{ddx}$ |
| Vih | | 0.8 | | | $V_{ddx}$ |
| NSSP Port | | | | | |
| | Base bit rate, internal clock | | 3.6864 | | MHz |
| | Divisor for Internal clock | 1 | | 4096 | |
| | Clock rate, external source | | | 13 | MHz |

### 6.4.15 Crystal Frequencies

Agencies certifying the GCX for compliance for radio-frequency emissions typically need to know the frequencies of onboard oscillators. The following table lists the frequencies of all crystals on the GCX.

| Crystal | Device | Typ. | Units |
|---|---|---|---|
| X1 | Ethernet | 25.000 | MHz |
| X2 | ADSmartIO microcontroller | 3.6864 | MHz |
| X3 | XScale core | 3.6864 | MHz |
| X4 | XScale real-time clock (RTC) | 32.768 | kHz |
| X5 | CAN controller | 16.000 | MHz |
| X6 | Battery-backed RTC | 32.768 | kHz |
| X7 | UCB1400 codec | 24.576 | MHz |

### 6.4.16 PCMCIA

The PCMCIA port on the GCX is managed by the system controller (6.4.8) with firmware developed by ADS. The signals run through buffers before going to the PCMCIA (J11) header.

**Absolute Maximum Ratings**

Input voltage, port I/O pins.....6.5 V

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| $V_{ddx}$ | PCMCIA buffer power | | 3.3 | | V |
| $V_{ccCard}$ | PCMCIA supply voltage (note 28) | 3.3 | 5.0 | 5.0 | V |
| I 3.3V | 3.3 V socket power | | | 2 | W |
| I 5V | 5 V socket power | | | 2 | W |
| Rp pcmcia | Card detect (1 & 2) and voltage sense (VS1 & 2) pull-ups (note 29) | | 100 | | kΩ |
| Vp pcmcia | Card detect and voltage sense pull-up voltage | | 3.3 | | V |
| Digital Outputs | | | | | |
| Vol | | | | 0.2 | V |
| Voh | | 3.1 | | | V |
| Digital Inputs | | | | | |
| Vil | Vddx=3.3 V | | | 0.8 | V |
| Vih | Vddx=3.3 V | 2.0 | | 5.5 | V |

Notes:

28. The PCMCIA port supply voltage is selected programmatically.
29. Each card inserted in a PCMCIA slot can drain up to 0.4 mW when the system is in Sleep mode ( 4 * ($Vddx^2$/Rpcmcia) ).

### 6.4.17 $I^2C$ Bus Master

The I2C bus on the GCX is driven by the PXA255 and is configured as described in section 4.5.7.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| | bus clock (note 30) | 100 | | 400 | kHz |
| | buffer size | | | 1 | byte |
| Rbus | pull-up on SDA, SCK | | 1.8 | | kΩ |
| Vbus | | | 3.3 | | V |
| Rseries | resistance to ADSmartIO bus | | 33 | | Ω |

Notes:

30. The PXA255 supports "standard" and "fast" I2C speeds of 100 and 400 kHz.

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# 7 Board Revision History

## 7.1 Identifying the board revision

The product revision number of the GCX is etched on the underside of the printed circuit board. That number is 170116-1000x, where "x" is the board revision.

## 7.2 Revision History

The following is an overview of the revisions of the GCX circuit board.

### 7.2.1 Revision 1

Initial release.

The GCX was designed to be backward compatible with the StrongARM SA-1110 Graphics Client Plus product. The following summarizes the changes from revision F of the GC Plus:

#### *New Features*

Serial 3 adds four modem control signals to become a 9-wire serial port

NSSP signals replace unused modem interface lines on J2

| Pin | From | To |
|---|---|---|
| *19* | *UCB_TINP* | *NSSP RXD* |
| *21* | *UCB_TINN* | *NSSP TXD* |
| *23* | *UCB_TOUTN* | *NSSP SFRM* |
| *25* | *UCB_TOUTP* | *NSSP SCLK* |

LAN91C1111 10/100 Ethernet controller replaces 10BT LAN91C96

Supports five-wire touch panels (volume production option)

Support for stereo headphone output (volume production option)

Adds JP24 for RTC power (volume production option)

#### *Enhancements*

AC'97 UCB1400 replaces the UCB1200 codec and touch panel controller

Philips SJA1000T CAN bus controller replaces the Intel 82527.

Amplifier for speaker output

Option for stereo audio output

Socketed boot ROM is now optional

Vee is powered by Vbacklight (6.4.4)

#### *Other Changes*

Orientation of some configuration shunts has changed

JP16 and JP17 are generally no longer needed, as Serial 3 is now a 9-wire port

Removes GC Plus JP22 (LED1/audio oscillator)

Profile is slightly higher

### 7.2.2 Revision A

First production release. This revision makes a number of mechanical changes that improve manufacturability and durability.

#### *Enhancements*

RTC battery is mounted flat; no longer vertical

#### *Changes*

JP5 and JP6 are rotated 180 degrees

JTAG and ADSMARTIO ISP signals combine onto single header J9

Adds power-on reset supervisor

Improved PCMCIA power control logic

Update Ethernet and CAN logic

Update onboard 3.3V supply

Vee and backlight PWMs move from ADSMARTIO to PXA255

Backlight on/off moves from ADSMARTIO to CPLD

### 7.2.3 Revision B

Second production release.

#### *Enhancements*

Sleep mode regulator can be turned off with a digital I/O

LCD power transistor supports higher current

#### *Changes*

Vee is not populated on standard production systems.