Applied
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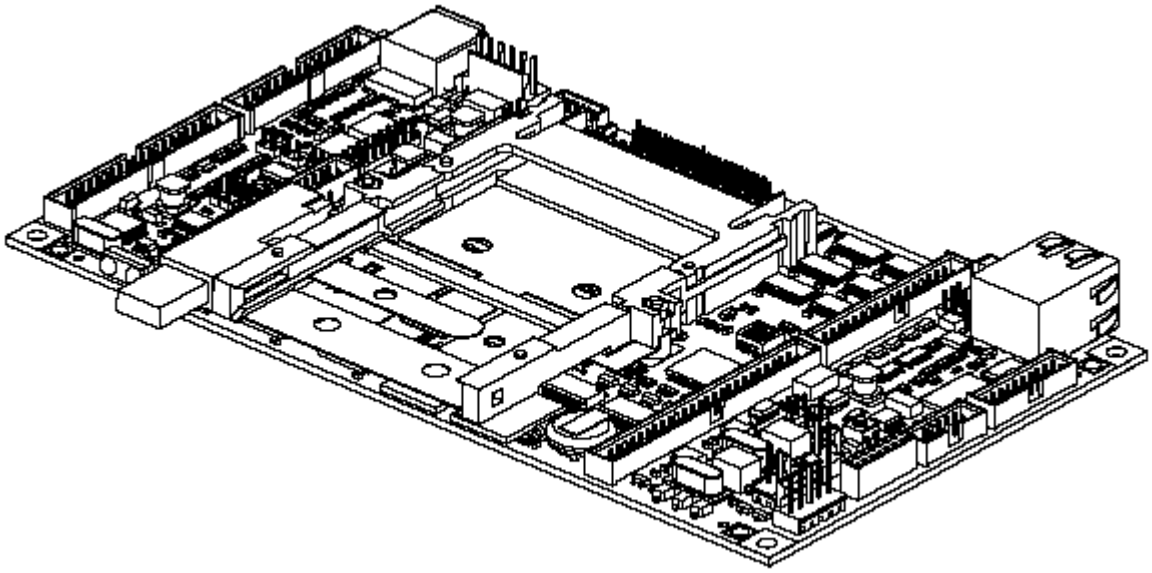
VGX User's Manual



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ADS document # 110116-20012

About the Cover Image

The cover image shows a fully populated Rev A VGX.

Printing this Manual

This manual has been designed for printing on both sides of a 8.5x11 inch paper, but can be printed single-sided as well. It has also been optimized for use in electronic form with active cross-reference links for quick access to information.

Revision History

The following list summarizes the changes that have been made between released revisions of the manual.

REV	DESCRIPTION	BY
1	Initial Release	7/6/04 ak
2	Additions: Added description of changes from Rev 2 through Rev E Add section for I^2C device addresses (4.5.6) Move I^2C specifications to new section (6.2.17) Add details about J12 LVDS connector in sections 3.4.10 and 4.8.3 Add and update mating connector details Update Introduction (remove RTC and backup power) Added "13-14" to JP4 shunt settings (3.3.4) Updates: Update cover image Update J16 to 16-pin format Corrections: Add negative-logic polarity to /RESET_OUT (3.2.2, 3.4.7) Remove J12 from list of headers with LCD power (3.3.1) Correct J9.29 PNL_PWR cross-reference (JP3 to JP1) (3.4.9) Correct J19 pin 28 to PNL_PWR (3.4.17) Microphone and speaker connections J10 changed to J5; HP_IN changed from J3.32 to J14.16 (4.4) Deleted capacitor from diagram (4.5.4)	12/13/07 lcj

Table of Contents

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1 Introduction

1.1 Overview

The VGX is a full-featured single board computer using the PXA255 XScale RISC microprocessor. The VGX is designed to meet the needs of embedded and graphical systems developers.

This manual applies to the most current revision of the VGX listed in Chapter 7, the Revision History.

1.2 Features

1.2.1 Processor

- PXA255 32-bit XScale
- Clock 400 MHz, typical
- Voltage and frequency scaling

1.2.2 Power Supply

- 5 V input for main power

1.2.3 Memory

- 16, 32, 64 or 128 [1] MiB[2] synchronous DRAM
- 32 or 64 [3] MiB flash RAM
- PCMCIA and CompactFlash[4] (CF), Type I and II, 3.3 and 5 V

1.2.4 Communications

- USB 1.1 Host port (low 1.5 Mbit/s and full 12 Mbit/s speeds)
- USB 1.1 Function port, full speed (e.g. to connect to PC)
- Seven Serial Ports
  - Serial 1: EIA/TIA-232, 3.3V logic (5-wire), EIA/TIA-422/485 or J1708
  - Serial 2: EIA/TIA-232, 3.3V logic (5-wire) or IrDA
  - Serial 3: EIA/TIA-232 or 3.3V logic (9-wire)
  - Serial A and B: EIA/TIA-232 or 3.3V logic (9-wire)
  - Serial C and D: 3.3V logic (9-wire)

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[1] The VGX supports 128 MiB SDRAM. However, those components are not yet commercially available as of April 2003.

[2] MiB is the IEC abbreviation for mebibyte = 2^{20} byte = 1 048 576 byte. The kibi and mebi abbreviations are based on the 1998 IEC standard for binary multiples. For further reading, see the US NIST web site, http://physics.nist.gov/cuu/Units/binary.html

[3] The VGX supports synchronous and asynchronous flash. The 64 MiB flash option is available only in synchronous flash.

[4] CompactFlash is a trademark of the CompactFlash Association, http://www.compactflash.org/.

- 10/100BT Ethernet, RJ45
- Two independent CAN controllers
- CompactFlash Interface (card guides not included) and PCMCIA

1.2.5 User Interface and Display

- SM501 graphics accelerator
- Logic-level flat panel interface
- Backlight intensity and on/off control signals
- Software-controlled VEE generator for passive LCD contrast control
- Four-wire analog-resistive touch panel interface (five-wire factory option)
- PS/2 keyboard port

1.2.6 Discrete I/O

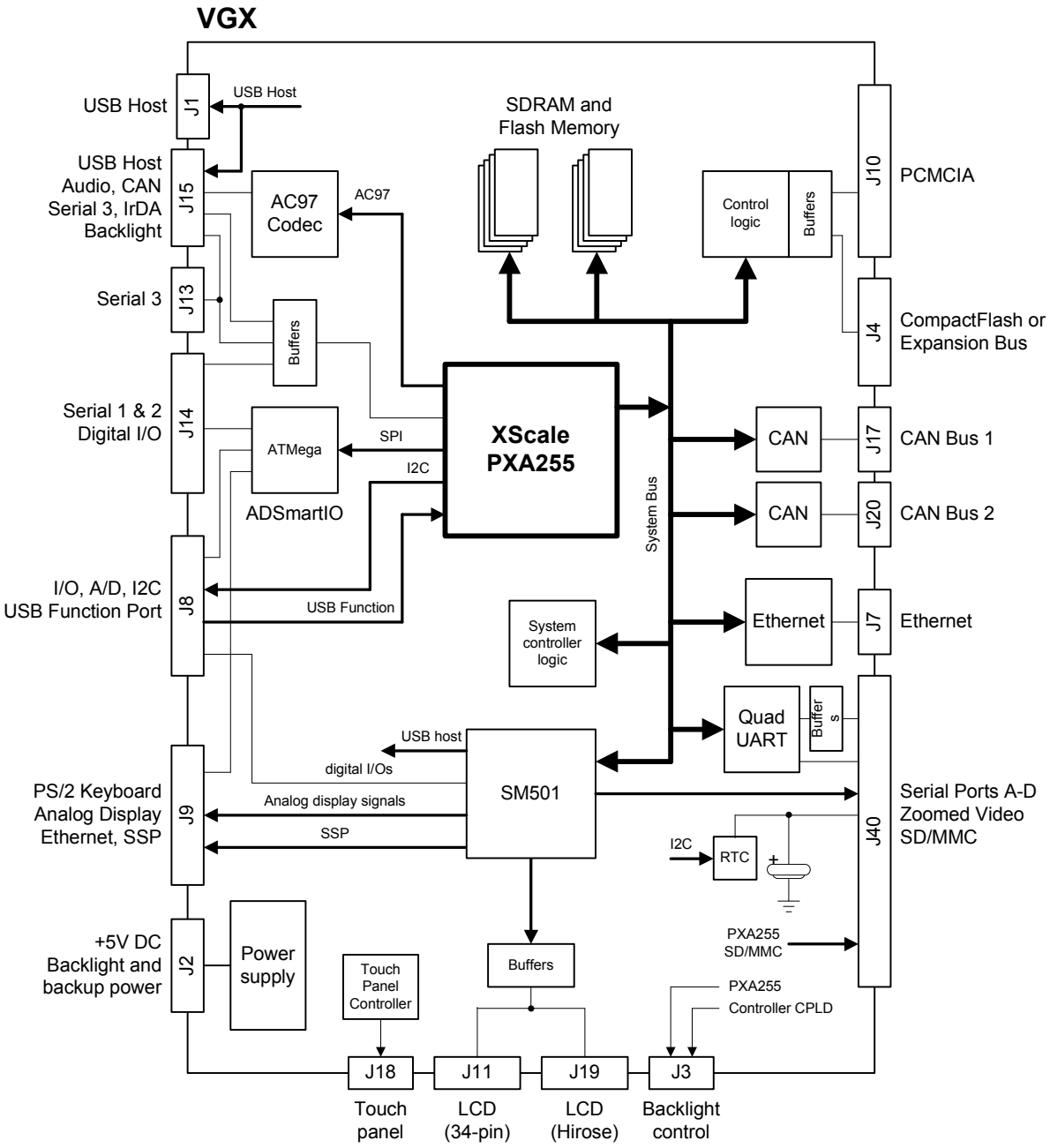
- Sixteen ADSmartIO™ ports configurable for digital I/O and/or up to 8x8 matrix keypad
- Ten additional general-purpose digital I/Os
- Four A/D inputs

1.2.7 Audio Interface

- AC '97 Codec
- Stereo Microphone Input
- Stereo 1W Speaker Outputs
- Headphone Output

1.3 Block Diagram

The following diagram illustrates the system organization of the VGX. Arrows indicate direction of control and not necessarily signal flow.



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2 Getting Started

2.1 Development Systems

VGX boards are shipped as development systems designed to get the developer up and running quickly.

To use the system, simply plug power supply into the mini DIN-8 receptacle on the system.

If the screen does not display anything after five to ten seconds, check the *Frequently Asked Questions*, below. Most operating systems cold boot within twenty seconds.

2.1.1 System Components

A typical development system is shown at right (system at right illustrates a BitsyX development system). It consists of the following components:

- VGX single-board computer
- Flat panel display and cable
- Backlight inverter and cable
- Touch screen and cable
- 120/240 VAC power adapter
- Plexiglas mounting
- Developer's Cable Kit including
  - Serial Port DB9 adapter (ADS cable #610111-80001)
  - DB9F/F null modem cable
- Operating system of your choice
- User's Guide (this document and operating system guide)

Please make sure you have received ***all*** the components before you begin your development.

2.2 Frequently Asked Questions

The following are some of the most commonly asked questions for development systems:

Q: When I plug in power, my screen is white and nothing comes up on it.

A: Check the connector seating. The flat panel connector may have come loose in shipping. Press it firmly into the panel and reapply power to your system.

Q: When I plug in power, the LED doesn't turn on.

A: Your system may still be booting. The LED is software controlled and is not necessarily turned on at boot.

Q: Do I have to turn off the system before I insert a PCMCIA or CompactFlash card?

A: No. The VGX supports hot-swapping of PCMCIA and CompactFlash cards. Consult the operating system documentation for details.

Q: Do I need to observe any ESD precautions when working with the system?

A: Yes. Where possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the board or touching any components on the board.

Q: What do I need to start developing my application for the system?

A: You will need a flash ATA card (16 MiB or larger, 32 MiB recommended) and the cables supplied with your system to interface your development station to the system. For further direction, consult the ADS guide for the installed operating system.

Q: Who can I call if I need help developing my application?

A: ADS provides technical support to get your development system running. For customers who establish a business relationship with ADS, we provide support to develop applications and drivers.

Q: Is there online support?

A: Yes. Information about the VGX hardware and software is available on the ADS support site at http://www.applieddata.net/support. See section 2.4 for further details.

Q: Can I upgrade the version of the operating system?

A: Yes. ADS provides regular operating system updates on its developers' web site. For operating systems not maintained by ADS, contact the operating system vendor.

Q: I would like to interface to a different display panel. How can I do this?

A: ADS may have already interfaced to the panel you are interested in. Consult ADS for availability.

2.3 Organization of this Manual

The manual organizes information in five key sections:

Introduction	Provides an overview of the functionality and organization of the VGX, as well as how to use this manual.
Hardware Reference	Describes the configuration settings and pinouts for all connectors and jumpers on the VGX.
Feature Reference	Gives details about the various subsystems of the VGX.
Power Management	Provides key information about power management, tips for system integration and electrical and mechanical interface specifications.
Specifications	Electrical and mechanical interface specifications.

To locate the information you need, try the following:

1. Browse the *Table of Contents.* Section titles include connector designators and their function.
2. Follow cross-references between sections.
3. View and search this manual in PDF format

2.4 Errata, Addenda and Further Information

Errata and addenda to this manual are posted on the ADS support forums along with the latest release of the manual. Consult the support forums any time you need further information or feel information in this manual is in error. You may access the forums from the ADS support site,

http://www.AppliedData.net/support

In addition to manuals, the support forums include downloads, troubleshooting guides, operating system updates and answers to hundreds of questions about developing applications for ADS products. You may also post questions you have about ADS products on the forums.

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3 Hardware Reference

This section gives an overview of the hardware features of the VGX. This overview includes a description of the switches, jumper settings, connectors and connector pinouts.

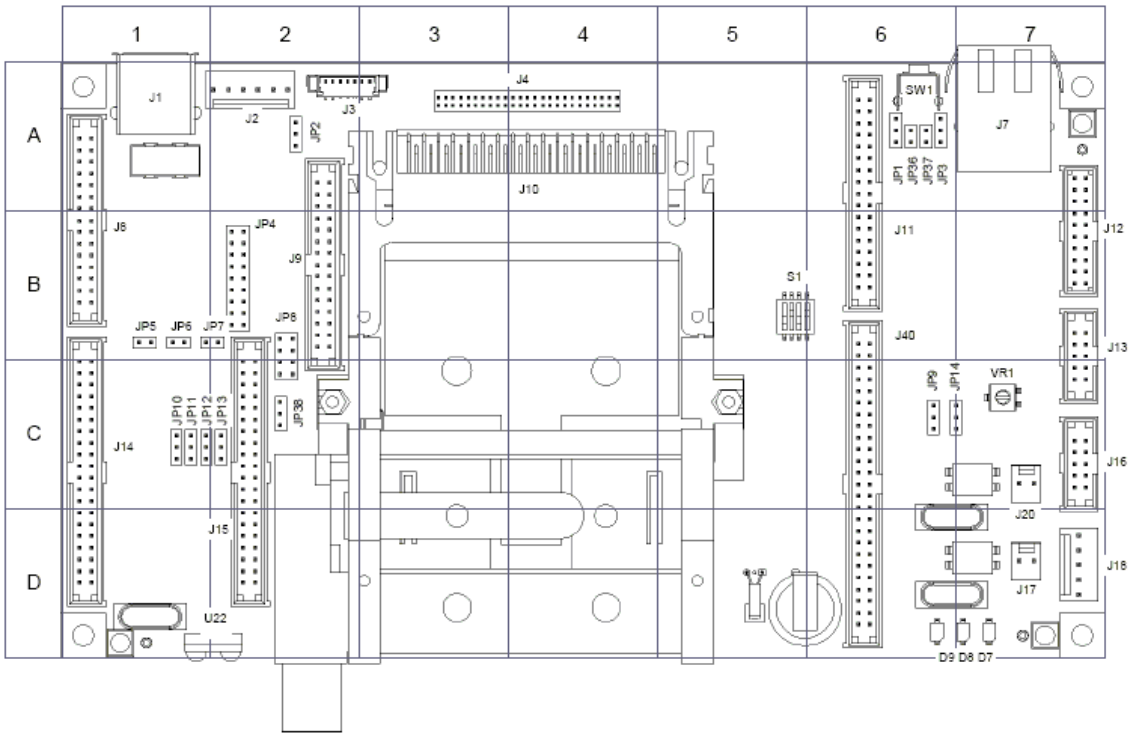
3.1 Identifying Connectors

The section describes how to locate connectors on the board and how to determine how each header is numbered.

3.1.1 Locating Connectors

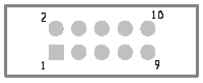
The following diagram illustrates the location of key components on the VGX. For example, the USB socket is located in square A1 and the reset button is in A6. Component listings in this chapter refer to this diagram.

This diagram shows the VGX with the PCMCIA ejector production option installed (6.1.4).



3.1.2 Determining Pin Numbers

The pins of headers and connectors on ADS products are numbered sequentially. Double-row headers place even pins on one side and odd pins on the other. The diagram at right indicates how pins are numbered, as seen from the component side[5] of the board.



[5] The "component side" of the VGX is the one on which the PCMCIA ejector is installed. As a factory option, some through-hole connectors may be installed on the "bottom side" of the VGX.

To locate pin 1 of a connector or jumper, try the following:

1. Look for a visible number or marking on the board that indicates connector pin numbering. A notch or dot usually indicates pin 1.

2. Look at the underside of the board. The square pad is pin 1.

3. Download the mechanical drawing of the VGX from the ADS Support site (section 2.4). The square or indicated pad on each connector is pin 1.

3.2 Switches, Controls and Indicators

This section describes various switches, controls and indicators on the VGX board. The location indicated for each item refers to the grid diagram of the VGX in section 3.1.1.

3.2.1 S1: DIP Switch

Location on board: B5

S1 is a four-position DIP switch. When in the "ON" position, switches are closed and connect to ground. Otherwise they are pulled up. The DIP switches connect to the system controller.

Most operating systems on the VGX reserve these switches for their use. Consult the operating system manual for details.

3.2.2 SW1: Reset Switch

Location on board: A6

SW1 is the reset button for the VGX. This switch issues a hardware reset to the PXA255 and system peripherals. Press this button to restart the VGX without cycling power. Most operating systems clear the contents of DRAM when a hardware reset occurs.

Pressing SW1 shorts the /RESET_IN signal (J9 pin 16) to ground. If your peripherals need to be reset when this button is pressed, use the /RESET_OUT signal on J9, pin 29. You can hold the VGX in reset by pressing and holding this button.

3.2.3 LED Indicators

The VGX has several onboard light-emitting diodes (LEDs) to indicate system operation. Some are software-controllable, while others indicate the status of specific functions.

Software-Controllable LEDs

Location on board: D6-D7

Three LEDs are controlled by the CPU (section 4.1.6) and are used to indicate boot and operating system status. These LEDs can often be used by applications to indicate operational status.

Signal Name	Designator	Color
LEDOUT0	*D9*	*Green*
LEDOUT1	*D8*	*Amber*
LEDOUT2	*D7*	*Red*

The LEDs are driven by the same buffers as the display driver data lines, so they will be off when the display buffers are disabled (see power management section 5.2.2).

Ethernet LEDs

Location on board: A7 (Ethernet socket J7)

Two LEDs integrated into Ethernet socket J7 indicate when a valid Ethernet connection has been made and when there is activity on the bus.

3.2.4 IrDA Transceiver

Location on board: D1-D2

U22 is an IrDA transceiver that converts Serial 2 electrical signals to infrared light pulses for IrDA communications. See section 4.5.1 for further details.

3.2.5 VR1: Vee Contrast Adjustment

Location on board: C7

Vee is the contrast adjustment voltage required for most passive LCD displays. VR1 and a PWM signal set the output voltage for Vee. See section 4.8.3 for further details.

3.3 Jumper Settings

Jumpers on the VGX select a variety of operational modes. All use 2mm shorting blocks (shunts) to select settings. Turn off power to the VGX before changing the position of a shunt.

The location indicated for each item refers to the grid diagram of the VGX in section 3.1.1

3.3.1 JP1: LCD Display Power

Type: 3-post header, 2mm
Location on board: A6

This jumper selects the supply voltage for the LCD display. The voltage selected here is passed to the *PNL_PWR* pins on J11 (3.4.9) and J19 (3.4.17).

Jumper setting	Voltage Selected
1-2	*Vddx (3.3 V)*
2-3	*Vcc (5.0 V)*

WARNING! Make sure you have selected the correct voltage before connecting the panel. Flat panels can be irreparably damaged by incorrect voltages.

IMPORTANT! This shunt is populated at the factory to match the voltage of the signal buffer circuits populated on the board. While the buffers may perform adequately at a different voltage than what was set at the factory, ADS cannot guarantee long-term performance.

Contact ADS Sales if your display requires a different display voltage than what is configured on standard production systems.

3.3.2 JP2: Source of 3.3 V Power (Vddx)

Type: 3-post header, 2mm
Location on board: A2

This jumper selects the source of 3.3 V power, Vddx, for the system. Standard production systems include an onboard 3.3 V regulator, but an external 3.3 V supply (+3.3V_IN from J2) can alternatively be used.

Jumper setting	Vddx is supplied by…
1-2	*external source*
2-3	*internal regulator*

3.3.3 JP3: LCD Display Data Voltage

Type: 3-post header, 2mm
Location on board: A6

This jumper selects the voltage for the data signals to the LCD display.

Important: These jumpers are set at the factory to match the panel and drivers shipped with the system. You may damage the panel or panel drivers if you change this jumper setting.

Tip: Most 5 V panels will run correctly with 3.3 V data.

Jumper setting	Data to display is…
1-2	*3.3 V (Vddx)*
2-3	*5.0 V (Vcc)*

3.3.4 JP4: Serial 2 Mode Select

Type: 2x9 header, unshrouded, 2mm
Location on board: B2

This header selects the communications mode of Serial Port 2 of the PXA255.

The operating system must configure the processor for the target serial mode. The table below lists the standard voltages to expect on the transmit line of the port when the transmitter is idle.

Important: When using Serial 2 as IrDA, make sure that the operating system configures the port as IrDA. Otherwise, the transmitter may be turned on continuously, which will drain significant amounts of power and may damage the IrDA transmitter.

Serial 2 Mode	JP4 Shunt Settings	Tx Vidle [6]
RS-232	*1-2, 3-4, 7-8, 9-10, 11-12, 13-14, 15-16, 17-18*	-6 V
3.3V logic	*1-3, 8-10 11-13,16-18*	3.3 V
IrDA[7]	*3-5, 6-8*	0 V

3.3.5 JP5: RS-485 Terminator

Type: 2-post header, 2mm
Location on board: B1

[6] Polarity and magnitude of idle voltages are listed. Actual voltages may vary.

[7] The IrDA transceiver is enabled with the IrDAOn signal from the system controller CPLD.

Install this jumper to make the VGX the last device in an RS-485 network. Shorting the pins of this header places a 120 Ω termination resistor across the RS-485 RX lines.

Jumper setting	RS-485 Terminator…
1-2	*installed*
n/c	*not installed*

3.3.6 JP6-7, JP10-13: Serial Port 1 Mode Select

Type: 3-post headers, 2mm
Location on board: B1-C2

Serial port 1 can be field-configured for operation in RS-232, RS-422 and RS-485 modes. It can also be factory-configured for J1708 or 3.3V logic operation in volume production.

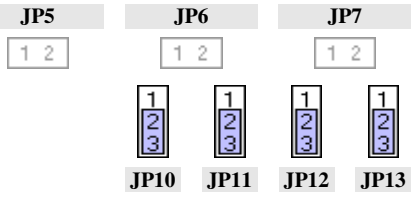
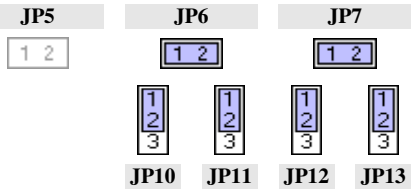
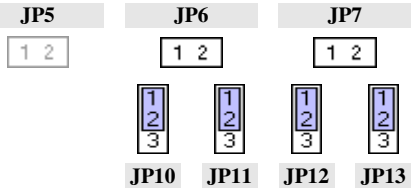
Jumpers JP6, JP7 and JP10 through JP13 select between RS-232 and RS-485/422 mode and set the duplex mode of RS-485/422.

RS-422 and RS-485 are differential serial protocols with the same voltage characteristics. RS-422 is a point-to-point protocol while RS-485 turns off the transmitter when not in use, allowing multi-drop installations. Each can be configured in half- or full-duplex mode. The Graphics Client Plus supports RS-422 by leaving the transmitter enabled all the time.

In half-duplex mode, TX+/RX+ and TX-/RX- are shorted together. Half-duplex devices can see their own transmissions. Connect to either the + or – connection on J7, but make sure to observe correct polarity.

You may find the following RS-485/422 signal locations helpful for diagnostic purposes: JP6.2 TX+; JP6.1 RX+; JP7.2 TX-; JP7.1 RX-; JP11.1 RX_enable; JP12.1 TX_enable.

Headers shaded gray in the following table are not relevant to the mode listed, but are shown for reference.

Mode	Jumper Setting
RS-232	
RS-485/422 Half Duplex (two-wire)	
RS-485/422 Full Duplex (four-wire)	

3.3.7 JP8: Future Use

Type: 2x4 header, 2mm
Location on board: B2-C2

3.3.8 JP9: Vee Polarity Select

Type: 3-post header, 2mm
Location on board: C6

This jumper selects the polarity of Vee, the contrast control voltage for passive LCD displays. Vee is controlled with a PWM signal from the ADSmartIO. See section 4.8.3 for further details

Jumper setting	Vee
1-2	*positive*
2-3	*negative*
n/c	*no Vee*

3.3.9 JP14: Source of Sleep Mode Power

Type: 3-post header, 2mm
Location on board: C6-C7

This jumper selects the source of power to back up the VGX when it is in sleep mode. See chapter 5 for further details.

Jumper setting	Voltage Selected
1-2	*Vperm (J2, pin 6)*
2-3	*Vcc (5.0 V)*

3.3.10 JP36: LCD UD Signal

Type: 2-post header, 2mm
Location on board: A6

This jumper determines the voltage for the PNL_UD signal on J11 and J19. On some active-matrix LCD displays, the PNL_UD signal flips the displayed image bottom-to-top.

Jumper setting	Connects UD to…
1-2	*GND*
n/c	*PNL_PWR*

3.3.11 JP37: LCD RL Signal

Type: 2-post header, 2mm
Location on board: A6

This jumper determines the voltage for the PNL_RL signal on J11 and J19. On some active-matrix LCD displays, the PNL_RL signal flips the displayed image right-to-left.

Jumper setting	Connects RL to…
1-2	*GND*
n/c	*PNL_PWR*

3.3.12 JP38: SM501 SSP Mode Select

Type: 3-post header, 2mm
Location on board: C2

This shunt supports the SM501 control of the SSP bus (4.5.2).

Jumper setting	Function
1-2	*(not supported)*
2-3	*SM501 is bus master*

3.4 Signal Headers

The following tables describe the electrical signals available on the connectors of the VGX. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions and references to related chapters.

The location indicated for each item refers to the grid diagram of the VGX in section 3.1.1 For details about how to determine pin numbers of a header, see section 3.1. For precision measurements of the location of the connectors on the VGX, refer to section 6.1.1.

Legend:

n/c	Not connected
GND	VGX ground plane
(3.3.9)	Reference section for signals

Signal Types

I	signal is an input to the system
O	signal is an output from the system
IO	signal may be input or output
P	power and ground
A	analog signal
OCI	open-collector/open-drain input
OC	open-collector/open-drain output

3.4.1 J1: USB Host Port

Board connector: USB Type A, Amp 787616-1

Location on board: A1

Connector J1 provides the signals for USB host connectivity. USB mice, keyboards and other USB function devices may be plugged in.

Pin	Name	Type	Description
1	*USB_M_VCC*	*PO*	*DC Power Input*
2	*USB_M_UDC-*	*IO*	*USB host +*
3	*USB_M_UDC+*	*IO*	*USB host -*
4	*GND*	*P*	*ground*

3.4.2 J2: Input Power Connector

Board Connector: 1x6 Molex #22-23-2061, 0.1 inch spacing

Recommended mating connector: Molex 22-01-3067

Location on board: A2

J2 supplies power to the VGX. +5V_IN is the main power supply, with a factory option to supply 3.3 V to the system, as well. See section 5.2.1 for an overview of how the VGX power supply is structured.

Pin	Name	Type	Description
1	*+5V_IN*	*PI*	*5V input power*
2	*GND_IN*	*PI*	*Ground*
3	*+3.3V_IN*	*PI*	*3.3V input power (optional)* [8]
4	*+12V_IN*	*PI*	*12V input power (backlight, 5.2.1)*
5	*POWERON*	*O*	*Output for power supply management (5.2.2)*
6	*VPERM*	*PI*	*"Permanent voltage" (5.2.1)*

3.4.3 J3: Backlight Inverter

Board Connector: Molex 53398-0790

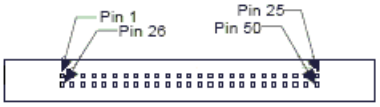
Recommended mating connector: Molex 51021-0700 or Quadrangle Products RT51021-0700-18

Location on board: A2-A3

See the "Brightness Control (Backlight)" paragraph in section 4.8.3 for additional details about these signals..

Pin	Name	Type	Description
1	*+12V*	*PO*	*Power supply for backlight inverter (also available on J15 pins 23 and 24)*
2			
3	*GND*	*P*	*ground*
4			
5	*BacklightOn*	*OC*	*On/off control for backlight inverter (also available on J15, pin 21)*
6	*BacklightPWM*	*AO*	*Brightness control for backlight inverter (also available on J15, pin 22)*
7	*GND*	*P*	*ground*

3.4.4 J4: CompactFlash / Expansion Bus



Board Connector : Samtec ASP-100925-01

Recommended Mating Connector: see text below
Recommended Board-to-Board Connector: none

Location on board: A3-A4

The VGX makes its CompactFlash bus signals (VGX "Card B") available on this header. These signals can be used to add a CompactFlash socket to a daughter board or to expand the capabilities of the VGX as a digital expansion bus. See section 4.1.5 for details.

Although the header included on the VGX does not include guide rails, you can plug a CompactFlash card directly onto this socket for testing purposes. The top of the card should face the PCMCIA header. Support the card mechanically to avoid bending the pins.

[8] The 3.3V power input is for cost-sensitive, volume production systems

The pins on PCMCIA and CompactFlash sockets are numbered down the length of the row as shown in the diagram above; this numbering is different from other sockets on the VGX. The signal names listed below are for the CF bus in I/O mode.[9]

Pin	Name	Type	Description
1	GND	P	ground
2	D3	IO	Data 3-7
3	D4	IO	
4	D5	IO	
5	D6	IO	
6	D7	IO	
7	/CE1	O	High Byte Chip Select
8	A10	O	Address 10
9	/OE	O	Memory Read
10	A9	O	Address 7-9
11	A8	O	
12	A7	O	
13	VCC	PI	External Switched CardB Power Input
14	A6	O	Address 0-6
15	A5	O	
16	A4	O	
17	A3	O	
18	A2	O	
19	A1	O	
20	A0	O	
21	D0	IO	Data0-2
22	D1	IO	
23	D2	IO	
24	/IOIS16	I	16 Bit Access
25	/CD2	I	Card Detect 2
26	/CD1	I	Card Detect 1
27	D11	IO	Data 11-15
28	D12	IO	
29	D13	IO	
30	D14	IO	
31	D15	IO	
32	/CE2	O	Low Byte Chip Select
33	/VS1	I	Voltage Sense 1 Input
34	/IORD	O	IO Read
35	/IOWR	O	IO Write
36	/WE (/MWR)	O	Memory Write
37	IRQ	I	Interrupt Signal
38	VCC	P	Card Power

[9] CompactFlash Association. "CF+ and CompactFlash Specification Revision 1.4," July 1999.

Pin	Name	Type	Description
39	/CARDSEL	O	Card Select
40	/VS2	I	Voltage Sense 2 Input
41	RESET	O	Reset
42	/WAIT	I	Wait
43	/INPACK	I	Interrupt Acknowledge
44	/REG	O	Register Access
45	SPKR	I/O	Speaker Input
46	/STSCHG	I/O	Status Change
47	D8	IO	Data 8-10
48	D9	IO	
49	D10	IO	
50	GND	P	ground

3.4.5 J7: Ethernet

Board Connector: RJ-45 with integrated magnetics and LEDs (Pulse J0026D21B)

Location on board: A7

Ethernet signals are also available for connection to an off-board socket on header J9. See section 4.5.4 for interface details.

3.4.6 J8: I/O, Analog Inputs, USB Function Port, I²C

Board Connector: 2x15 header, 2 mm spacing, Samtec STMM-115-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-115-02-F-D-500)

Location on board: A1-B1

Pin	Name	Pin	Type	Description		
1	GC_GPIO0		IO	Graphics controller digital I/Os (4.6.1, 6.2.9)		
3	GC_GPIO1		IO			
5	GC_GPIO2		IO			
7	GC_GPIO3		IO			
9	GC_GPIO4		IO			
	GC_GPIO9	2	IO			
	GC_GPIO8	4	IO			
	GC_GPIO7	6	IO			
	GC_GPIO6	8	IO			
	GC_GPIO5	10	IO			
11	ANIN0		AI	Analog input (4.6.2)		Factory option: SM501 Zoomed Video Port Signals 8..11
13	ANIN1		AI	PA5	Analog inputs (4.6.2)	
15	ANIN2		AI	PA6		
17	ANIN3		AI	PA7		
	I2C_SCL	12	IO	PC6	I²C Bus (4.5.6) (or ADSmartIO, 4.3.6)	
	I2C_SDA	14	IO	PC7		
	GC_GPIO10	16	IO	Graphics controller GPIO 10		
	CPLDIO0	18	IO	CPLD I/Os		
	CPLDIO1	20	IO			
	CPLDIO2	22	IO			
	/EXT_IRQ	24	I	External interrupt		

Pin	Name	Pin	Type	Description
19	*VPDATA12*			*SM501 Zoomed Video Port Signals*
21	*VPDATA13*			
23	*VPDATA14*			
25	*VPDATA15*			
	USB_VCC	*26*	*PI*	*USB function port, data (4.5.2)*
27	*USB_GND*		*P*	
	USB_UDC-	*28*	*IO*	
	USB_UDC+	*30*	*IO*	
29	*GND*		*P*	*ground*

3.4.7 J9: VGA Out, PS/2 Keyboard, Ethernet, System Reset

Board Connector: 2x15 header, 2 mm spacing, Samtec STMM-115-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-115-02-F-D-500)

Location on board: A2-B2

Pin	Name	Pin	Type	Description
1	*VCC*		*PO*	*5 V*
	VDDX	*2*	*PO*	*3.3 V*
3	*VGA_VSYNC*		*O*	*Analog Display Signals (4.8.4)*
	VGA_HSYNC	*4*	*O*	
5	*GND*		*P*	
	CRT_VCC	*6*	*PO*	
7	*GND*		*P*	
9	*GND*		*P*	
11	*GND*		*P*	
	VGA_BLUE	*8*	*O*	
	VGA_GREEN	*10*	*O*	
	VGA_RED	*12*	*O*	
13	*PS2_VCC*		*PO*	*PS/2 keyboard power (5 V, fused)*
	GND	*14*	*P*	*ground*
15	*/RQONOFF*		*OCI*	*"Request On/Off" Switch Input*
	/RESET_ BUTTON	*16*	*OCI*	*System reset*
17	*n/c*			
	ETH_LED1K	*18*		*External Ethernet LED1, cathode*
19	*ETH_TD+*		*O*	*Ethernet (J7, 4.5.4)*
	ETH_RD+	*20*	*I*	
21	*ETH_TD-*		*O*	
	ETH_RD-	*22*	*I*	
	ETH_LED2K	*24* [10]		*External Ethernet LED2, cathode*
25	*SIGPS2*		*IO*	*External PS/2 keyboard inputs*
	CLKPS2	*26*	*IO*	

Pin	Name	Pin	Type	Description
23 [10]	*SPI_CLK*		*IO*	*SPI Port (4.5.2)*
27	*SPI_RXD*		*I*	
	SPI_FRM	*28*	*IO*	
	SPI_TXD	*30*	*O*	
29 [10]	*/RESET_OUT*		*O*	*System reset output (3.2.2)*

3.4.8 J10: PCMCIA

Board connector: AMP 535655-2 (ejector hardware is a factory option)

Location on board: A3-D5

The 68-pin PCMCIA socket conforms to the PCMCIA standard, revision 2.1, for 5 V-tolerant Type II cards. The socket can also run at 3.3 V. The socket is normally de-energized; the operating system is responsible for turning on the socket when a card is inserted and turning it off when the card is removed.

Vpp (pins 18 and 52), which is 12 V in older PCMCIA implementations, is left unconnected in this implementation. See section 6.2.16 for electrical specifications.

3.4.9 J11: LCD Display (34-pin)

Board Connector: 2x17 header, 2mm spacing, STMM-117-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-117-02-F-D-500)

Location on board: A6-B6

The following table describes the signals on the LCD interface connector. Signal names shown are for TFT active matrix color LCDs at 16 bpp (bit-per-pixel). For other color depths and LCD technologies, consult the table in section 4.8.3. Signals from the XScale are buffered and EMI filtered before reaching J1. See section 4.8 for further details about displays.

Pin	PXA255 Signal Name	Color Active TFT Display at 16bpp	
		ADS Signal Name	Description
1		*PNL_VEE*	*V_{EE} (contrast); see JP9 (3.3.7)*
2		*GND*	*ground*
3	*L_PCLK*	*PNL_PIXCLK*	*Pixel Clock*
4	*L_LCLK*	*PNL_HSYNC*	*Horizontal Sync.*
5	*L_FCLK*	*PNL_VSYNC*	*Vertical Sync.*
6		*GND*	*ground*
7	*L_DD15*	*PNL_RED0*	*Red data*
8	*L_DD11*	*PNL_RED1*	
9	*L_DD12*	*PNL_RED2*	
10	*L_DD13*	*PNL_RED3*	
11	*L_DD14*	*PNL_RED4*	
12	*L_DD15*	*PNL_RED5*	
13		*GND*	*ground*

[10] Note that the listed signals are slightly out of numeric order to facilitate grouping of signals .

14	*L_DD5*	*PNL_GREEN0*	*Green data*
15	*L_DD6*	*PNL_GREEN1*	
16	*L_DD7*	*PNL_GREEN2*	
17	*L_DD8*	*PNL_GREEN3*	
18	*L_DD9*	*PNL_GREEN4*	
19	*L_DD10*	*PNL_GREEN5*	
20		*GND*	*ground*
21	*L_DD4*	*PNL_BLUE0*	*Blue data*
22	*L_DD0*	*PNL_BLUE1*	
23	*L_DD1*	*PNL_BLUE2*	
24	*L_DD2*	*PNL_BLUE3*	
25	*L_DD3*	*PNL_BLUE4*	
26	*L_DD4*	*PNL_BLUE5*	
27		*GND*	*ground*
28	*L_BIAS*	*PNL_LBIAS*	*Data enable*
29		*PNL_PWR*	*Vcc (5 V) or 3.3 V (JP1)*
30			
31		*PNL_RL*	*Horizontal Mode Select (set by JP37)*
32		*PNL_UD*	*Vertical Mode Select (set by JP36)*
33	*(CPLD)*	*PNL_ENA*	*Panel enable signal*
34		*VCON*	*low-voltage adjust for contrast control of some displays (6.2.4)*

3.4.10 J12: LCD Signals: LVDS

Board Connector: 2x10 header, 2 mm spacing, Molex 87331-2020.

Location on board: A7-B7

J12 supplies the LCD signals in LVDS format. The LCD signals on each differential pair are listed in the table below (data is clocked out MSB first but is listed LSB first below). Additional details about LVDS are listed in section 4.8.3.

Note: The LVDS signal mapping changed between revisions A and B of the VGX.

Pin	Name	Type	Description [Rev. A VGX]
1	*PNL_PWR*	*PO*	*Display power*
2			
3	*GND*	*P*	*ground*
4			
5	*RXIN0-*	*O*	*LVDS Data 0*
6	*RXIN0+*	*O*	*(R4, R0, R1, R2, R3, R4,G0)*
7	*GND*	*P*	*ground*
8	*RXIN1-*	*O*	*LVDS Data 1*
9	*RXIN1+*	*O*	*(G1, G2, G3, G4, G5 B4, B0)*
10	*GND*	*P*	*ground*
11	*RXIN2-*	*O*	*LVDS Data 2*
12	*RXIN2+*	*O*	*(B1, B2, B3, B4, HSYNC, VSYNC, DE)*
13	*GND*	*P*	*ground*
14	*CKIN-*	*O*	*LVDS Clock (PCLK)*
15	*CKIN+*	*O*	
16	*GND*	*P*	*ground*
17	*RXIN3-*	*O*	*Reserved for LVDS Data 3*
18	*RXIN3+*	*O*	
19	*GND*	*P*	*ground*
20			

3.4.11 J13: Serial 3

Board Connector: 2x5 header, 2mm spacing, Samtec STMM-105-01-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-105-02-F-D-500)

Location on board: B7-C7

Pin	Name	Type	Description
1	*DCD3*	*I*	*Data Carrier Detect*
2	*DSR3*	*I*	*Data Set Ready*
3	*RXD3*	*I*	*Receive data*
4	*RTS3*	*O*	*Ready To Send (or RTR Ready to Receive)*
5	*TXD3*	*O*	*Transmit data*
6	*CTS3*	*I*	*Clear To Send*
7	*DTR3*	*O*	*Data Terminal Ready*
8	*RIB3*	*I*	*Ring Indicator*
9	*GND_COM3*	*P*	*Serial 3 ground*
10	*n/c*	-	

3.4.12 J14: ADSmartIO, Serial 1 and 2, EIA-422/485, I/O

Board Connector: 2x20 header, 2 mm spacing, Samtec STMM-120-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-120-02-F-D-500)

Location on board: C1-D1

Pin	Name	Pin	Type	Description	
1	*ROW0*		*IO*	*PC0*	*ADSmartIO Keypad rows or digital I/O*
3	*ROW1*		*IO*	*PC1*	
5	*ROW2*		*IO*	*PC2*	
7	*ROW3*		*IO*	*PC3*	
9	*ROW4*		*IO*	*PC4*	
11	*ROW5*		*IO*	*PD5*	
13	*ROW6*		*IO*	*PD6*	
15	*ROW7*		*IO*	*PD7*	
	RXD2	*2*	*I*	*Serial 2, EIA-232*	
	TXD2	*4*	*O*		
	CTS2	*6*	*I*		
	RTS2	*8*	*O*		
	GNDCOM2	*10*	*P*		
	RXD1	*12*	*I*	*Serial 1 EIA-232 with 3.3 V logic factory option*	
	TXD1	*14*	*O*		
	CTS1	*16*	*I*		
	RTS1	*18*	*O*		
	GNDCOM1	*20*	*P*		
17	*COL0*		*IO*	*PA0*	*ADSmartIO Keypad columns or digital I/Os*
19	*COL1*		*IO*	*PA1*	
21	*COL2*		*IO*	*PA2*	
23	*COL3*		*IO*	*PA3*	
25	*COL4*		*IO*	*PA4*	
27	*COL5*		*IO*	*PD1*	
29	*COL6*		*IO*	*PB1*	
31	*COL7*		*IO*	*PD4*	
	RX422+	*22*	*I*	*Serial 1, EIA-422/485*	
	RX422-	*24*	*I*		
	TX422+	*26*	*O*		
	TX422-	*28*	*O*		
	GNDRS422	*30*	*P*		
	CPLDIO3	*32*	*IO*	*CPLD GPIOs (4.6.1)*	
	CPLDIO4	*34*	*IO*		
	CPLDIO5	*36*	*IO*		
	CPLDIO6	*38*	*IO*		
33	*VREF*		*AO*	*ADSmartIO A/D reference voltage*	
35	*VCC*		*PO*	*5 V*	
37	*VDDX*		*PO*	*3.3 V*	
39	*GND*		*P*	*ground*	
		40	*P*		

3.4.13 J15: Audio, Touch Panel, Backlight, CAN, Serial 3, IrDA, USB Host

Board Connector: 2x20 header, 2 mm spacing, Samtec STMM-120-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-120-02-F-D-500)

Location on board: C2-D2

Pin	Name	Pin	Type	Description		
1	CAN1HIGH		IO	CAN Bus 1 (4.5.5)		
	CAN1LOW	2	IO			
3	USB_M_VCC		PO	USB Host		
	USB_M_UDC-	4	IO			
5	USB_M_UDC+		IO			
	USB_M_GND	6	P			
				4-wire	5-wire	
7	TSPX		AIO	right	UL	Touch screen
	TSPY	8	AIO	bottom	UR	
9	TSMX		AIO	left	LL	
	TSMY	10	AIO	top	LR	
	WIPER	12	AI	n/a	WIPER	
11	GND		P	ground		
13	RIB3		I	Serial 3		
	DCD3	14	I			
15	TXD3		O			
	RXD3	16	I			
17	CTS3		I			
	RTS3	18	O			
19	DSR3		I			
	DTR3	20	O			
21	BacklightOn		O	Backlight on/off (4.8.3)		
	BacklightPWM	22	AO	Backlight intensity control (4.8.3)		
23	+12V		PO	12 V power for backlight from J2 (3.4.2)		
		24	PO			
25	SPKR+		AO	Stereo speaker, right channel		
	SPKR-	26	AO			
27	SPKL+		AO	Stereo speaker, left channel		
	SPKL-	28	AO			
29	GNDCOM3		P	Serial 3 ground		
	VCCTXIRDA	30	PO	IrDA (4.5.1)		
31	RXIRDA		I			
	TXIRDA	32	O			
33	VCCRXIRDA		PO			
	/IRDAON	34	O			
35	CAN2HIGH		IO	CAN Bus 2 (4.5.5)		
	CAN2LOW	36	IO			
37	MIC1_IN		AI	left	Stereo microphone input	
	MIC2_IN	38	AI	right		
39	AGND		AP	Analog ground		
		40	AP			

3.4.14 J16: Manufacturing Test Connector

Board Connector: 2x8 receptacle, 2mm spacing, Samtec SQT-108-01-L-D [11]

Location on board: C7

This header is used during manufacturing to program the boot flash, onboard logic and ADSmartIO firmware. These JTAG and SPI signals are intended only for factory use and are not otherwise supported. In the table below, pins are grouped by function.

Pin	Name	Pin	Type	Description
1	*TRST*			*JTAG*
	TMS	*2*	*I*	
	TDI	*4*	*I*	
5	*TCLK*			
	TDO	*8*	*O*	
9	*FWE*			
	FRDY	*10*		
	VDDX	*6*	*PO*	*3.3 V*
3	*GND*		*P*	*ground*
7	*GND*		*P*	
	VCC	*12*		*5 V*
11	*MISO*		*O*	*ADSmartIO SPI for in-system programming*
13	*SCLK*		*I*	
15	*PRG*		*I*	
	MOSI	*14*	*I*	
	GND	*16*	*P*	*ground*

3.4.15 J17: CAN Bus 1

Board Connector: 1x2 header, 0.1 inch spacing, Molex 22-23-2021

Recommended Mating Connector: Molex 22-01-3027

Location on board: D7

The signals for CAN bus 1 are also available on header J15.

Pin	Name	Type	Description
1	*CAN1HIGH*	*IO*	*CAN bus1 (4.5.5)*
2	*CAN1LOW*	*IO*	

[11] J16 changed from a 10-pin header to this 16-pin receptacle in revision A of the VGX.

3.4.16 J18: Touch Panel

Board Connector: 1x4 or 1x5 header, 0.100 inch spacing, Molex 22-23-2051(5-pin)

Recommended Mating Connector: Molex 22-01-3047

Location on board: D7

Pin	Name	Type	Description		
			4-wire	*5-wire*	
1	*TSMX*	*AIO*	*left*	*LL*	*Touch screen*
2	*TSPX*	*AIO*	*right*	*UL*	
3	*TSPY*	*AIO*	*bottom*	*UR*	
4	*TSMY*	*AIO*	*top*	*LR*	
5	*WIPER*	*AI*	*n/a*	*WIPER*	

3.4.17 J19: LCD Display (Hirose)

Board Connector: Hirose DF9B-31P-1V

Location on board: B6, underside of board

This header can be used to directly connect to some 16 bpp active Sharp TFT displays and products that are compatible with them. The signals on this connector are a subset of the signals on J11. See section 3.4.9 for more detailed descriptions of the signals.

Pin	Name	Pin	Type	Description
1	*GND*		*O*	*ground*
	PNL_PIXCLK	*2*	*O*	*Pixel clock*
3	*PNL_HSYNC*		*O*	*Horizontal sync*
	PNL_VSYNC	*4*	*O*	*Vertical sync*
5	*GND*		*O*	*ground*
	PNL_RED0	*6*	*O*	*Red data*
7	*PNL_RED1*		*O*	
	PNL_RED2	*8*	*O*	
9	*PNL_RED3*		*O*	
	PNL_RED4	*10*	*O*	
11	*PNL_RED5*		*O*	
	GND	*12*	*O*	*ground*
13	*PNL_GREEN0*		*O*	*Green data*
	PNL_GREEN1	*14*	*O*	
15	*PNL_GREEN2*		*O*	
	PNL_GREEN3	*16*	*O*	
17	*PNL_GREEN4*		*O*	
	PNL_GREEN5	*18*	*O*	
19	*GND*		*O*	*ground*
	PNL_BLUE0	*20*	*O*	*Blue data*
21	*PNL_BLUE1*		*O*	
	PNL_BLUE2	*22*	*O*	
23	*PNL_BLUE3*		*O*	
	PNL_BLUE4	*24*	*O*	
25	*PNL_BLUE5*		*O*	
	GND	*26*	*O*	*ground*
27	*PNL_LBIAS*		*O*	*Data enable*
	PNL_PWR	*28*	*O*	*Panel power (JP1)*
29			*O*	
	PNL_RL	*30*	*O*	*Right/left flip*
31	*PNL_UD*		*O*	*Up/down flip*

3.4.18 J20: CAN Bus 2

Board Connector: 1x2 header, 0.1 inch spacing, Molex 22-23-2021

Recommended Mating Connector: Molex 22-01-3027

Location on board: C7

The signals for CAN bus 2 are also available on header J15.

Pin	Name	Type	Description
1	*CAN2HIGH*	*IO*	*CAN Bus 2 (4.5.5)*
2	*CAN2LOW*	*IO*	

3.4.19 J40: Serial Ports A-D, MMC, RTC Battery, HP_IN

Board Connector: 2x25 header, 2 mm spacing, Samtec STMM-125-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-125-02-F-D-500)

Location on board: B6-D6

Pin	Name	Pin	Type	Description	
1	*DTRC*		*O*	*Serial C (4.5.1) (additional signals below)*	
3	*RIC*		*I*		
5	*DCDC*		*I*		
7	*DSRC*		*I*		
	DTRD	*2*	*O*	*Serial D (4.5.1) (additional signals below)*	
	RID	*4*	*I*		
	DCDD	*6*	*I*		
	DSRD	*8*	*I*		
9	*MMCDAT*		*IO*	*Data*	*Multimedia Card (MMC) Controller (0)*
	MMCCS1	*10*	*O*	*Chip select 1*	
11	*MMCCLK*		*O*	*Clock*	
	MMCCS0	*12*	*O*	*Chip select 0*	
13	*MMCCD*		*I*	*Card Detect*	
15	*MCCCMD*		*O*	*Command*	
	BATPOS	*14*	*PI*	*Real-time clock backup battery*	
	HP_IN	*16*	*I*	*Headphone connected*	
17	*VPDATA8*			*SM501 Zoomed Video Port Signals*	
	VPDATA9	*18*			
19	*VPDATA10*				
	VPDATA11	*20*			
21	*VPDATA12*				
	VPDATA13	*22*			
23	*RXDA*		*I*	*Serial A (4.5.1)*	
25	*TXDA*		*O*		
27	*CTSA*		*I*		
29	*RTSA*		*O*		
31	*DTRA*		*O*		
33	*DCDA*		*I*		
35	*DSRA*		*I*		
37	*RIA*		*I*		
39	*GNDCOMA*		*P*		
	RXDB	*24*	*I*	*Serial B (4.5.1)*	
	TXDB	*26*	*O*		
	CTSB	*28*	*I*		
	RTSB	*30*	*O*		
	DTRB	*32*	*O*		
	DCDB	*34*	*I*		
	DSRB	*36*	*I*		
	RIB	*38*	*I*		
	GNDCOMB	*40*	*P*		

Pin	Name	Pin	Type	Description
41	*RXDC*		*I*	*Serial C (4.5.1) (additional signals above)*
43	*TXDC*		*O*	
45	*CTSC*		*I*	
47	*RTSC*		*O*	
49	*GNDCOMC*		*P*	
	RXDD	*42*	*I*	*Serial D (4.5.1) (additional signals above)*
	TXDD	*44*	*O*	
	CTSD	*46*	*I*	
	RTSD	*48*	*O*	
	GNDCOMD	*50*	*P*	

4 Feature Reference

This chapter provides details about the architecture and many features of the VGX, and how they can fit together to create a system that meets your application needs.

4.1 System Architecture

4.1.1 Boot Code

The VGX uses the first block of onboard flash to store the boot code. At the factory, boot code is loaded using the JTAG interface (J6, section 3.4.10). Most ADS VGX boot loaders are field-upgradeable using a flash card on either the CompactFlash or PCMCIA port.

4.1.2 Synchronous DRAM

One bank of synchronous DRAM (SDRAM) can be populated for a system total of 16, 32, 64 or 128 MiB of RAM[12]. The data bus width is 32 bit.

The memory clock speed is one half the CPU core clock speed. Typical memory bus operation is at 99.5 MHz.

The self-refreshed RAM consumes most of the system sleep current. Sleep current increases in direct proportion to the amount of RAM installed.

4.1.3 Non-Volatile Memory

There are several ways to store data on the VGX that will survive a power failure. Some devices can only be accessed through operating system drivers, and not all are available for application data storage.

Flash Memory

Flash memory is the primary site for non-volatile data storage. The VGX includes a bank of flash memory for non-volatile data storage. The board supports 8, 16 or 32 MiB of installed flash. The data bus width is 32 bit.

ADS systems store the operating system, applications and system configuration settings in the onboard flash. Most operating systems configure a portion of the flash as a flash disk, which acts like a hard disk drive.

ADSmartIO EEPROM

The ADSmartIO controller includes 256 bytes or more of EEPROM storage. ADS reserves a portion of this memory for future use. Drivers may not be available for all operating systems.

CompactFlash and PCMCIA/ATA Cards

CF and ATA cards provide removable storage in a wide variety of capacities. These cards can be cost-effective means to expand system storage capacity for applications that provide access to the PCMCIA and CF slots.

SD/MMC Cards

If your application includes a socket Secure Digital and Multimedia cards and your operating system supports them, you can use these cards for mass storage. See section 0for details about using SD/MMC.

---

[12] 128 MiB SDRAM was not yet commercially available as of April 2003.

RTC NVRAM

The real-time clock chip includes 56 bytes of non-volatile RAM. The RAM is maintained as long as main or backup power is provided to the chip. Built-in drivers may not be available to access this feature, but the RAM can be accessed using the I^2C driver. Contact ADS Sales if your application requires this feature.

4.1.4 Interrupts

The VGX includes several sources for external interrupts. The following table summarizes the external interrupt sources and the devices to which they are connected.

Interrupt Signal	Pin	IRQ Handler
/RqOnOff	*J9.15*	*PXA255, GP 0*
/EXT_IRQ	*J8.24*	*Controller CPLD*
CARDBIRQ	*J4.37*	*PCMCIA CPLD*
XScale GPIOs [13]	*varied*	*XScale CPU*

Your operating system may not include drivers for all interrupt sources.

4.1.5 CompactFlash / Expansion Bus

The VGX makes its CompactFlash bus signals available on J4 (3.4.4). These signals can be used to add a CompactFlash socket to a daughter board or to expand the capabilities of the VGX as a digital expansion bus. The voltage of the bus signals is fixed at 3.3 V. Electrical specifications are listed in section 6.2.16.

ADS document number 640111-8000 (available on the ADS Support Forums) is the schematic for the Bitsy Personality Board design, which illustrates how to use the CF bus either as a CompactFlash socket or for an Ethernet controller. Additional documents are available on the ADS support web site (section 2.4) that illustrate how to use the CF bus.

4.1.6 PXA255 GPIO Cross-Reference

The following table describes how the VGX utilizes the XScale GPIO lines (*GPn*). They are offered for reference purposes only. Most operating systems make this information transparent to developers.

GP	Signal Name	Type	Function (connector, section)
0	*WAKE_UP*	*I*	*Wakeup from ADSmartIO and debounced RqOnOff (6.2.1)*
1	*IRQ_CPLD*	*I*	*CPLD interrupt*
2	*CTS2*	*O*	*Serial 2 CTS (4.5.1)*
3	*USB_DET*	*I*	*USB function port, detect connection*
4	*IRQ_TS*	*I*	*Touch panel interrupt*
5	*USB_RECONN*	*O*	*USB function port, disconnect/reconnect*
6	*MMCCLK*	*O*	*MMC clock (J7, 0)*
7	*CARDAVS1*	*I*	*PCMCIA Voltage Sense 1*
8	*MMCCS0*	*O*	*MMC chip select 0 (J7, 0)*
9	*MMCCS1*	*O*	*MMC chip select 1 (J7, 0)*
10	*CARDAVS2*	*I*	*PCMCIA Voltage Sense 2*
11	*CARDBVS1*	*I*	*CompactFlash Voltage Sense 1*

[13] Important! The PXA255 has restrictive constraints concerning timing of successive interrupts. While you may configure one or more XScale GPIOs as interrupt sources, it's possible to create a condition under which interrupts in rapid succession can cause the processor to lock up.

GP	Signal Name	Type	Function (connector, section)
12	MMCCD	O	MMC card detect (J7, 0)
13	IRQ_USB	I	USB interrupt
14	CARDAVS2	I	CompactFlash Voltage Sense 2
15	/CS1	O	Asynchronous flash chip select
16	VEEPWM	O	PWM0 control of Vee voltage
17	PXAPWM1	O	PWM1 backlight brightness control
18	RDY	O	Variable latency access CPU ready
19	LED1	O	Onboard LED outputs
20	LED0	O	
21	LED2	O	
22	n/c		unused
23	SCLK-C	O	SPI to touch panel controller
24	SFRM-C	O	
25	TXD-C	O	
26	RXD-C	I	
27	GPIO27	O	Reset ADSmartIO controller
28	BITCLK		AC '97 Codec
29	SDATA_IN		
30	SDATA_OUT		
31	SYNC		
32	RTS2	O	Serial 2 RTS (4.5.1)
33	/CS_GC	O	Graphics controller chip select
34	FF_RXD	I	Full-featured UART (J13, J15, 4.5.1)
35	FF_CTS	I	
36	FF_DCD	I	
37	FF_DSR	I	
38	FF_RI	I	
39	FF_TXD	O	
40	FF_DTR	O	
41	FF_RTS	O	
42	BT_RXD	I	Bluetooth UART (J14, 4.5.1)
43	BT_TXD	O	
44	BT_CTS	I	
45	BT_RTS	O	
46	IR_RXD	I	Infrared/Serial 2 (J14, J15, 4.5.1)
47	IR_TXD	O	
48	/POE		PCMCIA/CF Card interface
49	/PWE		
50	/PIOR		
51	/PIOW		
52	/PCE1		
53	/PCE2		
54	PSKTSEL		
55	/PREG		
56	/PWAIT		
57	/IOIS16		

GP	Signal Name	Type	Function (connector, section)
58	L_DD0	O	LCD display (4.8, J11, J19)
59	L_DD1	O	
60	L_DD2	O	
61	L_DD3	O	
62	L_DD4	O	
63	L_DD5	O	
64	L_DD6	O	
65	L_DD7	O	
66	L_DD8	O	
67	L_DD9	O	
68	L_DD10	O	
69	L_DD11	O	
70	L_DD12	O	
71	L_DD13	O	
72	L_DD14	O	
73	L_DD15	O	
74	L_FCLK	O	
75	L_LCLK	O	
76	L_PCLK	O	
77	L_BIAS	O	
78	CS2	O	Controller CPLD chip select
79	CS3	O	USB chip select
80	CS4	O	Ethernet chip select

4.2 Real-Time Clock (RTC)

The VGX uses the DS1307 real-time clock chip to maintain the system date and time when the system is powered down.

The operating system typically reads the RTC on boot and wakeup, and sets the RTC when the system time or date is changed. The system communicates with the RTC on the I^2C bus (section 4.5.6).

The RTC is powered by a long-life 3 V battery. As a factory option, the battery can be removed from the VGX and the RTC can be powered via the BATPOS input on J40 pin 14. See section 6.2.2 for electrical specifications.

4.3 ADSmartIO

ADSmartIO™ is a RISC microcontroller on the VGX that is programmed with ADS firmware. This device provides additional I/O functionality for specialized tasks. Your application software can configure the standard ADSmartIO for a variety of functions, such as digital I/O, PWM, A/D, I^2C, keypad scan and PS/2 keyboard operation.

4.3.1 Overview

The ADSmartIO controller has four, eight-pin I/O ports named PA, PB, PC and PD. Some of these ports' pins are used internally, while others are available for user applications. See the signal cross-reference in section 4.3.6 for details.

Generally, ADSmartIO ports are referenced by port and pin number (e.g. PA2), but I/O signals may go by several names based on its functionality. See the connector pinouts to cross-reference ADSmartIO signal names.

Electrical specifications for the ADSmartIO are listed in section 6.2.4. The *ADSmartIO Programmer's Reference* (ADS document 110110-4004) gives information about how to use the ADSmartIO features.

4.3.2 ADSmartIO Features

The following are some of the functions that the ADSmartIO can perform. The functions actually implemented depend on the firmware loaded on your system:

- General purpose digital I/O and A/D
- Keypad scan (section 4.3.5)
- PS/2 keyboard input
- Backlight on/off and brightness control (section 4.8.3)
- Contrast control for display (enabled only when pixel clock is running) (section 4.8.3)
- Read/set real-time clock (RTC) (section 4.2)
- Wakeup via RQONOFF signal (section 5.2.3)
- Monitor system power
- Reset CPU

4.3.3 Digital I/Os

All available ports on the ADSmartIO controller can be individually configured as inputs or outputs. If you write a "1" to an I/O port when it is configured as an input, it enables a pull-up resistor. Electrical specifications are listed in section 6.2.4.

4.3.4 Analog Inputs (A/D)

Each of the Port A I/Os (PA0-PA7) includes an analog-to-digital (A/D) converter. The converters give full-scale readings when the voltage at the pin is equal to voltage reference Vref (e.g. V=Vref•reading/1023). Not all ports are available for external A/D use; see section 4.3.6 for port assignments. The A/D inputs on the VGX go through voltage dividers before reaching the pins. See the electrical specifications listed in section 6.2.6 for details.

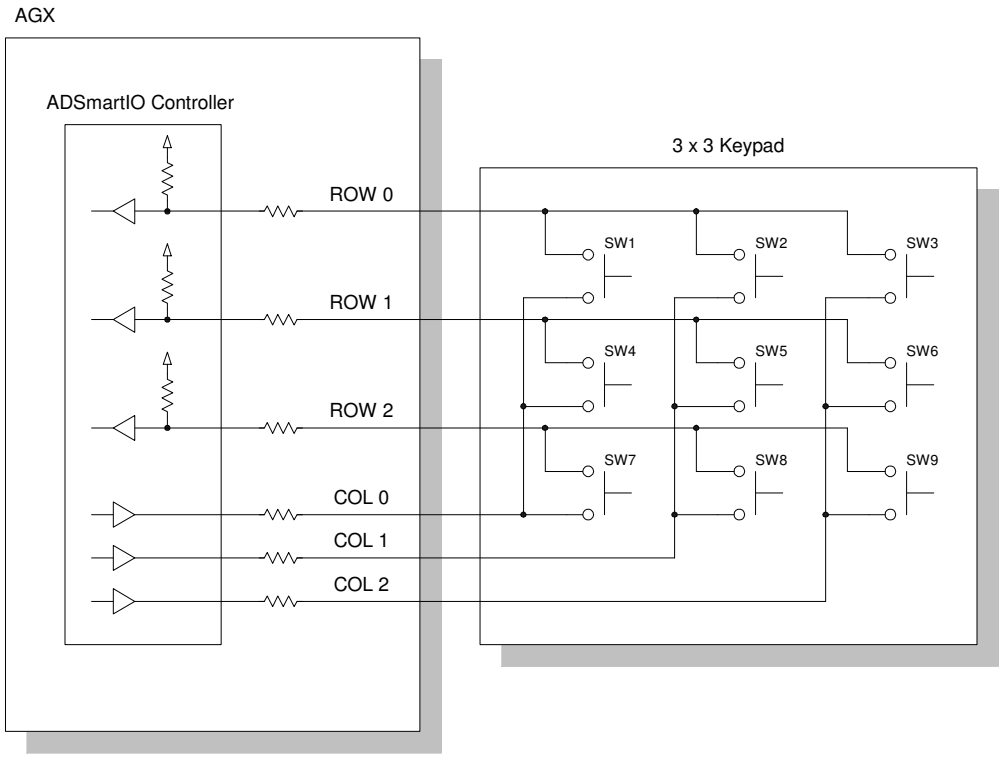
4.3.5 Keypad Scan

The ADSmartIO can scan a matrix keypad up to four by five keys in size. Matrix keypads are simpler and cost less than full keyboards and can be easily customized for your application. You can also create a keypad matrix from a collection of normally-open switches.

When configured to scan a keypad, the ADSmartIO configures the ROWn lines as inputs with software pull-ups enabled and configures the COLn lines as outputs set to "1"(high). For the scan, the keypad scanner sets successive COLn outputs to "0"(low), then looks for a "0" on one of the ROWn inputs. The scanner re-reads the pressed key after a delay to debounce the key press.

Unused row and column lines can be used for general purpose I/O or A/D.

The following diagram illustrates how to connect a 3x3 keypad matrix. The pull-ups are the software-activated internal resistors of the ADSmartIO, while the series resistors are part of the VGX.



4.3.6 ADSmartIO Signal Cross-Reference

The ADSmartIO microcontroller serves many functions in the VGX. The following table illustrates how the microcontroller ports are utilized for ADSmartIO functionality on the VGX.

Entries in parentheses indicate indirect connections to the listed pin (e.g. through voltage dividers or additional circuits). Signals with conventional protection circuits are considered directly connected. I=input, O=output.

Port	Pin	Type	Function
PA0	*J14.17*	*IO*	*Keypad, A/D or digital I/O*
PA1	*J14.19*	*IO*	
PA2	*J14.21*	*IO*	
PA3	*J14.23*	*IO*	
PA4	*J14.25*	*IO*	
PA5	*J8.13*	*AI*	*Analog inputs (ANIN1-3)*
PA6	*J8.15*	*AI*	
PA7	*J8.17*	*AI*	

Port	Pin	Type	Function	
PB0	*J9.25*	*O*	*PS/2 Data*	
PB1	*J14.29*	*IO*	*Keypad column or digital I/O*	
PB2	-	*O*	*Wake up CPU*	
PB3	-	*O*	*IRQ to CPU*	
PB4	-		*SFRM*	*SPI communication with controller CPLD*
PB5	-		*RX (MOSI)*	
PB6	-		*TX (MISO)*	
PB7	-		*CLK*	
PC0	*J14.1*	*IO*	*Keypad rows or digital I/O*	
PC1	*J14.3*	*IO*		
PC2	*J14.5*	*IO*		
PC3	*J14.7*	*IO*		
PC4	*J14.9*	*IO*		
PC5	-	*I*	*Pixel clock*	
PC6	*J8.12*	*IO*	*I^2C* [14]	
PC7	*J8.14*	*IO*		
PD0	-	*O*	*Passive panel enable (PNL_ENA)*	
PD1	*J14.27*	*IO*	*Keypad column or digital I/O*	
PD2	-	*I*	*Power enable from system*	
PD3	*J9.26*	*IO*	*PS/2 Clock*	
PD4	*J14.31*	*IO*	*Keypad column or digital I/O*	
PD5	*J14.11*	*IO*	*Keypad rows or digital I/Os*	
PD6	*J14.13*	*IO*		
PD7	*J14.15*	*IO*		

4.4 Audio

The VGX includes an AC '97 codec for stereo audio input and output. Electrical specifications for the audio system are listed in section 6.2.11.

4.4.1 Microphone Pre-amps

The VGX supports the connection of a stereo electret microphone to the MIC_R and MIC_L inputs on J5. The audio signals run through pre-amplifiers that low-pass filter and boost the signal before being passed on to the audio codec.

When connecting external electret microphones to the VGX, use the MIC_GND analog ground plane for improved signal-to-noise ratio. The VGX includes pull-ups to power electret microphones.

4.4.2 Audio Outputs: Speakers and Headphones

The VGX audio amplifier supports both differential and single-ended output devices. Differential (or "bridge") drive delivers greater output power and is suitable for speakers, which can be wired independently from each other. Single-ended mode is used for devices like headphones, which have a common ground between output channels.

[14] PC6 and PC7 are used for the I^2C bus master interface. See section 4.5.6 for details. These pins can be reconfigured as digital I/Os for custom production applications.

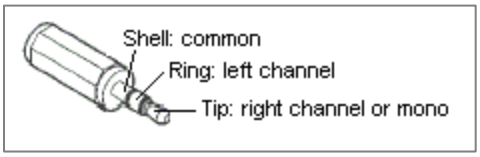
The HP_IN input (J14.16) determines the output mode of the amplifier: When HP_IN is high, the audio output drive is single-ended, when HP_IN is low, the output drive is differential. An on-board pull-up normally keeps HP_IN high.

Connecting Speakers

When using the VGX to drive speakers, short the HP_IN signal to ground. This places the output amplifier in differential mode. Connect speakers to the SPKR_L and SPKR_R outputs on J10.

Connecting Headphones

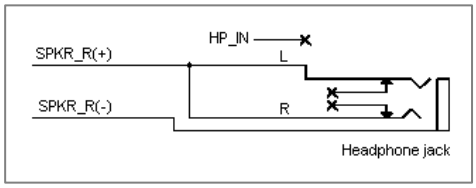
Standard headphones use a plug wired as shown at right. Three rings on the plug provide right and left channels and a common return. Mono headphones do not include the center ring.



The mating headphone jacks include spring contacts to make an electrical connection with the headphone and to mechanically hold the plug in place. Some jacks include a mechanical switch suitable for use with the HP_IN signal that is activated when a plug is inserted into the jack.

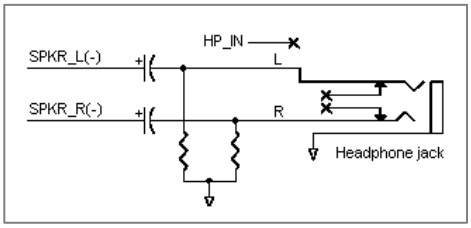
Mono Headphones

You can connect mono headphones directly to the VGX as shown at right. Keep in mind that the resulting impedance of the parallel-connected headphone speakers is half that of a single headphone speaker. See the audio driver specifications in section 6.2.11 for details about the minimum impedance an audio output channel can drive.



Stereo Headphones

When wiring for stereo headphones, wire blocking capacitors in series with the VGX SPKR- signals as shown at right. These capacitors block the DC component of the audio signal and complete the conversion from differential to single-ended output drive. Leave the HP_IN signal pulled high to enable headphone output.

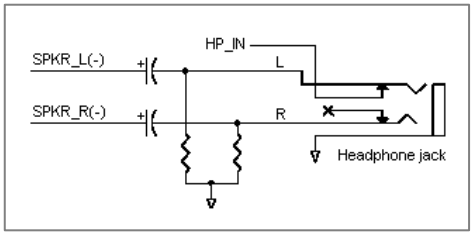


Select blocking capacitor size based on the lowest frequency your application will need to play out. Larger capacitors give improved bass response (lower frequency cutoff), but are physically larger and cost more. The corner frequency for the low-pass filter created by the capacitor and the headphone speaker is calculated as $fo=1/(2\pi R_L C)$. A 330 uF capacitor into a 32 ohm headphone speaker will give a low cutoff frequency of 15 Hz. Use electrolytic capacitors rated for at least 6.3 V.

The pull-down resistors shown in the diagram drain any charge that builds up on the headphone outputs when headphones are not connected. Use 1 kΩ resistors.

Using Stereo Headphones and Speakers in the Same System

Some applications use both headphones and speakers. You can wire the headphone jack to automatically switch the amplifier to single-ended mode when a headphone plug is inserted in the jack. This will disable the drive to any speakers that are wired into the system.



Most headphone jacks include mechanical switches that indicate when a headphone plug has been inserted. The diagram at right shows a circuit that pulls down the HP_IN signal when a headphone plug is removed.

For this circuit to work reliably in differential mode, the HP_IN signal must remain below V_{HP_IN} through the largest output voltage swings of SPKR_L. Use of 1 kΩ resistors meets this requirement.

4.5 Data Communications

The VGX has several built-in channels for communication with peripheral and peer devices. These include EIA/TIA-232, -422 and -485; J1708; logic-level serial; IrDA; USB host and client USB ports; Ethernet; CAN bus and I^2C.

4.5.1 Serial Ports

The VGX has seven serial ports: three from the XScale processor and four from a quad UART. The serial ports can be configured as follows:

Port	# signals	Headers	Standard	Factory options
1	5	J14, JP5-7, JP10-13	EIA/TIA-232, EIA/TIA-422/485	J1708, 3.3 V logic
2	5	JP4, J14, J15, U22	EIA/TIA-232, IrDA, 3.3 V logic	header for IrDA
3	9	J13, J15	EIA/TIA-232	3.3 V logic
A & B	9	J40	EIA/TIA-232	3.3 V logic
C & D	9	J40	3.3 V logic	(none)

XScale UART

The XScale processor supplies three standard serial ports. The "Bluetooth UART" is Serial 1 on the VGX; the "IrDA UART" is VGX Serial 2; and the "Full-featured" UART" is VGX Serial 3.

The Serial 2 IrDA signals are on J15. When Serial 2 is operated in IrDA mode, the serial driver should enable the IrDA transmitter with IrDAOn signal. The IrDA transceiver is normally mounted on the board (3.2.4), but as a factory option, a header can replace the transceiver for cabling to another location. Electrical specifications are listed in section 6.2.8.

The Serial 2 CTS and RTS serial handshaking signals are XScale GPIO lines that must be controlled by the software drivers when Serial 2 is operated as EIA/TIA-232 or 3.3 V logic.

Ports that are configured for 3.3 V logic operation connect directly to the XScale and should be treated electrically as GPIOs. See section 6.2.14 for GPIO electrical specifications and 6.2.8 for serial port specifications.

Quad UART

VGX includes a UART with four, full-featured ports. The ports are factory-configured for either EIA/TIA-232 or 3.3 V logic operation.

Ports that are configured for 3.3 V logic operation connect directly to the UART and should be treated carefully. See section 6.2.8 for serial port electrical specifications.

4.5.2 SSP/SPI Port

The VGX acts as master on a number of internal and external SSP/SPI buses. The following table describes how the buses are used on standard production VGX systems:

SSP Bus	Use on VGX
PXA255 SSP	*Touch panel controller*
PXA255 NSSP	*AVR ADSmartIO controller*
SM501 SSP0	*External SSP (J9)*

External SSP Port (SM501)

The SM501 controller drives the SSP signals available for user applications. The signals are located on header J9 (3.4.7). See section 6.2.9 for electrical specifications.

Factory Options

If your production VGX system will not have the SM501 populated, or if you have special SSP needs, please contact ADS Sales to discuss your application needs. The VGX has a variety of options for routing system SSP signals to the external header.

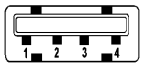
4.5.3 USB

The VGX includes signals for USB 1.1 Host and Function ports. The USB Host (downstream) signals are on socket J1 and header J15 and are controlled by the SM501; the USB Function signals are on header J8 and are connected to the PXA255.

To create a USB connection, you must wire a standard USB socket as described in the following sections. For each type of connector, pin numbering is as follows:

Pin	USB signal
1	*USB_PWR*
2	*USB -*
3	*USB +*
4	*GND*

USB Host Port



The VGX USB Host port allows you to connect one USB device to the VGX. USB mouse and keyboard are the most common client devices, but you can connect any USB function device that has USB drivers installed on the VGX.

The VGX includes Type A USB connector J1 for the host signals. You can also wire your own USB connector using the signals on J15 (section 3.4.13). The mating face of such a socket is shown at left. The USB standard also permits directly wiring the USB signals to the target USB device (e.g. USB mouse). To connect more than one USB client device to the VGX, use a USB hub.

The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The VGX supplies 5 V power through the USB_PWR pin. Make sure to account for power used through USB in your VGX power budget (section 5.3.1). Electrical specifications are in section 6.2.9.

USB Function Port

The VGX includes a USB Function (or "Client") port. This interface allows the VGX to appear as a client device to USB Host devices such as desktop and laptop computers.

The USB Function signals are available on connector J8 (section 3.4.6). Connect these signals to a USB client Type B socket (mating face shown at left). The USB standard also permits directly wiring the USB signals to the host or to a host connector (e.g. USB mouse).

The VGX supports the full USB connection speed (12 Mbit/s). It indicates this to the host device with a 1.5 kΩ pull-up on the USB+ signal.

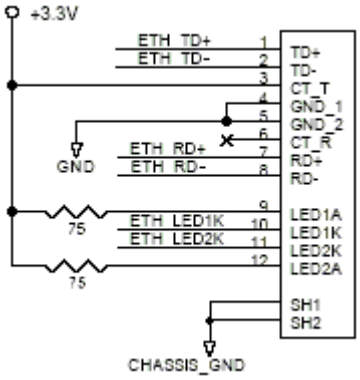
USB_VCC is power supplied from the host computer. Since the VGX is self-powered (not powered by the USB host), USB_VCC is not needed as a power input. However, USB_VCC tells the VGX when a USB cable is connected, so include it when connecting the USB signals to the VGX.

The VGX includes the capability to simulate a Function port cable disconnection. This feature can be used to force the host to re-enumerate the VGX (e.g. after wakeup).

4.5.4 Ethernet

The VGX includes a 10/100 BT Ethernet controller with an RJ-45 socket (J7).

The Ethernet signals are available on header J9 (3.4.7) for connection to an off-board socket. The diagram at the right illustrates how to connect the Ethernet signals to an RJ-45 socket like the one used on the VGX. You may also use separate transformer, socket and LEDs if desired. See the Bitsy Personality Board for a design example.



Ethernet details and electrical specifications are listed in section 6.2.11.

4.5.5 CAN Bus

CAN bus (Controller Area Network) is a protocol developed for the automotive industry that is increasingly being used in industrial control and automation applications. The VGX includes a CAN controller suitable for connection to a wide range of CAN networks.

The CAN signals are available on headers J15 (3.4.13), J17 (3.4.15) and J20 (3.4.18). Details and electrical specifications are listed in section 6.2.12.

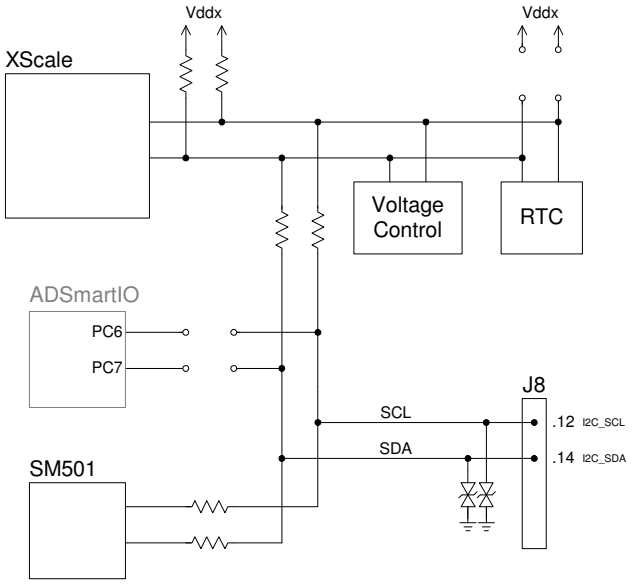
4.5.6 I²C Bus Master

I²C (Inter-IC) Bus is a multi-master, "two-wire" synchronous serial bus developed by Philips for communications between integrated circuits (ICs). The bus master addresses devices using the data line and provides a synchronous clock for reading and writing devices. Client devices respond only when queried by the master device. Philips has developed many I²C devices, but other organizations (e.g. Maxim) have adopted I²C as a convenient means for addressing peripherals in a system.

I²C on the VGX

The VGX uses the XScale I²C interface to communicate with the real-time clock (section 4.2) and the CPU core voltage controller. Applications can also use I²C to communicate with external peripherals.

The following diagram illustrates the I²C architecture on VGX. Parts are shown populated as they are found on standard production systems.



XScale I²C

The XScale typically controls all I²C peripherals on the VGX. Its I²C signals are routed to header J8 via low-impedance resistors. Specifications are listed in section 6.2.17.

SM501 I²C

As a factory option for volume production, the SM501 I²C controller could be used to control off-board peripherals. Contact ADS Sales if your application requires this feature.

ADSmartIO I²C

As a factory option in volume production, the ADSmartIO controller could be connected to the output pins as illustrated in the diagram to supply two additional GPIOs Electrical specifications are listed in section 6.2.6.

I²C Device Addresses

The following are the bus addresses of the I²C devices included on standard VGX systems:

0x20	Voltage controller
0x68	Real-time clock

Select I²C devices with addresses that will not conflict with the onboard devices. Onboard devices are typically controlled by operating system drivers and should not be addressed directly.

4.5.7 Multimedia Card (MMC) Controller

The XScale MMC controller provides a serial interface to MMC cards. Contact ADS Sales if your application requires Secure Digital or MMC functionality.

4.6 Discrete IOs

This section summarizes the discrete signals on the VGX that can be used for measurement or control.

4.6.1 Digital IOs

The ADSmartIO, system controller and SM501 display controller supply discrete digital I/Os on the VGX. Each discrete digital signal can be configured as an input or an output.

The ADSmartIO digital I/Os are available on header J14 (3.4.12) and are described in section 4.3.3.

The seven system controller digital I/Os (*CPLDIOn*) are available on headers J8 (3.4.6) and J14 (3.4.12). See section 6.2.7 for electrical specifications.

When installed, the SM501 display controller supplies the digital I/Os available on header J8 (3.4.6). See section 6.2.9 for electrical specifications.

4.6.2 Analog Inputs

The inputs on the ADSmartIO controller can be configured as analog inputs. These are known as ANIN1 to ANIN3 on header J8 (3.4.6). See ADSmartIO section 4.3.4 for details.

In addition, one input on the touch panel controller can also be used as an analog input. This signal is called ANIN0 and is found on header J8 (3.4.6).

4.6.3 Analog Outputs (PWM)

The VGX has two analog outputs. These are used to control LCD backlighting and contrast (section 4.8.3).

4.7 Touch Panel

The VGX supports four and five-wire analog resistive touch panels. Five-wire panels are a factory option. Connect the touch panel to the inputs on connector J3. The touch panel controller can wake the system from sleep (section 5.2.4) Electrical details are listed in section 6.2.5.

4.8 Display Controller

Standard production VGX systems use the Silicon Motion SM501 graphics accelerator, but the VGX can be factory configured to use the XScale display controller. This section describes both controllers and the VGX subsystems they use in common.

4.8.1 The XScale Display Controller

The XScale controller uses system memory for the display frame buffer. It can drive VGA (640x480) and SVGA (800x600) displays easily. Larger displays will work with the XScale, with some constraints imposed by the controller architecture. The ADS Support Forums provide details about the design tradeoffs that are required to support larger displays.[15]

Key features of the XScale controller include

- Frame buffer is in system DRAM
- Dual 16 x 8-byte display data FIFOs

See section 6.1.4 for additional implications of depopulating the SM501 display controller.

4.8.2 The SM501 Display Controller

The Silicon Motion SM501 graphics accelerator has its own internal frame buffer, which reduces the load on the system bus for displays with larger dimensions and higher refresh rates. The controller also features graphics acceleration and support for a variety of display types.

You can determine if your VGX has the SM501 populated by looking at the top of the board. The SM501 is a large, square IC located within the frame of the PCMCIA ejector. The reference designator is U62.

Features of the controller include:

- Internal frame buffer RAM
- 2D display engine (accelerator)
- Digital LCD or analog VGA outputs
- Hardware display rotation
- Dual and Virtual display support
- Hardware cursor (mouse)
- General-purpose digital I/Os

Additional factory options include:

- TV input (NTSC/PAL, Composite/S-Video) using external Zoomed Video Port converter
- USB Host
- Additional SPI port

Standard production systems make use of the basic features of the display controller. Contact ADS Sales if your application requires use of the advanced or factory option features of this controller. Electrical specifications for the controller are listed in section 6.2.9.

4.8.3 Using the LCD Display Signals

This section describes the features of the VGX used to control LCD displays. LCD display signals are found on headers J3 (3.4.3), J11 (3.4.9), J12 (3.4.10), J15 (3.4.13) and J19 (3.4.17).

[15] At the time of writing, posted at http://www.applieddata.net/forums/topic.asp?topic_id=580

Panel Voltages

The VGX supplies 3.3 V or 5 V power to the LCD display. Select this voltage with JP1 (3.3.1). Please observe the cautions listed with the JP1 settings.

LCD Signals

The LCD signals are driven by either the XScale or the SM501 controller. The signals are named using the XScale conventions (L_DDn). *L_DD0* through *L_DD15*—as well as the pixel clock, vertical sync and horizontal sync—are all buffered at a factory-set voltage. See section 6.2.4 for full specifications.

The *PNL_RL* and *PNL_UD* signals are for active (TFT) displays that support changing the scan direction. This feature allows the display to be flipped right-to-left (*RL*) or up-and-down (*UD*) by changing the voltage on these signals. See section 6.2.4 for full specifications.

Creating LCD Display Cables

ADS has designed cables for a wide variety of displays. See the list of supported displays on the ADS support forums. Cable drawings for supported displays are available on request.

LVDS for LCD Displays

The VGX includes an LVDS (Low-Voltage Differential Signaling) driver suitable for driving some LCD displays. LVDS multiplexes digital signals together onto differential pairs. LVDS has the advantage of using fewer wires, longer cable lengths and lower radiated noise.

LVDS signals are available on header J12. The table in section 3.4.10 illustrates how the display signals are multiplexed onto the LVDS differential pairs.

Electrical specifications for the LVDS transmitter are provided in section 6.2.4.

Brightness Control (Backlight)

Most LCD displays include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Some LCDs, such as passive transflective displays, can be viewed in daylight without backlighting.

Panel backlights are driven by backlight inverters. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. Fortunately, most backlight inverters include control signals to dim and turn off the backlight.

The VGX supplies two signals for backlight control: BacklightPWM and /BacklightOn. The signals are found on both J3 and J15. BacklightPWM is a filtered PWM signal from the PXA255 that supplies an analog output voltage to control the intensity of the backlight. The /BacklightOn signal is an open-collector output to turn the backlight on and off. See section 6.2.4 for electrical specifications.

Contrast Control (Vee and Vcon)

Vee and Vcon are used to control the contrast of passive panels. Many passive panels require a positive or negative bias voltage in the range of fifteen to thirty volts to bias the passive LCD display.

Some displays include a Vee generator and simply require a low-voltage analog signal to control the contrast. The Vcon output is a PWM-controlled output that can be used for this purpose. Electrical specifications for Vee and Vcon are listed in section 6.2.4.

4.8.4 Using Analog Displays

The VGX SM501 display controller supports VGA output with the signals on header J9 (3.4.7). These signals are mapped as follows:

J9 Pin	Signal Name	Analog VGA Connection
3	*VGA_VSYNC*	*Vertical retrace*
4	*VGA_HSYNC*	*Horiz. retrace*
6	*CRT_VCC*	
8	*VGA_BLUE*	*Blue*
10	*VGA_GREEN*	*Green*
12	*VGA_RED*	*Red*
5, 7, 9, 11	*GND*	*Ground*

4.8.5 Developing Display Drivers

ADS provides display timings for supported displays on request. For displays not yet supported, ADS has a panel configuration service to creates panel timings and cable drawings. Contact ADS Sales for further details.

4.9 EMI/RFI and ESD Protection

The VGX board incorporates a number of standard features that protect it from electrostatic discharge (ESD) and suppress electromagnetic and radio-frequency interference (EMI/RFI). Transient voltage suppressors, EMI fences, filters on I/O lines and termination of high-frequency signals are included standard on all systems. For details, see electrical specifications for subsystems of interest.

4.9.1 Agency Certifications

Many products using ADS single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. Because ADS supplies only the single-board computer and not fully integrated systems, ADS cannot provide meaningful system-level emissions test results.

The crystal frequencies (section 6.2.15) and electrical specifications listed in Chapter 6 may provide helpful information for agency certifications.

4.9.2 Protecting the Power Supply Inputs

It is the responsibility of the designer or integrator to provide surge protection on the input power lines. This is especially important if the power supply wires will be subject to EMI/RFI or ESD.

5 Power and Power Management

Power management is especially critical in portable and handheld applications where battery power is at a premium. The VGX includes advanced power management features, including the low power XScale CPU and partitioned power distribution. The VGX can also operate as a conventional single-board computer, taking advantage of the inherently low power consumption of the system.

This chapter describes the architecture of the VGX power supply, factors affecting power consumption and reference designs to get you started. For information about how much power the VGX consumes, consult the electrical specifications in section 6.2.3.

5.1 Power Management Modes

Most handheld and portable systems available today never really turn "off." They make use of power management algorithms that cycle the electronics into "standby" and "sleep" modes, but never fully remove power from the full system.

This section describes the various power management modes of the XScale processor and how the VGX makes use of them.

5.1.1 XScale Power Management Modes

The XScale PXA255 processor supports four operational modes: Turbo, Run, Idle, and Sleep.

- Sleep mode uses the least amount of electrical power. The processor core is powered off and only a few processor peripherals (RTC, I/Os and interrupt control) remain active. The transition back to Run mode may take a few hundred milliseconds, as clocks must stabilize and hardware that was powered off must be reinitialized.
- Idle mode reduces power consumption by pausing the processor core clock. Processor peripherals remain enabled. This mode is used for brief periods of inactivity and offers a quick transition back to Run mode.
- Run mode is the typical mode used when applications are running. It offers the best MIPS/mW (performance vs. power) performance when running applications from RAM.
- Turbo mode runs the processor core at up to three times the Run mode speed. Since external memory fetches are still performed at the memory bus frequency, Turbo mode is best used when running the application entirely from cache.

5.1.2 Power Management on the VGX

The VGX can actively be configured to be in XScale Run, Turbo or Sleep modes. Idle mode is controlled by the operating system or application and is typically transparent to the application.

In Turbo, Run and Idle modes, the power supplies are in their standard, full-power state and applications run normally on the system. Specific subsystems (as described in section 5.2.2) may be selectively disabled to conserve power during these states. The operating system is responsible for adjusting the core voltage (Vddi) for optimal power consumption in each mode.

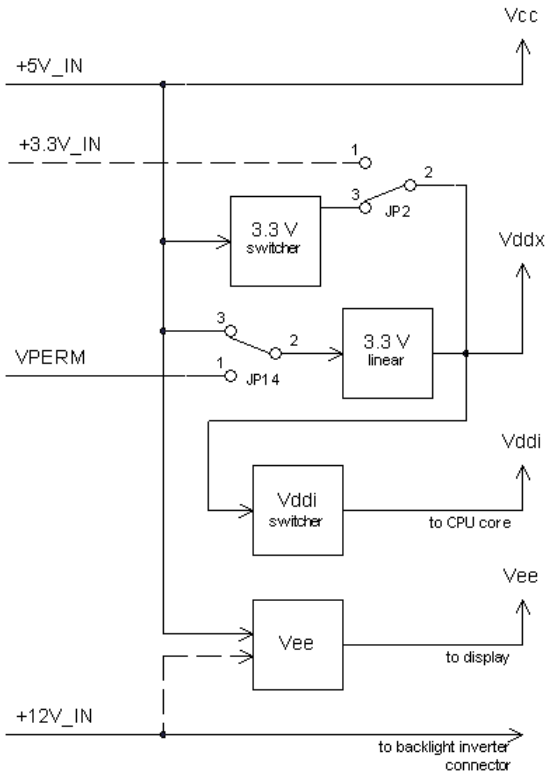
In Sleep mode, sometimes called "Suspend" mode, the processor puts the SDRAM in a low-power, self-refresh mode, the processor core shuts off, most peripheral sub-systems are shut down and the power supplies drop into low-power states or turn off entirely (see the diagram in section 5.2.2 for details). In this state, the VGX consumes very little power, most of which is dedicated to the maintenance of the RAM (see section 6.2.3 for specifications). The system can be "awakened" and returned to the Run state by initiating a system wakeup using one of the methods described in section 5.2.3.

5.2 Architectural Overview and Power Management Features

This section provides an overview of the architecture of the VGX power supply and a description of the various features of the VGX power management systems.

5.2.1 Power Supply Architecture

The VGX power supply is organized as shown in the following diagram.



Vddi is a variable-voltage power supply controlled by the XScale I^2C bus (4.5.6, 6.2.2). This voltage scaling feature allows the operating system to manage power consumption over the full range of CPU clock rates.

Factory options available are indicated by dashed lines in the diagram above. The options shown are available for production customers, but are outside the scope of this manual. Contact your ADS sales representative if you believe one or more of these options is required for your application.

Specifications for the VGX power supply are listed in section 6.2.2.

5.2.2 Subsystem Partitioning

The VGX can selectively turn off power to subsystems on the board. This load-shedding feature can extend battery life. Applications and the operating system determines how selective power management is utilized.

VGX systems that can be selectively disabled include the following:

- LCD display (panel power and signal buffers)
- Display controller (if installed)
- Backlight
- Vee (contrast)
- Audio codec and microphone pre-amps
- Audio output amplifier
- Serial A, B and 3
- IrDA transceiver

In addition, the VGX also controls its core power supplies to support sleep operation:

- Vddx (3.3 V)
- Vddi (processor core)

5.2.3 System Sleep

This section describes several methods for putting the system into Sleep mode. Section 5.2.4 describes how to return the system to its operating state.

RQOnOff Input

Operating systems and applications can configure the /RQONOFF signal (J9.15) to put the system to sleep. In conjunction with the wakeup function (section 5.2.4, below), the RQONOFF input can be used as an "on/off" button for some systems. Electrical specifications are listed in section 6.2.1.

Software Control

Applications can put the system to sleep programmatically. Operating systems may also put the system to sleep if the system has not been used for a certain amount of time or for other reasons. In remote, battery-powered applications, software Sleep can be used in conjunction with the Timed Wakeup feature (section 5.2.4) for minimum power consumption.

5.2.4 System Wakeup

This section describes several mechanisms for waking an VGX system that has been placed in Sleep mode (section 5.2.3). The system will resume operation in Run mode unless the power supply voltage is lower than Vsleep (section 6.2.1). If the input voltage is too low, the system will not wake under any circumstances. This protects the RAM from getting corrupted by an undervoltage condition.

RQOnOff Input

Shorting the /RQONOFF signal (section 5.2.3 above) to ground will wake the system. The signal is connected to the system controller. Electrical specifications are listed in section 6.2.7.

[18] The controller inverts the PowerEnable signal for use with some subsystems. This details is not shown in the diagram.

Touch Panel

The touch panel controller interrupts the processor when touch panel events occur. Before going to sleep, the processor can place the controller in a low-power sleep mode. When a touch event occurs, the controller still generates an interrupt, which can wake the system.

Timed Wakeup

The XScale can wake up at a predetermined time. This feature is controlled by software.

ADSmartIO

The ADSmartIO controller controls the wakeup signal to the XScale. For production applications, ADS can configure the ADSmartIO to wake up the system on specific events. Contact ADS Sales if your application requires a special wakeup event.

5.2.5 Backlight Power

The VGX provides software control of Backlight Intensity and On/Off. Power for the backlight is routed through the board from header J2. This provides the greater flexibility when selecting backlight inverters for an application. See section 4.8.3 for further details about backlight control.

5.2.6 Power Supply Efficiency

The VGX power supply achieves high efficiency through several means. First, it utilizes high-efficiency switching regulators. These regulators use conventional step-down switchers under operating load conditions, but are configured by the system for linear and "burst" mode[19] operation during low-load conditions that occur during system sleep. Additionally, there is only one level of cascaded regulation, reducing the losses that multiply through each stage.

5.3 Designing for Optimal Power Management

Designing a system for optimal power management requires careful attention to many details. This section provides some guidelines and tips for best power management.

5.3.1 Create a Power Budget for Peripherals

Embedded system designers using the VGX should have a clear understanding of how power usage will be allocated in the system they design. Designers should create a power budget that takes into account the types of devices that are expected to be used with the VGX.

The following lists detail some of the typical external loads that can be placed the VGX power supplies. Baseline power consumption of the VGX is listed in section 6.2.3.

3.3 V Loads

Typical external loads on the 3.3 V power supply include the following:

- Display
- Personality Board
- CF and some PCMCIA cards

[19] "Burst mode" in this context is a registered trademark of Linear Technology Corporation

5 V Loads

5 V loads come from both onboard and external devices. Typical loads include the following:

External:

- Display
- Many PCMCIA cards
- USB devices
- PS/2 keyboard
- Speaker(s)
  Assume 80% efficiency

Onboard:

- 3.3 V Supply
  Multiply by 115% to account for 3.3 V power supply efficiency

Loads on Main Supply

The main 5 V power supply is loaded by the and 3.3 V supplies as indicated in the diagram of section 5.2.1. Assume 85% efficiency for external loads that cascade through the 5 V supply. Consider these loads when creating your power budget.

5.3.2 Power Loads During Sleep

When designing systems for minimal power consumption during Sleep mode, make sure to consider DC losses to external connections. The following are a few of the ways your system may "leak" when asleep:

- PCMCIA and CF cards
  Cards in place when the system is asleep can drain power through the Card Detect and Voltage Sense lines. Assume that all four lines ground the VGX PCMCIA pull-ups (section 6.2.16) while the card is inserted.
- Digital I/Os
  Review digital I/O connections for potential voltage differences from external connections when the VGX is asleep.
- USB
  Depending on how USB devices are powered and how the operating system handles USB, USB devices may draw power during Sleep.

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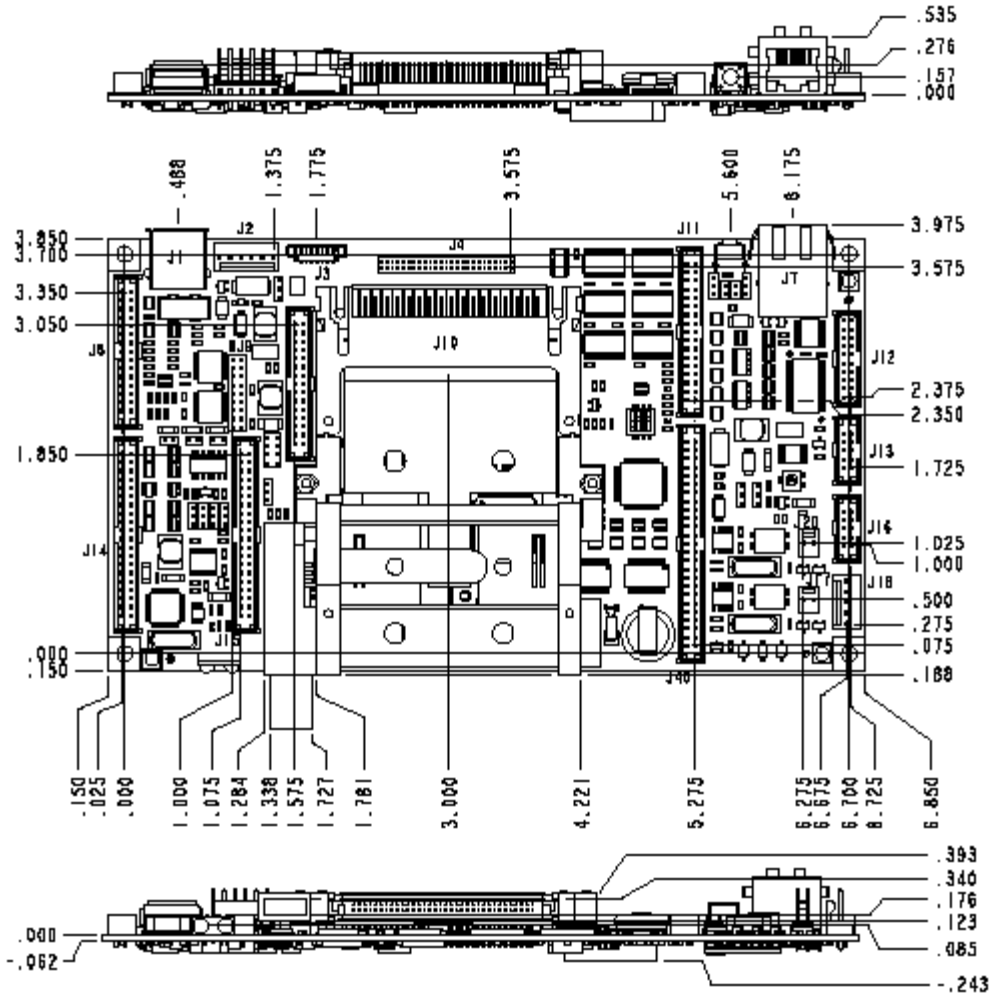
6 System Specifications

6.1 Mechanical Specifications

The VGX is 4.0 inches by 7.0 inches in size. This section describes the component dimensions and mounting of the board. Detailed drawings are available on the support forums (section 2.4), and 3D models are available from ADS in electronic format for production customers.

6.1.1 Mechanical Drawing

The following mechanical drawing specifies the dimensions of the VGX, as well as locations of key components on the board. The PCMCIA ejector can be detached from the board header and is a factory option. All dimensions are in inches. This image is an excerpt from the full mechanical drawings, ADS document number 630116-20002.



6.1.2 Mounting Holes

Four holes are provided, one on each corner, for mounting. The diameter of the holes is 0.138-in. Mounting holes are plated through and connected to the VGX ground plane.

For reliable ground connections, use locking washers (star or split) when securing a VGX in an enclosure. Make sure that washers do not extend beyond the limits of the pads provided.

6.1.3 Clearances

The VGX has a low profile. It can fit in an enclosure with inside dimensions as thin as 0.878 inch (22.3 mm). Key clearances are as follows:

- Highest component: 0.535 inch (16.6 mm), top
  0.181 inch (4.6 mm), bottom
- Board thickness: 0.062 inch (1.57 mm)
- Clearance over top and bottom: 0.05 inch (1.3 mm), each

Note: Selection of connectors and wiring harnesses will determine height of final assembly.

6.1.4 Production Options

The VGX has a number of production options detailed throughout this manual. This section describes options that most significantly affect the mechanical design of the board. These options are generally available only for volume production orders.

Installation of PCMCIA Ejector

Systems can be shipped with a PCMCIA ejector.

Mating Headers on Underside of Board

Through-hold signal headers can be mounted on the underside of the VGX. This allows the VGX to sit on top of another board.

Note that special configuration charges may apply for the creation of alternate test fixtures.

Important! When the headers are placed on the underside of the board, the pin numbers will not correspond to the signals as described in this manual. Lay out the mating board with this in mind.

Connector Plating

ADS can populate headers with other platings as required.

Remove SM501 Display Controller

VGX systems can be produced without the SM501 display controller (4.8). However, there are a number of features that the SM501 provides that will also be lost:

- Accelerated graphics and other SM501 display controller features
- USB Host
- SSP

There are two other ADS products that may fit your needs if your application does not require two CAN controllers.:

1. Consider using the AGX product if your application requires USB Host functionality
2. Consider the GCX product if you do not need USB Host.

Contact ADS Sales for recommendations of other ADS products that may meet your application requirements.

6.2 Electrical Specifications

6.2.1 Reset, Sleep, Wakeup, Temperature

Absolute Maximum Ratings

Reset Input (RESET_IN)..... 3.6 V (note 1)

Symbol	Parameter	Min	Typ.	Max	Units
Temperature					
Trun	operating temperature	-40		+85	°C
Reset_In (J10.45)					
Vrst	trigger voltage (Note 2)		2.7		V
Vprst	pull-up voltage		Vddx		V
Rprst	pull-up resistance		47		kΩ
Sleep (5.2.3)					
Vsleep	Sleep trigger voltage (Note 3)	5.4		5.8	V
Vsleep,hyst	Sleep trigger release hysteresis (Note 4)	0.06		0.25	V
Wakeup: RqOnOff (5.2.5)					
trq	wakeup pulse duration (Note 5)	100			ms
Vprq	pull-up voltage		Vddx		V
Rprq	pull-up resistance		47		kΩ
Vih,max	maximum input voltage			3.3	V
Vil	trigger voltage			0.9	V

Notes:

1. The reset controller can support operating voltages up to 10 VDC. However, such high voltages on Vddx through the pull-up resistor may damage the system.
2. Short /Reset_In to GND to reset system
3. This is the voltage at VBATT_POS at which the DC_GOOD signal (4.3.6) changes from high to low, which can trigger the system to go into Sleep mode. Sleep trigger at DCIN_POS is Vsleep+Vdin (6.2.2).
4. **Important!** Once Vsleep has been triggered, the input voltage must rise at least Vsleep,hyst above Vsleep before the voltage detector will restore the DC_GOOD signal. Make sure that your input voltage is designed to always run above Vsleep+Vsleep,hyst, or systems that go to sleep may not be able to wake again.
5. Short /RqOnOff to GND to for at least trq to wake up system. A low-level voltage on /RqOnOff initiates wakeup.

6.2.2 Power Supply

The VGX is powered from a 5 V DC supply and generates additional voltages for onboard logic. The 5 V and 3.3 V supplies are available on the VGX output connectors and are limited to the current draws specified below.

The system time is maintained by a DS1307 real-time clock and powered by a long-life battery (Panasonic BR1225-1HC or equivalent; located at D5-D6 on the top side of the VGX).

Symbol	Parameter		Min	Typ.	Max	Units
System Power						
5V_IN	5.0 V power input		4.75	5.0	5.25	V
VDDI	Processor core voltage (6.2.14)		0.85	1.0	1.3	V
VDDX	3.3 V onboard supply	Run	3.1	3.3	3.5	V
		Sleep		3.15		V
I (Vddx)	3.3 V available for display, PCMCIA, external peripherals, etc. (Note 6)	Run			700	mA
		Sleep			100	mA
I (Vcc)	5 V available for display and external peripherals (note 7)				1000	mA
RTC Backup Power (4.2)						
V BATPOS	real-time clock battery backup		2.2	3.0	3.6	V
I BATPOS	RTC current (note 8)			300	500	nA

Notes:

6. During Sleep mode, Vddx is powered by a linear regulator, which draws from the 5V supply.
7. In addition to the external 5V_IN power supply, the 5 V output is limited by the trace widths on the printed wiring board.
8. Vddx=0V, Vbatpos=3.2 V (source: DS1307 data sheet)

6.2.3 Power Consumption

The following table lists ***preliminary*** power consumption for the VGX with varying activity levels.

Power consumption varies based on peripheral connections, components populated on the system and the LCD panel connected. Input voltage, temperature and the level of processor activity affect power consumption to a lesser extent.

LCD displays and backlights add significantly to the total power consumption of a system. ADS development systems include the Sharp LQ64D343 5V TFT VGA display, which draws about one watt, and the Xentek LS520 backlight inverter, which draws about six watts at full intensity.

Symbol	Parameter	Min	Typ.	Max	Units
P sleep	Sleep mode power		50		mW
P idle	Idle mode power (note 9)		2		W
P run	Run mode power (note 10)			3	W

Notes: Power consumption was measured on a fully populated 64 MiB VGX with no peripheral connections under the following conditions:

9. System running only the Windows CE desktop (predominantly in Idle mode; <5% CPU utilization)
10. Full (95-100%) processor utilization in Run mode achieved by using Ethernet heavily and running multiple instances of a graphical application under Windows CE.

6.2.4 Display

LCD display panels have a wide range of voltage and data requirements. The VGX has a number of adjustable voltages to support these requirements, as well as controls for brightness (backlight) and contrast (passive panels only). See section 4.8 for further details.

Standard production VGXs use the SM501 graphics accelerator. See section 6.2.9 for SM501 specifications.

Symbol	Parameter	Min	Typ.	Max	Units
LCD (4.8.3)					
V pnl	LCD voltage (note 11)	3.3		5.0	V
P pnl_pwr	LCD power (note 12)			2	W
V pnl_data	LCD data voltage (note 13)	3.3	3.3	5.0	V
Scan Direction (active displays) (3.3.10, 3.3.11, 4.8.4)					
R pnl_scan	Pull-up resistance		4.7		kΩ
V pnl_scan	Pull-up voltage	0	V pnl	V pnl	V
Contrast Control (passive displays) (3.2.5, 3.3.7, 4.8.3, note 14)					
Vee(-)	Contrast adjust, R_L=5kΩ, JP9: 1-2	-30		-15	V
Vee(+)	Contrast adjust, R_L=5kΩ, JP9: 2-3	15		30	V
Vcon	Low-voltage contrast adjust (note 14)	0		0.75	V
Brightness Control (backlight, 4.8.3)					
R backlightOn	Pull-up		10		kΩ
V backlightOn	With pull-up (note 15)			12	V
	No pull-up (factory option, note 16)			30	V
V backlightPWM	PWM (note 17)	0		5	V
R backlightPWM	PWM series resistance (note 18)		2.2		kΩ

Notes:

11. Jumper JP1 (3.3.1) selects the display voltage.
12. Total power available depends on system power budget.
13. Systems are configured at the factory with buffers for 3.3 or 5 V panel data. Jumper JP3 (3.3.3) selects the voltage for those buffers. 5 V displays with Vih <= 0.6•Vpnl_pwr (3.0 V) will work reliably with 3.3 V data. 3.3 V buffers can be run at 5 V for test purposes, but if your application requires 5 V data, contact ADS Sales to ensure the correct buffers are used for your display.
14. Vcon is the filtered, low-voltage PWM signal used to control Vee. It can be used directly with some passive displays to control contrast. Vcon and Vee are controlled by PXA255 PWM0. Vcon is the 3.3 V PWM signal RC filtered with a 25% (20k/6.8kΩ)voltage divider.
15. The "12 V" voltage is supplied at power header J2, pin 4. The BacklightOn signal is an open-collector output managed by the system controller CPLD.
16. As a factory option, the pull-up resistor can be removed for use with an external pull-up resistor. The maximum voltage rating of the transistor is listed.
17. The standard configuration for BacklightPWM signal is as an open collector output with a 5 V pull-up. The output can also be factory configured as 5 or 12 V open collector or 3.3 V, push-pull CMOS output, with or without an output filter capacitor. The "12 V" voltage is supplied at power header J2, pin 4.
18. The backlight PWM output is driven by PXA255 PWM1.

6.2.5 Touch Panel Controller

The VGX uses touch panel controllers from Burr Brown. It uses the ADS7846 to support four-wire analog-resistive touch panels and the ADS7845 to support five-wire panels. The system is factory-configured for use with four-wire panels. All touch-panel signals are ESD and RF protected. The touch panel controller is powered during sleep mode and can generate an interrupt to wake the system.

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	Supply voltage		Vddx		V
	A/D sample resolution		12		bit

6.2.6 ADSmartIO Controller

The ADSmartIO Controller is a second RISC microcontroller on the VGX designed to handle I/O functions autonomously. The VGX communicates with the ADSmartIO controller via the system controller CPLD. On the VGX, ADSmartIO is implemented with the Atmel AVR 8535 microcontroller, which has 512 bytes EEPROM.

Absolute Maximum Ratings

Input voltage, any pin .....3.8 V

Input voltage, A/D inputs PA5-PA7 (note 23) .....15 V

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	ADSmartIO supply voltage		3.3		V
Rs	Series resistance (note 19)		1		kΩ
Vprot	(note 19)				V
Digital Outputs (4.3.3)					
Vol				0.5	V
Voh		2.3	3.3		V
I sink	(see notes 19, 20)			20	mA
I source	(see notes 19, 20)			12	mA
Digital Inputs (4.3.3)					
Vih		0.6			Vdd
Vil				0.3	Vdd
R	Software-selectable pull-ups to 3.3 V (see note 21)	35		120	kΩ
A/D Inputs (4.3.4)					
n	resolution (note 22)		8	10	bit
Rin	input impedance (note 23)		43.2		kΩ
Vin	A/D input voltage range (note 23)	0		10.8	V
Vref	A/D reference voltage (note 24)		2.5		V
Ivref	Current drain from ref voltage			100	uA
I (Vref)	J10.43			100	µA
I2C Bus (4.5.6, note 25)					
	Bus clock		50		kHz
	input buffer size			32	byte
	packet size			32	byte
Vi/o	I/O voltages	see digital I/Os, above			V
Rbus	pull-up on SDA, SCK		4.7		kΩ
Vbus			3.3		V

Notes:

19. Row and column I/Os have series resistance and overvoltage protection to ground. The series resistance limits the dc current that any one pin can source or sink.
20. I^2C outputs PC6 and PC7 are directly connected to I/O controller without external protection.
21. Control pull-up resistors by writing to bits of IO port when the port is configured as a digital input (bit mask 1=enable, 0=disable).
22. Digital noise on the board may degrade analog performance under some conditions.

23. ADSmartIO A/D inputs include an input voltage divider of 33.2k series with 10k to ground.
24. Vref is usually turned off when the system is in Sleep mode (section 5.2.2).
25. Specifications based on ADSmartIO release 1010 rev 2 (ADS release #700114-10102)

6.2.7 System Controller

A Xilinx XCR3256XL CPLD on the VGX provides system logic for chip selects, power management, interrupt decoding, clock generation, PCMCIA logic and other system control functions. It is programmed at the factory using the JTAG interface (3.4.14).

Absolute Maximum Ratings

Input voltage, digital I/O pins..... -0.5 to 5.5 V [tbd]

Output current, continuous,
digital I/O pins ..... -100 to 100 mA [tbd]

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	Supply voltage		3.3		V
Digital Outputs					
Vol	[tbd]	0		0.4	V
Voh		2.4			V
Digital Inputs					
Vil	[tbd]	0		0.8	V
Vih		2.0		3.5	V

6.2.8 Serial Ports

The VGX supports several serial ports as described in section 4.5.1.

Serial ports 1 through 3 are controlled by the XScale processor. Serial ports A through D are controlled by an Exar ST16C554 or compatible quad UART.

EIA-232 signals are generated using charge pump devices (e.g. Sipex SP3232 and SP3243). Signals 422/485/J1708 are buffered with the Maxim MAX491. IrDA signals from the XScale are converted to IrDA using a Vishay TFDU6100 infrared transceiver.

Symbol	Parameter	Min	Typ.	Max	Units
	Logic voltage, serial ports		3.3		V
IrDA (4.5.1)					
VccRxIrda	Receiver voltage		3.3		V
RvccRxIrda	Reciever power series resistance		10		Ω
VccTxIrda	Transmitter voltage		3.3		V
RvccTxIrda	Transmitter power series resistance		3.6		Ω
PtxIrda	Transmitter power		330	630	mA

6.2.9 Silicon Motion SM501

The Silicon Motion SM501 is a graphics controller that includes support for USB Host and SSP functions. The VGX also brings out the SM501s general purpose IOs (GPIOs) for application use.

Symbol	Parameter	Min	Typ.	Max	Units
Digital I/Os (J8, 3.4.6; 4.6.1; note 26)					
Voh	High-level output voltage				V
Vol	Low-level output voltage		[tbd]		V
I gc_io	Sink/Source current				mA
USB Host (4.5.3)					
SSP (4.5.2.)					
	Base bit rate, internal clock				MHz
	Divisor for Internal clock				
	Clock rate, external source				MHz

Notes:

26. These digital I/Os are available only if the SM501 display controller is installed.

6.2.10 USB

The VGX supports USB operation as described in section 4.5.3. See section 6.2.14 (PXA255) for USB function port specifications and section 6.2.9 (SM501) for USB host specifications.

6.2.11 Ethernet

The VGX uses an SMSC LAN91C111 10/100 BT Ethernet controller. The MAC (Media Access Control) address is stored in a serial EPROM connected to the controller.

6.2.12 CAN Bus

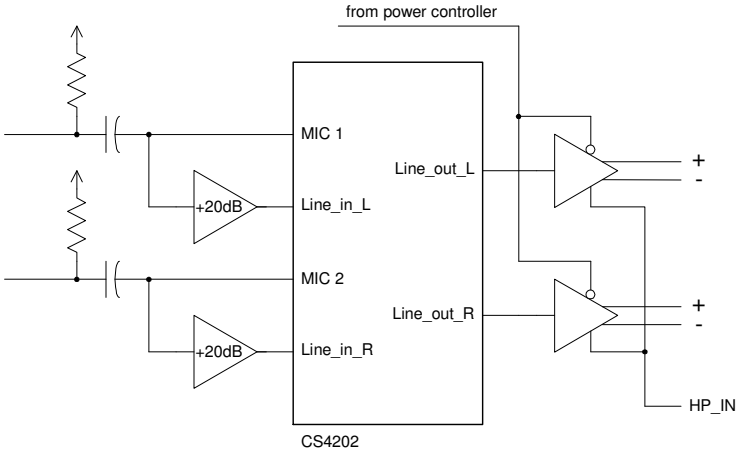
The VGX uses two SJA1000T CAN controllers with Intel 82C251 CAN transceivers for its CAN bus capabilities.

6.2.13 Audio

For its audio sub-system the VGX uses the Crystal CS4202, an AC '97 stereo codec with dual audio input and output channels. The VGX adds an output power amplifier (National LM4863LQ) and a microphone pre-amp with power for electret microphones.

The output amplifier supports differential and single-ended modes. When the HP_IN signal is greater than V(HP_IN), the amplifier is in single-ended mode; when lower, it is in differential mode.

The following diagram illustrates the relationship of the VGX signal amplifiers to the codec:



The VGX microphone circuitry can be factory configured to support "line in" inputs (1 Vrms with no electret pull-ups) and different input gain and filtering. If a special configuration needed for your project, consult ADS Sales with information about your requirements.

Absolute Maximum Ratings

Vin_mic .....5 Vdc

Symbol	Parameter	Min	Typ.	Max	Units
DVdd	codec digital supply voltage		3.3		V
Avdd	codec analog supply voltage		5.0		V
fso	sample rate, output		48		kHz
fsi	sample rate, input (note 27)	8		44.1	kHz
Audio Input					
Vin_mic	signal input voltage		100		mV_{rms}
Gain_mic	pre-amp gain		20		dB
fo_mic	pre-amp low-pass cutoff (note 28)		3.4		kHz
Rin_mic	input impedance		12.5		kΩ
Cin_mic	DC blocking capacitor		1		µF
Vmicpwr	microphone power (MIC_L/R+)		5		V
Rmicpwr	microphone power, series resistance			3.2	kΩ
Audio Output					
Rl	speaker load	4	8		Ω
Vout	Zspkr=4Ω, differential mode			3.7	V_{rms}
Vdc	DC bias, differential mode		0.5		Avdd
Pspkr	output power, ea. channel (note 29)				
	differential, THD+N 1%, Rl 4Ω		1.0	2.2	W
	differential, THD+N 10%, Rl 4Ω		1.0	2.7	W
	differential, THD+N 1%, Rl 32Ω		1.0	0.34	W
	single-ended, THD+N 0.5%, Rl 32Ω		75	85	mW
	single-ended, THD+N 1%, Rl 8Ω			340	mW
	single-ended, THD+N 10%, Rl 8Ω			440	mW

Symbol	Parameter	Min	Typ.	Max	Units
R HP_IN	pull-up to Vcc			100	kΩ
V HP_IN	threshold voltage		4		V

Notes:

27. The output sample rate is fixed, but the input sample rate can be set to 8, 11.025, 22.05 or 44.1 kHz.
28. Pre-amp anti-aliasing filter rolls off at 3dB/octave (first-order filter)
29. Typical values are guaranteed to National Semiconductor's AOQL (Average Outgoing Quality Level). Operating above typical values for a sustained period of time may result in thermal shutdown of the amplifier.

6.2.14 PXA255 Processor

The XScale PXA255 core can change system voltage Vddi (6.2.2) dynamically to achieve lower power consumption at high clock rates. It uses voltage Vddx to power its interface I/Os. The EIOn digital I/Os include series resistance and ESD protection.

Serial ports configured for 3.3 V logic operation run directly to the processor (section 4.5.1). These lines should be treated as digital I/Os and protected for over-current and over-voltage accordingly.

Absolute Maximum Ratings

Input voltage, digital I/O pins.....3.6 V

Symbol	Parameter	Min	Typ.	Max	Units
Digital Outputs					
Vol			0		V_{ddx}
Voh			1.0		V_{ddx}
Io		-2		2	mA
Digital Inputs					
Vil				0.2	V_{ddx}
Vih		0.8			V_{ddx}
NSSP Port					
	Base bit rate, internal clock		3.6864		MHz
	Divisor for Internal clock	1		4096	
	Clock rate, external source			13	MHz
Vol	[tbd]		0		V_{ddx}
Voh			1.0		V_{ddx}
Vil				0.2	V_{ddx}
Vih		0.8			V_{ddx}

6.2.15 Crystal Frequencies

Agencies certifying the VGX for compliance for radio-frequency emissions typically need to know the frequencies of onboard oscillators. The following table lists the frequencies of all crystals on the VGX.

Crystal	Device	Typ.	Units
X1	ADSmartIO microcontroller	3.6864	MHz
X2	CAN controller 2	16.000	MHz
X3	XScale RTC	32.768	kHz
X4	RTC	32.768	kHz
X5	XScale core	3.6864	MHz
X7	Codec	24.576	MHz
X8	CAN controller 1	16.000	MHz
X9	Ethernet	25.000	MHz
X10	SM501 display controller	24.000	MHz

6.2.16 PCMCIA and CompactFlash Controller

VGX PCMCIA and CompactFlash control logic is managed by a Xilinx XCR3032XL CPLD with firmware developed by ADS. The signals run through buffers before going to the PCMCIA (J10, 3.4.8) and CompactFlash (J4, 3.4.4).headers.

On the VGX, the CompactFlash (CF) port can be used as a digital expansion bus. See section 4.1.5 for details.

Absolute Maximum Ratings

Input voltage, port I/O pins.....6.5 V

Symbol	Parameter	Min	Typ.	Max	Units
V_{ddx}	PCMCIA/CF buffer power		3.3		V
$V_{ccCardA,B}$	PCMCIA and CF supply voltage (note 30)	3.3	5.0	5.0	V
I 3.3V	3.3 V socket power			2	W
I 5V	5 V socket power			2	W
Rp pcmcia	Card detect (1 & 2) and voltage sense (VS1 & 2) pull-ups (note 31)		100		kΩ
Vp pcmcia	Card detect and voltage sense pull-up voltage		3.3		V
Digital Outputs					
Vol				0.2	V
Voh		3.1			V
Digital Inputs					
Vil	Vddx=3.3 V			0.8	V
Vih	Vddx=3.3 V	2.0		5.5	V

Notes:

30. The PCMCIA port supply voltage is selected programmatically.
31. Each card inserted in a PCMCIA or CF slot can drain up to 0.4 mW when the system is in Sleep mode (4 * ($Vddx^2$/Rpcmcia)).

6.2.17 I^2C Bus Master

The I2C bus on the VGX is driven by the PXA255 and is configured as described in section 4.5.6.

Symbol	Parameter	Min	Typ.	Max	Units
	bus clock (note 32)	100		400	kHz
	buffer size			1	byte
Rbus	pull-up on SDA, SCK		1.82		kΩ
Vbus			3.3		V
Rseries	resistance to ADSmartIO bus		33		Ω

Notes:

32. The PXA255 supports "standard" and "fast" I2C speeds of 100 and 400 kHz.

7 Board Revision History

7.1 Identifying the board revision

The product revision number of the VGX is etched on the underside of the printed circuit board. That number is 170116-2000x, where "x" is the board revision.

7.2 Revision History

The following is an overview of the revisions of the VGX circuit board.

7.2.1 Revision 2

Initial release.

The design was based on the PXA255 AGX product. The following summarizes the changes from revision 2 of that product:

New Features since AGX rev 2

Factory option to populate Silicon Motion SM501 graphics controller.
Can support active displays with up to 24 bits of data per pixel (LVDS).
Adds SM501 Zoomed Video Port Signals to headers J8 and J40

Adds second CAN bus. Signals are on J15 and new header, J20.

Adds SPI port to J9.

Other Differences from AGX rev 2

Option for SM501 on VGX replaces Epson SID13806 graphics controller used on AGX.

RTC backup battery is mounted lying down for increased mechanical durability.

I^2C buses are reorganized, allowing separate operation of user and system functions. Signals on pins 12 and 14 of J8 are now used primarily for I^2C operation.

J8 signals (3.4.6) change as follows:

Pin	From	To
12	*SMTIO0*	*I2C_SCL*
14	*SMTIO1*	*I2C_SDA*
19	*SPDIF/SDOUT*	*VPDATA12*
21	*EAPD/SCLK*	*VPDATA13*
23	*GPIO1/SDOUT*	*VPDATA14*
25	*GPIO0/LRCLK*	*VPDATA15*

J9 removes the Ethernet anode signals and add the SPI bus signals. Changes are as follows:

Pin	From	To
17	*ETH_LED1A*	*n/c*
23	*ETH_LED2A*	*SPI_CLK*
27	*n/c*	*SPI_RXD*
28	*n/c*	*SPI_FRM*
30	*n/c*	*SPI_TXD*

J15 removes two of the analog ground and replaces them with the signals for CAN bus 2:

Pin	From	To
35	*Analog ground*	*CAN2HIGH*
36	*Analog ground*	*CAN2LOW*

J40 replaces USB On-The-Go signals with Zoomed Video Port signals as follows:

Pin	From	To
17	*OTG_M_VCC*	*VPDATA8*
18	*OTG_ID*	*VPDATA9*
19	*OTG-*	*VPDATA10*
20	*OTG+*	*VPDATA11*
21	*GND*	*VPDATA12*
22	*GND*	*VPDATA13*

7.2.2 VGX Revision A

New Features

Enable 3.3V regulator at power-on

Enhancements

Reduce sleep current

Changes

J16 changes from 10-pin header to 16-pin socket

7.2.3 Revision B

New Features

Allow 18-bit LVDS LCDs
Add optional power off
Enable 3.3V regulator at power-on

7.2.4 Revision C

New Features

Allow 24-bit LVDS LCDs

Enhancements

Improve USB and Ethernet performance

Changes

Change lithium battery to 12 mm coin battery
Revert to old Ethernet Driver

7.2.5 Revision D

New Features

Add FETs to support P30 flash

7.2.6 Revision E

New Features

Replace crystal with oscillator for USB bus stability

Enhancements

LVDS supports many displays and Intel P30 flash

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