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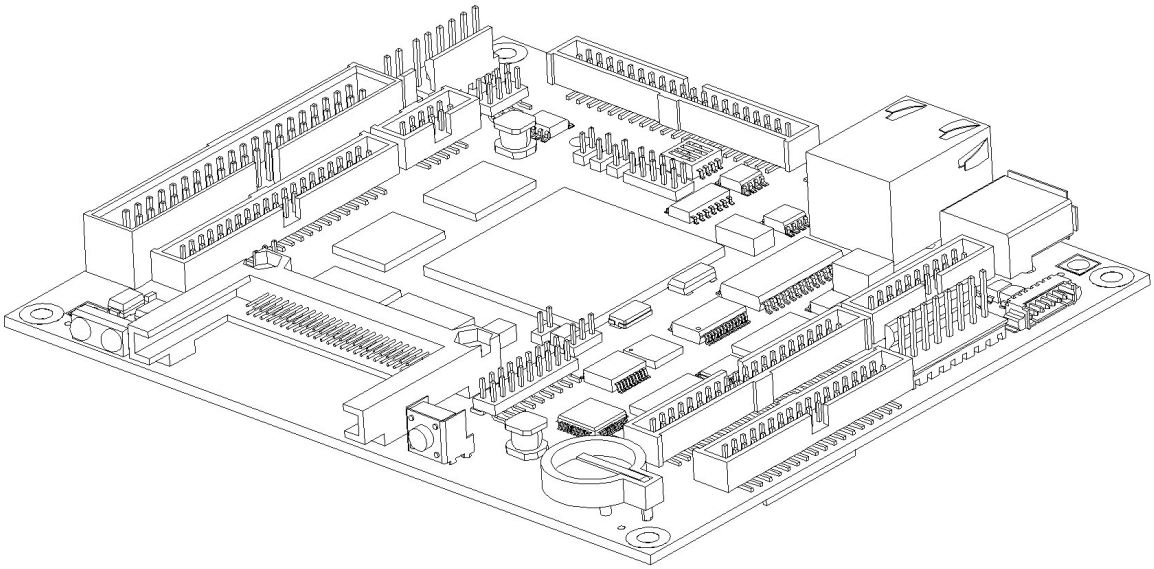
Embedded Computer Systems

Sphere II User's Manual



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About the Cover Image

The cover image shows a fully populated Revision 1 Sphere II board.

Printing this Manual

This manual has been designed for printing on both sides of an 8.5x11 inch paper, but can be printed single-sided as well. It has also been optimized for use in electronic form with active cross-reference links for quick access to information.

Revision History

The following list summarizes the changes that have been made between released revisions of the manual.

REV	DESCRIPTION	BY
	First release	1/12/07 ak

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Table of Contents

1 Introduction

1.1 Overview

The Sphere II is a full-featured single board computer driven by the highly integrated Cirrus Logic EP9315 ARM system-on-chip processor. Among other features, the EP9315 supports Ethernet, USB, EIDE, LCD displays and includes a floating point math engine optimized for digital music compression and decompression.

The Sphere II is designed to meet the needs of embedded and graphical systems developers whose applications require low power, a small form factor and an aggressive price point. It is a successor to the ADS Sphere single-board computer.

This manual applies to the most current revision of the Sphere II, as listed in the Revision History section of this manual.

1.2 Features

The following is a summary of key features of the Sphere II single-board computer.

1.2.1 Processor

- Cirrus Logic EP9315 system-on-chip processor
- 200 MHz, 32-bit ARM920T core
- 100 MHz system bus

1.2.2 Power Supply

- Requires external 5 V and 3.3 V for main power
- External inputs for real-time clock and LCD Contrast power

1.2.3 Memory and Storage

- 64 MiB synchronous DRAM [1] [2]
- 32 MiB flash RAM [3]
- CompactFlash[4] (CF), Type I and II, 3.3 V or 5 V
- IDE interface for hard drives and CD-ROM drives

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[1] The Sphere II supports 32 or 64 MiB SDRAM.

[2] MiB is the IEC abbreviation for mebibyte = 2^{20} byte = 1 048 576 byte. The kibi and mebi prefixes are based on the 1998 IEC standard for binary multiples. For further reading, see the US NIST web site, http://physics.nist.gov/cuu/Units/binary.html

[3] The Sphere II supports up to 64 MiB of onboard flash memory.

[4] CompactFlash is a trademark of the CompactFlash Association, http://www.compactflash.org/.

1.2.4 Communications [5]

- Three USB 2.0 Host ports at low (1.5 Mbps) and full (12 Mbps) speed
- One low/full speed USB 2.0 Function port
- Three Serial Ports
  - Serial 1: 7-wire EIA/TIA-232 with 3.3V logic production option
  - Serial 2: 5-wire EIA/TIA-232, 3.3V logic or IrDA
  - Serial 3: EIA/TIA-422/485 with 3-wire, 3.3V logic production option
- 10/100BT Ethernet, RJ45
- CAN 2.0b (production option)
- CompactFlash
- I^2C
- SPI/SSP

1.2.5 User Interface and Display

- Logic-level flat panel interface
- LVDS LCD interface (production option)
- Backlight brightness and on/off control signals
- Four, five, seven or eight-wire analog-resistive touch panel interface
- Option for external, software-controlled power supply for passive LCD contrast control

1.2.6 Discrete I/O

- 8x8 matrix keypad or sixteen digital I/Os
- Up to twenty additional general-purpose digital I/Os

1.2.7 Audio Interface

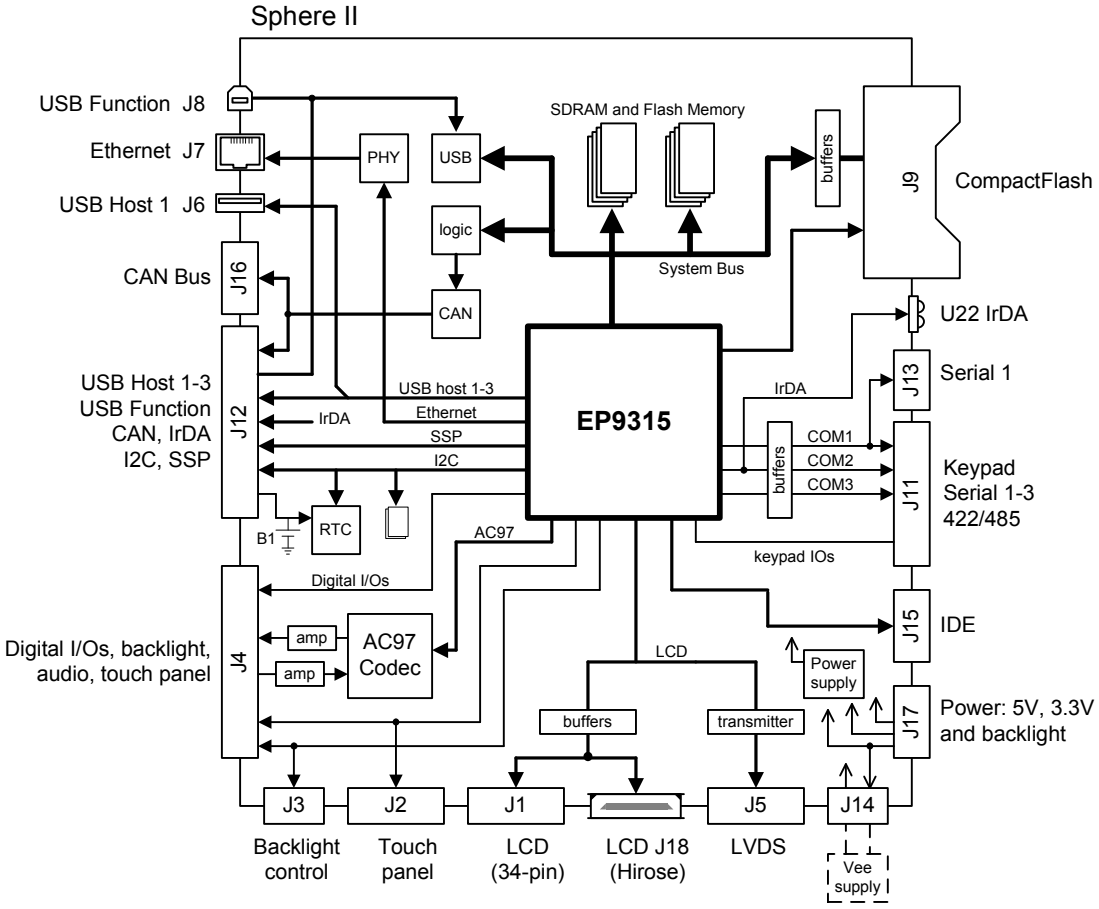
- AC'97 codec
- Stereo microphone input
- Stereo 1W speaker outputs
- Headphone output

[5] Consult factory for availability of drivers for the operating system you select.

1.3 Block Diagram

The following diagram illustrates the system organization of the Sphere II. Arrows indicate direction of control and not necessarily signal flow.

Note that this diagram is schematic and does not represent the physical layout of the Sphere II. See sections 3.1and 6.1 for layout and mechanical details.



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2 Getting Started

This chapter describes the standard Sphere II development platform, addresses frequently asked questions about the development platform, provides an overview of this manual and provides references for errata and further reading.

2.1 Development Systems

Sphere II boards are shipped as development systems designed to get the developer up and running quickly.

To use the system, simply plug power supply into the mini DIN-8 receptacle on the system.

If the screen does not display anything after five to ten seconds, check the *Frequently Asked Questions*, below. Most operating systems cold boot within twenty seconds.

2.1.1 System Components

A typical development system is shown at right (system at right illustrates a BitsyX development system). It consists of the following components:

- Sphere II single-board computer
- Flat panel display and cable
- Backlight inverter and cable
- Touch screen and cable
- 120 VAC power adapter
- Plexiglas mounting
- Developer's Cable Kit including
  - Serial port cable, 2x5 2mm to DB9 (ADS cable #610111-8000)
  - DB9F/F null modem cable
- Operating system of your choice
- User's Guide (this document and operating system guide)

Please make sure you have received ***all*** the components before you begin your development.

2.1.2 The Sphere II Connector Board

Development systems include a connector board that breaks out the signals from headers J11, J12 and J13. The board include the following features:

- Two USB host ports
- Headers for serial ports 1 and 2
- Synchronous serial port header
- Keypad header

Schematics and mechanical drawings for this board are provided on the ADS support site.

2.2 Frequently Asked Questions

The following are some of the most commonly asked questions for development systems:

Q: When I plug in power, my screen is white and nothing comes up on it.

A: Check the connector seating. The flat panel connector may have come loose in shipping. Press it firmly into the panel and reapply power to your system.

Q: Is there online support?

A: Yes. Information about the Sphere II hardware and software is available on the ADS support site at http://www.applieddata.net/support. See section 2.4 for further details.

Q: When I plug in power, the LED doesn't turn on.

A: Your system may still be booting. The LED is software controlled and is not necessarily turned on at boot.

Q: Do I have to turn off the system before I insert a CompactFlash card?

A: No. The Sphere II supports hot-swapping of CompactFlash cards. Consult the operating system documentation for details.

Q: Do I need to observe any ESD precautions when working with the system?

A: Yes. If possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the board or touching any components on the board.

Q: What do I need to start developing my application for the system?

A: You will need a flash ATA card (32 MiB or larger) and the cables supplied with your system to interface your development station to the system. For further direction, consult the ADS guide for the installed operating system.

Q: Who can I call if I need help developing my application?

A: ADS provides technical support to get your development system running. For customers who establish a business relationship with ADS, we provide support to develop applications and drivers.

Q: Can I upgrade the version of the operating system?

A: Yes. ADS provides regular operating system updates on its developers' web site. For operating systems not maintained by ADS, contact the operating system vendor.

Q: I would like to interface to a different display panel. How can I do this?

A: ADS may have already interfaced to the panel you are interested in. Consult ADS for availability.

2.3 Organization of this Manual

The manual organizes information in five key sections:

Introduction	Provides an overview of the functionality and organization of the Sphere II, as well as how to use this manual.
Hardware Reference	Describes the configuration settings and pinouts for all connectors and jumpers on the Sphere II.
Feature Reference	Gives details about the various subsystems of the Sphere II.
Power Management	Provides key information about power supply architecture, power management and tips for system integration.
Specifications	Electrical and mechanical interface specifications.

To locate the information you need, try the following:

1. Browse the *Table of Contents.* Section titles include connector designators and their function.
2. Follow cross-references between sections.
3. View and search this manual in PDF format

2.4 Errata, Addenda and Further Information

Errata and addenda to this manual are posted on the ADS support forums along with the latest release of the manual. Consult the support forums any time you need further information or feel information in this manual is in error. You may access the forums from the ADS support site,

http://www.applieddata.net/support

In addition to manuals, the support forums include downloads, troubleshooting guides, operating system updates and answers to hundreds of questions about developing applications for ADS products. You may also post questions you have about ADS products on the forums.

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3 Hardware Reference

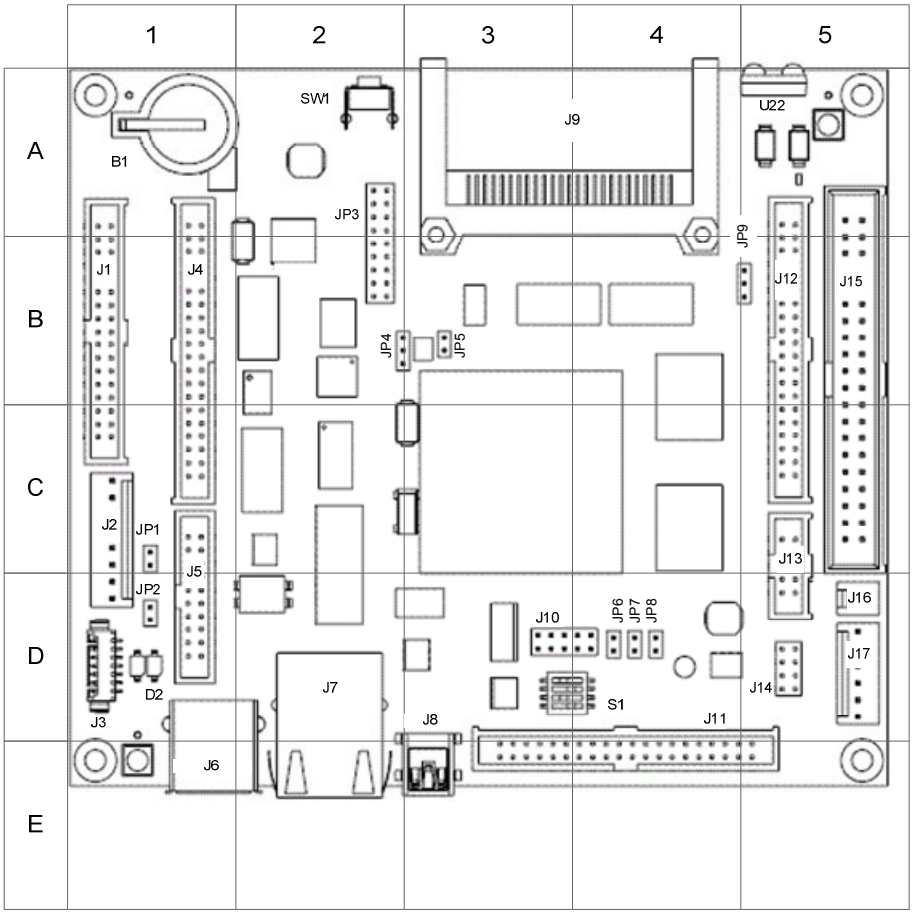
This section gives an overview of the hardware features of the Sphere II. This overview includes a description of the switches, jumper settings, connectors and connector pinouts.

3.1 Identifying Connectors

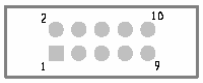
The section describes how to locate connectors on the board and how to determine how each header is numbered.

3.1.1 Locating Connectors

The following diagram illustrates the location of key components on the Sphere II. For example, the USB socket is located in square D1 and the reset button is in A2. Component listings in this chapter refer to this diagram.



3.1.2 Determining Pin Numbers



The pins of headers and connectors on ADS products are numbered sequentially. Double-row headers place even pins on one side and odd pins on the other. The diagram at right indicates how pins are numbered, as seen from the component side[6] of the board.

To locate pin 1 of a connector or jumper, try the following:

1. Look for a visible number or marking on the board that indicates connector pin numbering. A notch or dot usually indicates pin 1.

2. For through-hole connectors, look at the underside of the board. The square pad is pin 1.

3. Download the mechanical drawing of the Sphere II from the ADS Support site (section 2.4). The square or indicated pad on each connector is pin 1.

3.2 Switches, LEDs, RTC Battery and IrDA

This section describes various switches, controls and indicators on the Sphere II. The location indicated for each item refers to the grid diagram of the Sphere II in section 3.1.1.

3.2.1 S1: DIP Switch

Location on board: D3-D4

S1 is a four-position DIP switch. When in the "ON" position, switches are closed and connect to ground. Otherwise they are pulled up. The DIP switches connect to the system controller.

Most operating systems on the Sphere II reserve these switches for their use. Consult the operating system manual for details.

3.2.2 SW1: Reset Switch

Location on board: A2

SW1 is the reset button for the Sphere II. This switch issues a hardware reset to the EP9315 and system peripherals. Press this button to restart the Sphere II without cycling power. The contents of DRAM are usually lost when a hardware reset occurs.

Pressing SW1 shorts the /RESET_IN signal (J12) to ground. If your peripherals need to be reset when this button is pressed, use the RESET_OUT signal on pin 2 of J12. You can hold the Sphere II in reset by pressing and holding this button.

[6] The "component side" of the Sphere II is the one on which the CompactFlash socket is installed. As a factory option, some through-hole connectors may be installed on the "bottom side" of the Sphere II.

3.2.3 LED Indicators

The Sphere II has several onboard light-emitting diodes (LEDs) to indicate system operation. Some are software-controllable, while others indicate the status of specific functions.

Software-Controllable LED

Location on board: D1

One LED is controlled by the processor (section 4.1.6) and is used to indicate boot and operating system status. This LED can be used by applications to indicate operational status.

The LED control signal comes out to header J11. The red LED signal from the EP9315 is available on header J11 but is used for a processor workaround and is not for application use.

Signal Name	Designator	Color
GRNLED	*D2*	*Green*

Ethernet LEDs

Location on board: E2 (Ethernet socket J7)

Two LEDs integrated into Ethernet socket J7 indicate when a valid Ethernet connection has been made and when there is activity on the bus.

3.2.4 U22: IrDA Transceiver

Location on board: A5

U22 is an IrDA transceiver that converts Serial 2 electrical signals to infrared light pulses for IrDA communications. IrDA signals are also available on header J12. See section 4.4.1 for further details.

3.2.5 B1: Battery Socket for Real-Time Clock

Location on board: A1

The B1 socket holds a coin cell battery that allows the Sphere II to maintain time and date information when the rest of the system is powered off.

Battery specifications are listed in section 6.4.1.

3.3 Jumper Settings

Jumpers on the Sphere II select a variety of operational modes. All use 2mm shorting blocks (shunts) to select settings. Turn off power to the Sphere II before changing the position of a shunt.

The location indicated for each item refers to the grid diagram of the Sphere II in section 3.1.1

3.3.1 JP1: LCD RL Signal

Type: 2-post header, 2mm
Location on board: C1

This jumper determines the voltage for the PNL_RL signal on J1 and J18. On some active-matrix LCD displays, the PNL_RL signal flips the displayed image right-to-left.

Jumper setting	Connects RL to…
1-2	*GND*
n/c	*PNL_PWR*

3.3.2 JP2: LCD UD Signal

Type: 2-post header, 2mm
Location on board: D1

This jumper determines the voltage for the PNL_UD signal on J1 and J18. On some active-matrix LCD displays, the PNL_UD signal flips the displayed image bottom-to-top.

Jumper setting	Connects UD to…
1-2	*GND*
n/c	*PNL_PWR*

3.3.3 JP3: Serial 2 Mode Select

Type: 2x9 header, unshrouded, 2mm
Location on board: A2-B2

This header selects the communications mode of Serial Port 2 of the EP9315. As a production option (6.2), this header can be replaced by resistor packs that select a specific serial mode.

The operating system must configure the processor for the target serial mode. The table below lists the standard voltages to expect on the transmit line of the port when the transmitter is idle.

See section 4.4.1 for further details about Serial 2 usage on the Sphere II.

Serial 2 Mode	JP3 Shunt Settings	Tx Vidle [7]
EIA-232	*1-2, 3-4, 7-8, 9-10, 11-12, 13-14, 15-16, 17-18*	-6 V
3.3V logic	*1-3, 8-10 11-13,16-18*	3.3 V
IrDA[8]	*3-5, 6-8*	0 V

[7] Polarity and magnitude of idle voltages are listed. Actual voltages may vary.

[8] The IrDA transceiver is enabled with the IrDA_On signal from the system controller CPLD.

3.3.4 JP4: LCD Display Power

Type: 3-post header, 2mm
Location on board: B2-B3

This jumper selects the supply voltage for the LCD display. The voltage selected here is passed to the *PNL_PWR* pins on J1, J5 and J18.

Jumper setting	Voltage Selected
1-2	*Vddx (3.3 V)*
2-3	*Vcc (5.0 V)*

WARNING! Make sure you have selected the correct voltage before connecting the panel. Flat panels can be irreparably damaged by incorrect voltages.

IMPORTANT! This shunt is populated at the factory to match the voltage of the signal buffer circuits populated on the board. While the buffers may perform adequately at a different voltage than what was set at the factory, ADS cannot guarantee long-term performance.

Contact ADS Sales if your display requires a different display voltage than what is configured on standard production systems.

3.3.5 JP5: Test Shunt

Type: 2-post header, 2mm
Location on board: B3

This jumper should be left unpopulated for normal operation.

Jumper setting	Mode
1-2	*Serial boot*
n/c	*Standard boot*

3.3.6 JP6, JP7: EIA-485 Duplex

Type: 2-post headers, 2mm
Location on board: D4

These jumpers select full or half duplex for EIA-485 communications. See section 4.4.1 for further details.

Jumper setting	EIA-485 is...
1-2	*Half Duplex*
n/c	*Full Duplex*

3.3.7 JP8: EIA-485 Termination

Type: 2-post headers, 2mm
Location on board: D4

This jumper inserts a termination resistor across the lines of the EIA-485 bus. See section 6.4.4for electrical specifications.

Jumper setting	EIA-485 termination resistor
1-2	*Installed*
n/c	*Not installed*

3.3.8 JP9: EIDE Cable Select (CS/CSEL)

Type: 3-post header, 2mm
Location on board: B5

This jumper selects the voltage at pin 28 of EIDE header J15. This signal is used for drives that use a special cable to select which of two drives will be Device 0 (master). Most drives use physical shunts to select priority, and ignore this setting.

Jumper setting	J15 pin 28 is...
1-2	*pulled up to Vddx (3.3V)*
2-3	*pulled down to ground*

3.4 Signal Headers

The following tables describe the electrical signals available on the connectors of the Sphere II. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions and references to related chapters.

The location indicated for each item refers to the grid diagram of the Sphere II in section 3.1.1. For details about how to determine pin numbers of a header, see section 3.1. For precision measurements of the location of the connectors on the Sphere II, refer to section 6.1.1.

Legend:

n/c	Not connected
GND	ground plane
(3.3.1)	Reference section for signals

Signal Types

I	signal is an input to the system
O	signal is an output from the system
IO	signal may be input or output
P	power and ground
A	analog signal
OCI	open-collector/open-drain input
OC	open-collector/open-drain output

3.4.1 J1: LCD Display (34-pin)

Board Connector: 2x17 header, 2mm spacing, STMM-117-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-117-02-F-D-500)

Location on board: A1-C1

The following table describes the signals on the LCD interface connector. Signal names shown are for TFT active matrix color LCDs at 16 bpp (bit-per-pixel). For other color depths and LCD technologies, consult the table in section 4.7.2. Signals from the EP9315 are buffered and EMI filtered before reaching J1. See section 4.7 for further details about displays.

Pin	Signal Name	Color Active TFT Display at 16bpp	
		ADS Signal Name	Description
1		*PNL_VEE*	*V_{EE} (contrast); see J14*
2		*GND*	*ground*
3	*LCD_PCLK*	*PNL_PIXCLK*	*Pixel Clock*
4	*LCD_LCLK*	*PNL_HSYNC*	*Horizontal Sync.*
5	*LCD_FCLK*	*PNL_VSYNC*	*Vertical Sync.*
6		*GND*	*ground*
7	*LCD_P15*	*PNL_RED0*	*Red data*
8	*LCD_P11*	*PNL_RED1*	
9	*LCD_P12*	*PNL_RED2*	
10	*LCD_P13*	*PNL_RED3*	
11	*LCD_P14*	*PNL_RED4*	
12	*LCD_P15*	*PNL_RED5*	
13		*GND*	*ground*

14	*LCD_P5*	*PNL_GREEN0*	*Green data*
15	*LCD_P6*	*PNL_GREEN1*	
16	*LCD_P7*	*PNL_GREEN2*	
17	*LCD_P8*	*PNL_GREEN3*	
18	*LCD_P9*	*PNL_GREEN4*	
19	*LCD_P10*	*PNL_GREEN5*	
20		*GND*	*ground*
21	*LCD_P4*	*PNL_BLUE0*	*Blue data*
22	*LCD_P0*	*PNL_BLUE1*	
23	*LCD_P1*	*PNL_BLUE2*	
24	*LCD_P2*	*PNL_BLUE3*	
25	*LCD_P3*	*PNL_BLUE4*	
26	*LCD_P4*	*PNL_BLUE5*	
27		*GND*	*ground*
28	*L_BIAS*	*PNL_LBIAS*	*Data enable*
29		*PNL_PWR*	*LCD power (set by JP4)*
30			
31		*PNL_RL*	*Horizontal Mode Select (set by JP1)*
32		*PNL_UD*	*Vertical Mode Select (set by JP2)*
33	*(CPLD)*	*PNL_ENA*	*Panel enable signal*
34		*VCON*	*low-voltage adjust for contrast control of some displays (6.4.4)*

3.4.2 J2: Touch Panel

Board Connector: 1x4, 1x5 or 1x8 header, 0.100 inch spacing, Molex 22-23-2041, -2051 or -2081

Location on board: C2-D2

The EP9315 touch panel controller drives four-, five-, seven- and eight-wire analog-resistive touch panels.[9] The Sphere II brings the controller lines out to headers J2 and J4. As a production option, header J2 may be populated to suit the type of touch panel you have connected. See section 6.2 for details. Electrical specifications for the touch panel controller are listed in section 6.4.5.

The following table illustrates how to connect touch panels to Sphere II header J2. LL stands for "lower left" and UR for "upper right" and in the signal names, the letter "s" stands for "sense." The X+/- and Y+/- signals are sometimes referred to as the "excite" lines of a touch panel.

		Four and Eight-Wire			**Five- and Seven-Wire**		
Pin	**Type**	**Signal**	**4-wire**	**8-wire**	**Signal**	**5-wire**	**7-wire**
1	*AIO*	*X-*	*left*	*left*	*V-*	*LL*	*LL*
2	*AIO*	*X+*	*right*	*right*	*V+*	*UR*	*UR*
3	*AIO*	*Y+*	*top*	*top*	*Z+/-*	*UL*	*UL*
4	*AIO*	*Y-*	*bottom*	*bottom*	*Z-/+*	*LR*	*LR*
5	*AIO*	*sY+*		*top*	*Wiper*	*Wiper*	*Wiper*
6	*AIO*	*sY-*		*bottom*	*n/c*		
7	*AIO*	*sX+*		*right*	*sV+*		*sUR*
8	*AIO*	*sX-*		*left*	*sV-*		*sLL*

[9] Seven- and eight wire panels add sense lines to five- and four-wire panels to compensate for temperature and panel size.

3.4.3 J3: Backlight Inverter

Board Connector: Molex 53398-0790

Location on board: D1

This connector supplies power and control signals to a backlight inverter. These signals are also available on header J4.

See the "Brightness Control (Backlight)" paragraph in section 4.7.2 for additional details about these signals.

Pin	Name	Type	Description
1	*Vbacklight*	*PO*	*Power supply for backlight inverter*
2			
3	*GND*	*P*	*ground*
4			
5	*BacklightOn*	*OC*	*On/off control for backlight inverter*
6	*BacklightPWM*	*AO*	*Brightness control for backlight inverter*
7	*GND*	*P*	*ground*

3.4.4 J4: Audio, Digital I/Os, Touch Panel, Backlight

Board Connector: 2x20 header, 2 mm spacing, Samtec STMM-120-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-120-02-F-D-500)

Location on board: A1-C1

Pin	Name	Type	Description
1	*Vbacklight*	*PO*	*Backlight power*
2	*Vbacklight*	*PO*	
3	*VCC*	*PO*	*5 V*
4	*VCC*	*PO*	
5	*VDDX*	*PO*	*3.3 V*
6	*VDDX*	*PO*	
7	*GND*	*P*	*ground*
8	*GND*	*P*	
9	*BacklightOn*	*O*	*Backlight on/off (4.7.2)*
10	*BacklightPWM*	*AO*	*Backlight intensity control (4.7.2)*
11	*X-*	*AIO*	*Touch panel (4.6)* *(see signal descriptions on header J2)*
12	*X+*	*AIO*	
13	*Y+*	*AIO*	
14	*Y-*	*AIO*	
15	*sY+*	*AIO*	
16	*sY-*	*AIO*	
17	*sX+*	*AIO*	
18	*sX-*	*AIO*	

Pin	Name	Type	Description	
19	reserved	IO	PA1 [10]	EP9315 digital I/Os (4.5.1)
20	EGPIO_EX6	IO	PA6 [10]	
21	reserved	IO	PA7 [10]	
22	EGPIO_EX10	IO	PB2	
23	EGPIO_EX11	IO	PB3	
24	EGPIO_EX12	IO	PB4	
25	EGPIO_EX13	IO	PB5	
26	EGPIO_EX14	IO	PB6	
27	SPDIF_OUT	O	Audio codec serial interface	
28	POWERENABLE	O	Output for power supply management (5.1)	
29	HP_STATUS	0	State of headphone/speaker mode (4.3.2)	
30	HP_SW	I	Programmatic control of HP_STATUS (4.3.2)	
31	SPKL+	AO	Stereo speaker, left channel	
32	SPKL-	AO		
33	SPKR+	AO	Stereo speaker, right channel	
34	SPKR-	AO		
35	AGND	AP	Analog ground	
36		AP		
37	MIC1_IN	AI	left	Stereo microphone input
38	MIC2_IN	AI	right	
39	AGND	AP	Analog ground	
40		AP		

3.4.5 J5: LCD Signals, LVDS

Board Connector: 2x10 header, 2 mm spacing, Molex 87331-2020.

Location on board: C1-D1

This header supplies the LCD signals in LVDS format. The LCD signals on each differential pair are listed in the table below, in the order that they are clocked out.[11] Additional details about LVDS are listed in section 4.7.2.

Pin	Name	Type	Description
1	PNL_PWR	PO	Display power
2			
3	GND	P	ground
4			
5	TXOUT0-	O	LVDS Data 0 (G0, R5..R0)
6	TXOUT0+	O	
7	GND	P	ground
8	TXOUT1-	O	LVDS Data 1 (B1-B0, G5-G1)
9	TXOUT1+	O	
10	GND	P	ground

[10] See the discrete IO reference tables in sections 4.1.6 and 4.5.1 for alternate functions of these signals. PA1 and PA7 are reserved for USB use on the Sphere II.

[11] Signals shown are with the EP9315 LCD raster controller in 18 bpp mode.

Pin	Name	Type	Description
11	*TXOUT2-*	*O*	*LVDS Data 2*
12	*TXOUT2+*	*O*	*LBIAS/DE, VSYNC, HSYNC, B5-B2)*
13	*GND*	*P*	*ground*
14	*CKOUT-*	*O*	*LVDS Clock (PCLK)*
15	*CKOUT+*	*O*	
16	*GND*	*P*	*ground*
17	*n/c*		*reserved*
18	*n/c*		
19	*GND*	*P*	*ground*
20			

3.4.6 J6: USB Host Port 1

Board connector: USB Type A, Amp 787616-1

Location on board: E1

This connector provides the signals for USB host connectivity. USB mice, keyboards and other USB function devices may be plugged in. Further details about USB are provided in section 4.4.3.

These signals for host port 1, as well as host ports 2 and 3 are available on header J12.

Pin	Name	Type	Description
1	*USB_M_VCC*	*PO*	*DC power output*
2	*USB_M_UDC-*	*IO*	*USB host +*
3	*USB_M_UDC+*	*IO*	*USB host -*
4	*GND*	*P*	*ground*

3.4.7 J7: Ethernet

Board Connector: RJ-45 with integrated magnetics and LEDs

Location on board: D2-E2

This header is a standard RJ-45 Ethernet socket. See section 4.4.4 for further details about the Ethernet interface.

3.4.8 J8: USB Function Port

Board connector: USB Mini Type B, FCI 55671-1505T

Location on board: E3

This connector provides the signals for USB function connectivity, and is typically used to connect "upstream" to a PC. These signals are also available on header J12. Further details about USB are provided in section 4.4.3.

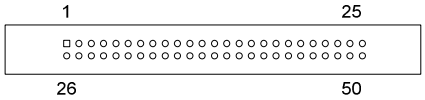
Pin	Name	Type	Description
1	*USB_F_VCC*	*PI*	*DC power in*
2	*USB_F_UDC-*	*IO*	*USB function +*
3	*USB_F_UDC+*	*IO*	*USB function -*
4	*USB_F_ID*	*IO*	*USB ID* [12]
5	*GND*	*P*	*ground*

[12] The USB_F_ID signal is not used by the Sphere II USB controller.

3.4.9 J9: CompactFlash

Board Connector: FCI 62453-022

Location on board: A3-A4



Header J9 is a CompactFlash socket suitable for use with an array of third-party memory and I/O cards to expand the Sphere II's capabilities. See section 4.1.5 for additional details. Electrical specifications are listed in section 6.4.14.

As shown in the diagram above; the pins on CompactFlash sockets are numbered down the length of the row (this pin numbering is different from that of other sockets on the Sphere II). The signal names listed below are for the CF bus in I/O mode.[13]

Pin	Name	Type	Description
1	*GND*	*P*	*ground*
2	*D3*	*IO*	*Data 3-7*
3	*D4*	*IO*	
4	*D5*	*IO*	
5	*D6*	*IO*	
6	*D7*	*IO*	
7	*/CE1*	*O*	*High Byte Chip Select*
8	*A10*	*O*	*Address 10*
9	*/OE*	*O*	*Memory Read*
10	*A9*	*O*	*Address 7-9*
11	*A8*	*O*	
12	*A7*	*O*	
13	*CARDVCC*	*PI*	*Power Output to Card*
14	*A6*	*O*	*Address 0-6*
15	*A5*	*O*	
16	*A4*	*O*	
17	*A3*	*O*	
18	*A2*	*O*	
19	*A1*	*O*	
20	*A0*	*O*	
21	*D0*	*IO*	*Data 0-2*
22	*D1*	*IO*	
23	*D2*	*IO*	
24	*/IOIS16*	*I*	*16 Bit Access*
25	*/CD2*	*I*	*Card Detect 2*
26	*/CD1*	*I*	*Card Detect 1*
27	*D11*	*IO*	*Data 11-15*
28	*D12*	*IO*	
29	*D13*	*IO*	
30	*D14*	*IO*	
31	*D15*	*IO*	
32	*/CE2*	*O*	*Low Byte Chip Select*
33	*/VS1*	*I*	*Voltage Sense 1 Input*
34	*/IORD*	*O*	*IO Read*
35	*/IOWR*	*O*	*IO Write*
36	*/WE (/MWR)*	*O*	*Memory Write*
37	*IRQ*	*I*	*Interrupt Signal*
38	*VCC*	*P*	*Card Power*

[13] CompactFlash Association. "CF+ and CompactFlash Specification Revision 1.4," July 1999.

Pin	Name	Type	Description
39	*/CARDSEL*	*O*	*Card Select*
40	*/VS2*	*I*	*Voltage Sense 2 Input*
41	*RESET*	*O*	*Reset*
42	*/WAIT*	*I*	*Wait*
43	*/INPACK*	*I*	*Interrupt Acknowledge*
44	*/REG*	*O*	*Register Access*
45	*SPKR*	*I/O*	*Speaker Input*
46	*/STSCHG*	*I/O*	*Status Change*
47	*D8*	*IO*	*Data 8-10*
48	*D9*	*IO*	
49	*D10*	*IO*	
50	*GND*	*P*	*ground*

3.4.10 J10: Manufacturing Test

Board Connector: 2x5 receptacle, 2mm spacing, Samtec SQT-105-01-L-D

Location on board: D3-D4

This header is used for manufacturing test and to program the boot flash and onboard logic. These signals are intended only for factory use.

Pin	Name	Type	Description
1	*/TRST*	*I*	*JTAG signals*
2	*TMS*	*I*	
3	*GND*	*P*	
4	*TDI*	*I*	
5	*TCLK*	*I*	
6	*VDDX*	*PO*	
7	*GND*	*P*	
8	*TDO*	*O*	
9	*/FEW*	*I*	
10	*FRDY*	*O*	

3.4.11 J11: Keypad, Serial 1, 2 and 3, EIA-422/485, LEDs

Board Connector: 2x20 header, 2 mm spacing, Samtec STMM-120-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-120-02-F-D-500)

Location on board: E3-E5

Pin	Name	Type	Description	
1	*ROW0*	*IO*	*C0*	*Keypad rows (4.1.7) or GPIOs (4.5.1)*
2	*ROW1*	*IO*	*C1*	
3	*ROW2*	*IO*	*C2*	
4	*ROW3*	*IO*	*C3*	
5	*ROW4*	*IO*	*C4*	
6	*ROW5*	*IO*	*C5*	
7	*ROW6*	*IO*	*C6*	
8	*ROW7*	*IO*	*C7*	

Pin	Name	Type	Description		
9	COL0	IO	D0	Keypad columns (4.1.7) or GPIOs (4.5.1)	
10	COL1	IO	D1		
11	COL2	IO	D2		
12	COL3	IO	D3		
13	COL4	IO	D4		
14	COL5	IO	D5		
15	COL6	IO	D6		
16	COL7	IO	D7		
17	RXD1	I	Serial 1, EIA-232 (4.4.1)		
18	TXD1	O			
19	DTR1	O			
20	GND	P	ground		
21	DSR1	I	Serial 1, EIA-232 (4.4.1)		
22	RTS1	O			
23	CTS1	I			
24	RXD2	I	Serial 2, EIA-232 (4.4.1)		
25	TXD2	O			
26	CTS2	I			
27	RTS2	O			
28	GND	P	ground		
29	(RXD3)	I	Volume production option: Logic-level Serial 3 (4.4.1, 6.2)		
30	(TXD3)	O			
31	RX422+	I	EIA485+	I/O	Serial 3, EIA-422/485 (4.4.1)
32	RX422-	I	EIA485-	I/O	
33	TX422+	O	(RTS3)	O	
34	TX422-	O	(CTS3)	I	
35	VCC	PO	5 V		
36	reserved	O	Red LED. Not for application use. Leave unconnected.		
37	VDDX	PO	3.3 V		
38	GRNLED	O	Digital IO connected to transistor that drives Green LED		
39	GND	P	ground		
40		P			

3.4.12 J12: USB, I^{2}C, SSP, CAN, IrDA

Board Connector: 2x20 header, 2 mm spacing, Samtec STMM-120-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-120-02-F-D-500)

Location on board: A5-C5

Pin	Name	Type	Description
1	/RESET_OUT	O	Reset output
2	/RESET_IN	I	Reset input
3	/RqOnOff	I	Reserved for future use
4	VEEPWM	O	Contrast control PWM
5	CANHIGH	IO	CAN bus (4.4.5)
6	CANLOW	IO	
7	n/c	-	
8	n/c	-	

Pin	Name	Type	Description
9	IRDA_VccRx	PO	Production option for external IrDA transceiver (4.4.1, 6.2)
10	IRDA_RX	I	
11	IRDA_VccTx	PO	
12	IRDA_TX	O	
13	/IRDA_On	O	
14	GND	P	ground
15	USB_VCC	PO	USB Host power
16	USB1_H-	IO	USB Host Port 1 (4.4.3)
17	USB1_H+	IO	
18	USB2_H-	IO	USB Host Port 2 (4.4.3)
19	USB2_H+	IO	
20	GND	P	ground
21	USB3_H-	IO	USB Host Port 3 (4.4.3)
22	USB3_H+	IO	
23	USB_F_VCC	PI	USB Function port (4.4.3)
24	USB_F-	IO	
25	USB_F+	IO	
26	GND	P	ground
27	I2C_SDA	IO	I^2C (4.4.6)
28	I2C_SCL	O	
29	SSP_SCLK	(I)O	SSP (4.4.2)
30	SSP_SFRM	(I)O	
31	SSP_TX	O	MOSI
32	SSP_RX	I	MISO
33	GPIO_G2	IO	G2 GPIOs (4.5.1) [14]
34	GPIO_G3	IO	G3
35	VCC	PO	5 V
36	RTC_BATT	PI	RTC backup power (4.2)
37	VDDX	PO	3.3 V
38	GND	P	ground
39	GND	P	
40	GND	P	

[14] The EP9315 User Manual lists G2 and G3 as SLA[1..0], "PCMCIA voltage control pins". The Sphere II uses these pins as GPIOs.

3.4.13 J13: Serial 1

Board Connector: 2x5 header, 2mm spacing, Samtec STMM-105-01-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-105-02-F-D-500)

Location on board: C5-D5

These signals are also available on header J11, with the exception of RI1. See section 4.4.1 for further details about Serial 1.

Pin	Name	Type	Description
1	*n/c*	-	
2	*DSR1*	*I*	*Data Set Ready*
3	*RXD1*	*I*	*Receive data*
4	*RTS1*	*O*	*Ready To Send (or RTR Ready to Receive)*
5	*TXD1*	*O*	*Transmit data*
6	*CTS1*	*I*	*Clear To Send*
7	*DTR1*	*O*	*Data Terminal Ready*
8	*(RI1)*	*I*	*(Ring Indicator)*[15]
9	*GND_COM1*	*P*	*Serial 1 ground*
10	*n/c*	-	

3.4.14 J14: LCD Contrast Control Power Supply

Board Connector: 2x4header, 2mm spacing, Samtec TMM-104-01-G-SM

Location on board: D5

This header connects to an external power supply adapter that can be used to control contrast on passive LCD displays.

Header J14 supplies power (VCC or VDDX) and control (V_CON) to the adapter and receives the contrast control voltage (VEE) from the adapter.

Pin	Name	Type	Description
1	*VCC*	*PO*	*5V*
2	*VDDX*	*PO*	*3.3V*
3	*VEE_EN*	*O*	*Vee enable signal (GPIO_EX6)*
4	*VEE*	*PI*	*Vee contrast control voltage*
5	*V_CON*	*O*	*low-voltage contrast control voltage*
6	*n/c*		
7	*GND*	*P*	*Ground*
8	*GND*	*P*	

[15] The RI (ring) signal is normally not connected. However, it can be connected to EPGIO0 in factory-custom configurations of the Sphere II. See section 6.2 for further details.

3.4.15 J15: EIDE Connector

Board Connector: 2x20 header, 0.1 mm spacing, Samtec TST-120-01-G-D

Location on board: A5-C5

This header is suitable for cabling to an Extended IDE (EIDE) mass storage device. It is the same connector as found on standard PCs.

If the header is not used for IDE, some of the signals may be remapped as general-purpose input/output pins (GPIOs). EP9315 port names are listed in the table below (e.g. PA5, PG7).

Pin	Name	Pin	Type	Description	
1	*/RESET_OUT*		*O*	*System reset*	
	GND	*2*	*P*	*ground*	
3	*UBDD7*		*IO*	*PH7*	*IDE Data and Address or GPIOs (4.5.1)*
5	*UBDD6*		*IO*	*PH6*	
7	*UBDD5*		*IO*	*PH5*	
9	*UBDD4*		*IO*	*PH4*	
11	*UBDD3*		*IO*	*PH3*	
13	*UBDD2*		*IO*	*PH2*	
15	*UBDD1*		*IO*	*PH1*	
17	*UBDD0*		*IO*	*PH0*	
	UBDD8	*4*	*IO*		
	UBDD9	*6*	*IO*		
	UBDD10	*8*	*IO*		
	UBDD11	*10*	*IO*		
	UBDD12	*12*	*IO*	*PG4*	
	UBDD13	*14*	*IO*	*PG5*	
	UBDD14	*16*	*IO*	*PG6*	
	UBDD15	*18*	*IO*	*PG7*	
19	*GND*		*P*	*ground*	
	n/c	*20*	*-*		
	GND	*22*	*P*	*ground*	
	GND	*24*	*P*		
	GND	*26*	*P*		
	CSEL	*28*	*O*	*Cable Select* *Pulled up or down based on JP9*	
	GND	*30*	*P*	*ground*	
	n/c	*32*	*-*		
	n/c	*34*	*-*		
21	*/UBDMARQ*				
23	*/UBDIOW*				
25	*/UBDIOR*			*PE2*	
27	*UBIORDY*				*IDE Control Signals or GPIOs (4.5.1)*
29	*/UBDMACK*				
31	*UBINTRQ*				
33	*UBIDEDA1*			*PE6*	
35	*UBIDEDA0*			*PE5*	
	UBIDEA2	*36*		*PE7*	
37	*/UBIDECS0*			*PE3*	
	/UBIDECS1	*38*		*PE4*	
39	*/UBDSAP*				
	GND	*40*	*P*	*ground*	

3.4.16 J16: CAN Bus

Board Connector: 1x2 header, 0.1 inch spacing, Molex 22-23-2021

Location on board: D5

The signals for the CAN bus are also available on header J12.

Pin	Name	Type	Description
1	*CANHIGH*	*IO*	*CAN bus(4.4.5)*
2	*CANLOW*	*IO*	

3.4.17 J17: Power Supply

Board Connector: 1x6 Molex #22-23-2061, 0.1 inch spacing

Location on board: D5

This header supplies power to the Sphere II. +5V_IN and +3.3V_IN are the main power supply. See section 5.1 for an overview of how the Sphere II power supply is structured and specification sections 6.4.1 and 6.4.2 for power requirements.

Pin	Name	Type	Description
1	*+5V_IN*	*PI*	*5V input power*
2	*GND_IN*	*PI*	*Ground*
3	*+3.3V_IN*	*PI*	*3.3V input power*
4	*Vbacklight*	*PI*	*Backlight power, usu. 12V (5.1)*
5	*POWERENABLE*	*O*	*Output for power supply management (5.1)*
6	*n/c*	*-*	

3.4.18 J18: LCD Display (Hirose)

Board Connector: Hirose DF9B-31P-1V

Location on board: B1, underside of board

This header can be used to directly connect to some 16 bpp active Sharp TFT displays and products that are compatible with them. The signals on this connector are a subset of the signals on J1. See section 3.4.1 for more detailed descriptions of the signals.

Pin	Name	Pin	Type	Description
1	*GND*		*O*	*ground*
	PNL_PIXCLK	*2*	*O*	*Pixel clock*
3	*PNL_HSYNC*		*O*	*Horizontal sync*
	PNL_VSYNC	*4*	*O*	*Vertical sync*
5	*GND*		*O*	*ground*
	PNL_RED0	*6*	*O*	*Red data*
7	*PNL_RED1*		*O*	
	PNL_RED2	*8*	*O*	
9	*PNL_RED3*		*O*	
	PNL_RED4	*10*	*O*	
11	*PNL_RED5*		*O*	
	GND	*12*	*O*	*ground*

Pin	Name	Pin	Type	Description
13	*PNL_GREEN0*		*O*	*Green data*
	PNL_GREEN1	*14*	*O*	
15	*PNL_GREEN2*		*O*	
	PNL_GREEN3	*16*	*O*	
17	*PNL_GREEN4*		*O*	
	PNL_GREEN5	*18*	*O*	
19	*GND*		*O*	*ground*
	PNL_BLUE0	*20*	*O*	*Blue data*
21	*PNL_BLUE1*		*O*	
	PNL_BLUE2	*22*	*O*	
23	*PNL_BLUE3*		*O*	
	PNL_BLUE4	*24*	*O*	
25	*PNL_BLUE5*		*O*	
	GND	*26*	*O*	*ground*
27	*PNL_LBIAS*		*O*	*Data enable*
	PNL_PWR	*28*	*O*	*Panel power*
29	*PNL_PWR*		*O*	
	PNL_RL	*30*	*O*	*Right/left flip*
31	*PNL_UD*		*O*	*Up/down flip*

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4 Feature Reference

This chapter provides details about the architecture and many features of the Sphere II, and how they can fit together to create a system that meets your application needs.

4.1 System Architecture

This section describes memory and core features of the Sphere II, including boot code, memory, interrupts and EP9315 GPIOs.

4.1.1 Boot Code

The Sphere II uses the first block of onboard flash to store the boot code. At the factory, boot code is loaded using Serial Port 1. Most ADS Sphere II boot loaders are field-upgradeable using a flash card on the CompactFlash port.

4.1.2 Synchronous DRAM

One bank of synchronous DRAM (SDRAM) can be populated on the Sphere II. The data bus width is 32 bit.

The memory clock speed is one half the CPU core clock speed. Typical memory bus operation is at 100 MHz.

4.1.3 Non-Volatile Memory

There are several ways to store data on the Sphere II that will persist through a power failure. Some devices can only be accessed through operating system drivers, and not all are available for application data storage.

Flash Memory

Flash memory is the primary site for non-volatile data storage. The Sphere II includes a bank of flash memory for non-volatile data storage. The board supports several sizes of installed flash. The data bus width is 32 bit.

ADS systems store the operating system, applications and system configuration settings in the onboard flash. Most operating systems configure a portion of the flash as a flash disk, which acts like a hard disk drive.

CompactFlash Cards

CompactFlash (CF) cards provide removable storage in a wide variety of capacities. These cards can be cost-effective means to expand system storage capacity for applications that provide access to the CF slot.

Ethernet MAC EEPROM

The Sphere II uses an 8k-byte serial EEPROM to store the Ethernet MAC address. The remaining memory may be available for other purposes. Built-in drivers may not be available to access this feature, but the EEPROM can be accessed using the I^2C driver (section 4.4.6). Contact ADS Sales if your application requires this feature.

RTC NVRAM

The DS1307 real-time clock chip includes 56 bytes of non-volatile RAM. The RAM is maintained as long as main or backup power is provided to the chip. Built-in drivers may not be available to access this feature, but the RAM can be accessed using the I^2C driver (section 4.4.6). Contact ADS Sales if your application requires this feature.

4.1.4 Interrupts

The Sphere II supports external interrupts through EP9315 GPIO Ports A, B and F ("enhanced" GPIO ports) as summarized in the following table.

Interrupt Signal	EP9315 Port	Header
EGPIO_EX7, 6, 1, 0	*PA[7..6, 1..0]*	*J4*
EGPIO_EX14-10	*PB[7..2]*	*J4*
CF control signals	*PF[7..0]*	*J9*

4.1.5 CompactFlash

The Sphere II includes CompactFlash socket J9 to expand the capabilities of the Sphere II. Common uses are for mass storage and wireless communications. The CompactFlash port is also typically for loading operating system files into onboard flash. Electrical specifications are listed in section 6.4.14.

4.1.6 EP9315 GPIO Cross-Reference

The EP9315 organizes its general-purpose I/O lines into eight, eight-pin ports lettered A through H. The following table describes how the Sphere II utilizes each of those GPIO lines. Elsewhere in this manual, ports are referred to by their letter and port number (e.g. PA6, PG2).

The information in this table is offered for reference purposes only, as most ADS operating system releases make this information transparent to developers.

Port		Type	Function (connector pin, section)
A	*0*	*I*	*/RqOnOff (reserved for future use)* *Production option: Ring signal RI1(J13.8;6.2)*
	1	*IO*	*EGPIO_EX1 (J4)* *Production options: (1) EIA-485 Rx enable or (2) USB host power sense*
	2		*IDE UBDMARQ (J15.21)*
	3	*O*	*EIA-485 TX enable*
	4	*O*	*RTS2 (J11)*
	5	*I*	*CTS2 (J11)*
	6	*IO*	*VEE_EN (J14.3); EGPIO_EX6 (J4.20)*
	7	*I*	*USB function port DMA request (J4.21)*
B	*0*	*O*	*IDE /DMACK (J15.29)*
	1	*O*	*IDE SENSE, USB function /EOT*
	2	*IO*	*EGPIO_EX10 (J4)*
	3	*IO*	*EGPIO_EX11 (J4)*
	4	*IO*	*EGPIO_EX12 (J4)*
	5	*IO*	*EGPIO_EX13 (J4)*
	6	*IO*	*EGPIO_EX14 (J4)*
	7		*IDE UBDASP (J15.39)*

Port		Type	Function (connector pin, section)
C	0	IO	Keypad Row Scan (J11 and 4.1.7) or GPIOs (4.5.1)
	1	IO	
	2	IO	
	3	IO	
	4	IO	
	5	IO	
	6	IO	
	7	IO	
D	0	IO	Keypad Column Scan (J11, 4.1.7) or GPIOs (4.5.1)
	1	IO	
	2	IO	
	3	IO	
	4	IO	
	5	IO	
	6	IO	
	7	IO	
E	0	O	Green LED (D2)
	1	O	Red LED (D1). Reserved for internal use.
	2		IDE Control Signals (J15)
	3		
	4		
	5		
	6		
	7		
F	0		CompactFlash Control Signals (J9)
	1		
	2		
	3		
	4		
	5		
	6		
	7		
G	0	IO	EECLK (I^2C clock)
	1	IO	EEDAT (I^2C data)
	2	IO	GPIO_G2 (J12)
	3	IO	GPIO_G3 (J12)
	4	IO	IDE DD[15:12] or GPIOs (4.5.1)
	5	IO	
	6	IO	
	7	IO	
H	0	IO	IDE DD[7:0] or GPIOs (4.5.1)
	1	IO	
	2	IO	
	3	IO	
	4	IO	
	5	IO	
	6	IO	
	7	IO	

4.1.7 Keypad Scan

The Sphere II can scan a matrix keypad up to eight by eight keys in size. Matrix keypads are simpler and cost less than active keyboards and can be easily customized for your application. You can create a keypad matrix from a collection of normally-open switches or purchase a pre-assembled keypad "off the shelf."

Features and Theory of Operation

When configured to scan a keypad, the EP9315 configures the ROWn and COLn lines as inputs. It then drives one ROW line at a time to "0" and reads the value of the COL inputs, each of which includes a passive pull-up. COL inputs that read as "0" indicate a depressed key.

The following are added details about the EP9315 keypad scanner

- The scanner reads the pressed keys several times to debounce the key press
- Rows are scanned from ROW7 to ROW0 (higher-row keys have precedence)
- Scanner generates interrupt when key is released or pressed keys change

The EP9315 includes several features that enhance keypad operation:

- Detects two keys pressed at one time
- Apparent key detection for three or more pressed keys
- Interrupts CPU only on validated key presses
- Option for three-key watchdog reset (COL2, 4 and 7 on ROW0)

Row and column lines can be used as GPIOs if keypad scan functionality is disabled. See section 4.5.1 for details.

4.2 Real-Time Clock (RTC)

The Sphere II uses a real-time clock chip to maintain the system date and time when the board is not powered.

The operating system typically reads the RTC on boot, and sets the RTC when the system time or date is changed. The system communicates with the RTC on the I^2C bus (section 4.4.6).

Backup RTC power is typically supplied by a small coin cell in battery holder B1. Backup power can also be supplied via pin 36 of J12. See section 6.4.1 for electrical specifications.

4.3 Audio

The Sphere II includes an AC97 codec for stereo audio input and output. Electrical specifications for the audio system are listed in section 6.4.11.

4.3.1 Microphone Pre-amps

The Sphere II supports the connection of a stereo electret microphone to the MIC_R and MIC_L inputs on J4. The audio signals run through pre-amplifiers that low-pass filter and boost the signal before being passed on to the audio codec.

When connecting external electret microphones to the Sphere II, use the MIC_GND analog ground plane (AGND on J4) for improved signal-to-noise ratio. The Sphere II includes pull-ups to power electret microphones.

4.3.2 Audio Outputs: Speakers and Headphones

The Sphere II audio amplifier supports both differential and single-ended output devices. Differential (or "bridge") drive delivers greater output power and is suitable for speakers, which can be wired independently from each other. Single-ended mode is used for devices like headphones, which have a common ground between output channels.

The HP_IN input (J4.29) determines the output mode of the amplifier: When HP_IN is high, the audio output drive is single-ended; when HP_IN is low, the output drive is differential. An on-board pull-up normally keeps HP_IN high.

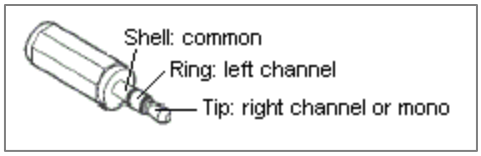
The HP_SW output from the system controller CPLD is connected to HP_IN. It can programmatically drive the HP_IN input, if needed.

Connecting Speakers

When using the Sphere II to drive speakers, short the HP_IN signal to ground. This places the output amplifier in differential mode. Connect speakers to the SPKR_L and SPKR_R outputs on J4.

Connecting Headphones

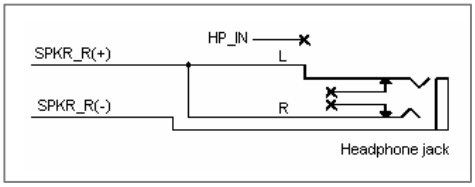
Standard headphones use a plug wired as shown at right. Three rings on the plug provide right and left channels and a common return. Mono headphones do not include the center ring.



The mating headphone jacks include spring contacts to make an electrical connection with the headphone and to mechanically hold the plug in place. Some jacks include a mechanical switch suitable for use with the HP_IN signal that is activated when a plug is inserted into the jack.

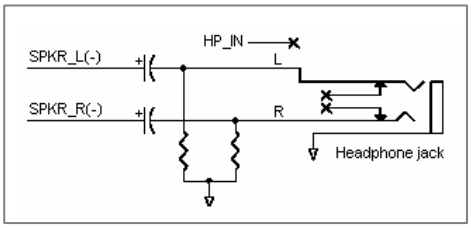
Mono Headphones

You can connect mono headphones directly to the Sphere II as shown at right. Keep in mind that the resulting impedance of the parallel-connected headphone speakers is half that of a single headphone speaker. See the audio driver specifications in section 6.4.11 for details about the minimum impedance an audio output channel can drive.



Stereo Headphones

When wiring for stereo headphones, wire blocking capacitors in series with the Sphere II SPKR- signals as shown at right. These capacitors block the DC component of the audio signal and complete the conversion from differential to single-ended output drive. Leave the HP_IN signal pulled high to enable headphone output.

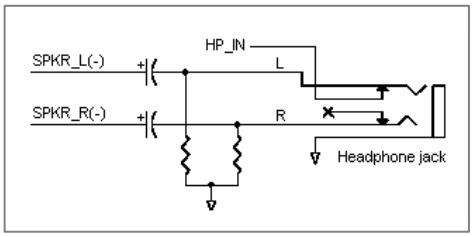


Select blocking capacitor size based on the lowest frequency your application will need to play out. Larger capacitors give improved bass response (lower frequency cutoff), but are physically larger and cost more. The corner frequency for the low-pass filter created by the capacitor and the headphone speaker is calculated as $fo=1/(2\pi R_L C)$. A 330 uF capacitor into a 32 ohm headphone speaker will give a low cutoff frequency of 15 Hz. Use electrolytic capacitors rated for at least 6.3 V.

The pull-down resistors shown in the diagram drain any charge that builds up on the headphone outputs when headphones are not connected. Use 1 kΩ resistors.

Using Stereo Headphones and Speakers in the Same System

Some applications use both headphones and speakers. You can wire the headphone jack to automatically switch the amplifier to single-ended mode when a headphone plug is inserted in the jack. This will disable the drive to any speakers that are wired into the system.



Most headphone jacks include mechanical switches that indicate when a headphone plug has been inserted. The diagram at right shows a circuit that pulls down the HP_IN signal when a headphone plug is removed.

For this circuit to work reliably in differential mode, the HP_IN signal must remain below V_{HP_IN} through the largest output voltage swings of SPKR_L. Use of 1 kΩ resistors meets this requirement.

4.4 Data Communications

The Sphere II has several built-in channels for communication with peripheral and peer devices. These include EIA/TIA-232, -422 and -485; logic-level serial; IrDA; USB host and client USB ports; Ethernet; CAN bus and I^2C.

4.4.1 Serial Ports (Asynchronous)

The EP9315 processor includes three standard serial UARTs (Universal Asynchronous Receiver/Transmitter), which on the Sphere II are mapped as Serial 1, 2 and 3.

The serial ports can be configured as follows. Production options are discussed further in section 6.2.

Port	# wires[16]	Headers	Standard	Production options
1	7	J11, J13	EIA/TIA-232	3.3 V logic
2	5	J11	EIA/TIA-232, IrDA, 3.3 V logic	
3	2-4	J11	EIA/TIA-422/485	3.3 V logic

EIA-232

EIA-232, known in the past as RS-232, is the most common serial standard. Data is transmitted with bipolar signals that are usually around six volts in magnitude, but can range from 3 to 25 volts. EIA-232 is commonly used in embedded systems for communication with PCs and peripherals.

[16] In this manual, the number listed is the total number of wires needed in a typical cable. EIA-232 and 3.3 V logic require a ground in addition to the data signals, while EIA-422/485 do not.

EIA-422/485

EIA-422 and -485 use differential signaling for greater signal integrity. EIA-485 adds multi-drop functionality and is commonly found in industrial and trucking applications. A single transceiver supports both protocols. Set the operating mode with shunts JP6 and JP7 (3.3.6).

The standard Sphere II configuration drives the transceiver's transmit-enable line with EP9315 GPIO3 and leaves the receiver permanently enabled. As a production option (6.2), the receive-enable line can be driven by GPIO3 or independently by GPIO1.

Infrared Operation

The EP9315 implements the physical layer of IrDA[17] standard version 1.1. The Sphere II supports SIR (Slow Infrared: 2.4 kbps to 115.2 kbps), MIR (Medium Infrared: 576 kbps to 1.152 Mbps) and FIR (Fast Infrared: 4 Mbps).

Software drivers for the Sphere II enable the IrDA transmitter with the IrDA_On signal, which is driven by the system controller. Electrical specifications are listed in section 6.4.7.

If your application requires external mounting of the IrDA transceiver, you may use the signals on header J12. ADS must remove the Sphere II's IrDA transceiver to prevent contention between parts. See section 6.2 for further details.

Logic-Level Operation

Ports configured for 3.3 V logic operation connect directly to the EP9315 and perform electrically as GPIOs. These IO lines are not protected, and may need ESD or over-current protection in some designs. See section 6.4.7 for serial port electrical specifications.

Serial 2 Handshaking

The RTS2 and CTS2 serial handshaking signals are EP9315 GPIO lines A4 and A5, and are not part of the EP9315's standard UART implementation. They are software-controlled in EIA/TIA-232 and 3.3 V logic modes.

4.4.2 SSP/SPI Port

The EP9315 controller drives SSP signals available for user applications. The signals are located on header J12. See section 6.4.12 for electrical specifications.

4.4.3 USB

The Sphere II includes signals for USB 2.0 Host and Function ports. USB Host (downstream) signals are on socket J6 and header J12; USB Function signals (upstream) are on socket J8 and header J12.

USB Host Port

The Sphere II USB Host ports allow you to connect up to three USB 2.0 devices to the Sphere II. USB mouse and keyboard are the most common client devices, but you can connect any USB function device that has USB drivers installed on the Sphere II.

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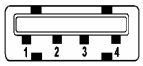
[17] In this manual, IrDA, the Infrared Data Association's standard, is used generically to refer to infrared optical communication. The standard itself includes additional protocols that must be implemented in software and are outside the scope of this manual.

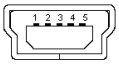


The Sphere II includes Type A USB connector J6 for Host Port 1 (mating face of socket is shown at left). You can also directly wire three USB devices to the signals on J12 or connect them via Type A sockets. Note that only one set of the USB Host Port 1 signals at J6 or J12 should be used at a time. To connect more than three USB client devices to the Sphere II, use a USB hub.

The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The Sphere II supplies 5 V power through the USB_VCC pins. Make sure to account for power used through USB in your Sphere II power budget (section 5.2.1). Electrical specifications are in section 6.4.8.

USB Function Port

The Sphere II includes a USB Function (or "Client") port. This interface allows the Sphere II to appear as a client device to USB Host devices such as desktop and laptop computers.



The USB Function signals are most easily accessed from mini USB Type B socket J8 (mating face shown at left). The signals are also available on header J12, which permits wiring the USB signals directly to the host USB port as permitted by the USB standard, or to a host connector. Note that only one set of the USB function signals at J8 or J12 should be used at a time.

The Sphere II supports the full USB connection speed (12 Mbit/s). It indicates this to the host device with a 1.5 kΩ pull-up on the USB+ signal.

USB_VCC is power supplied from the host computer and is used by the Sphere II to indicate when a USB cable has been connected. The Sphere II is self-powered (not powered by the USB host) and draws negligible current from the USB_VCC pin.

The Sphere II includes the capability to simulate a Function port cable disconnection. This feature can be used to force the host to re-enumerate the Sphere II to the host USB controller.

4.4.4 Ethernet

The EP9315 includes an integrated 10/100 BT Ethernet controller. The signals run through a physical interface controller and out to RJ-45 socket J7.

Ethernet details and electrical specifications are listed in section 6.4.9.

4.4.5 CAN Bus

CAN bus (Controller Area Network) is a protocol originally developed for the automotive industry that is increasingly being used in industrial control and automation applications. The Sphere II includes a CAN controller suitable for connection to a wide range of CAN networks.

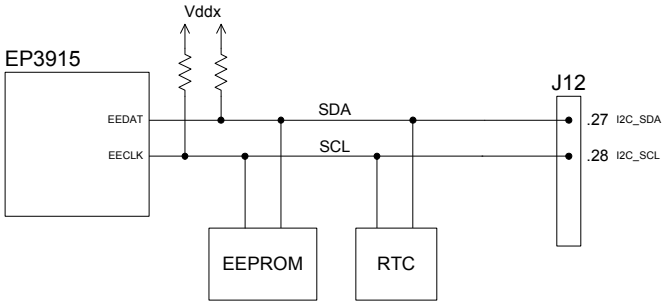
The CAN signals are available on headers J12 and J16. Details and electrical specifications are listed in section 6.4.10.

4.4.6 I²C Bus Master

I²C (Inter-IC) Bus is a multi-master, "two-wire" synchronous serial bus developed by Philips for communications between integrated circuits (ICs). The bus master addresses devices using the data line and provides a synchronous clock for reading and writing devices. Client devices respond only when queried by the master device. Philips has developed many I²C devices, but other organizations have adopted I²C as a convenient means for addressing peripherals in a system.

The Sphere II uses the EP9315 I²C interface to communicate with the real-time clock (section 4.2) and the MAC address EEPROM (section 4.1.3). Applications can also use I²C to communicate with external peripherals.

The following diagram illustrates the I²C architecture on Sphere II. See section 6.4.12 for electrical specifications.



The following table lists the addresses of the I²C devices on the Sphere II.

Device	Address Range	Function
DS1307	0xD0-D1	Real-time clock
24LC08	0x50-57	Ethernet MAC address

Important: The DS1307 supports a maximum bit rate of 100 kbps. Do not use the I²C bus at rates faster than 100 kbps.

4.5 Discrete IOs

This section describes discrete signals on the Sphere II that can be used for measurement and control.

4.5.1 Digital IOs

The EP9315 supplies a number of discrete digital I/Os for Sphere II application use. These are referred to as general-purpose digital inputs and outputs (GPIOs), as each discrete digital signal can be configured as an input or as an output.

The EP9315 signals are grouped into eight ports lettered A through H, each of which includes eight GPIO bits. The GPIO signal cross-reference in section 4.1.6 is a complete list of all EP9315 GPIO ports. Electrical specifications for EP9315 GPIOs are listed in section 6.4.12.

The following table describes the subset of EP9315 GPIOs that are available for use on the Sphere II. The table lists the ports, series resistance, whether the signals include ESD protection, the header number and the primary functions of the port signals on the Sphere II.

# signals	Ports	Series Resistance	ESD prot.	Header	Primary Functions
1	A6	1 kΩ	Y	J4	Vee enable
5	B [7..3]	1 kΩ	Y	J4	
8	C [7..0]	1 kΩ	Y	J11	Keypad row scan
8	D [7..0]	1 kΩ	Y	J11	Keypad column scan
2	G [3..2]	none	N	J12	GPIO

Ports E, G and H are reserved for the IDE interface, though some operating systems may support them as digital IOs as well. They are included for reference below:

2	E [3:2]	none	N	J15	IDE
4	G [7..4]	33 Ω	N	J15	IDE DD[15..12]
8	H [7:0]	33 Ω	N	J15	IDE DD[7..0]

4.5.2 Analog Inputs

It is possible to configure the unused inputs of the touch panel controller (section 4.6) as analog inputs. Because the analog inputs share an A/D converter with the touch panel controller, software drivers must be written carefully to coordinate conversion activity. Contact ADS Sales with details if your application requires analog inputs.

4.5.3 Analog Outputs (PWM)

The Sphere II has two filtered, pulse-width-modulated outputs that serve as analog control outputs. These are used to control LCD backlighting and contrast (section 4.7.2).

4.6 Touch Panel

The Sphere II supports four, five, seven and eight-wire analog resistive touch panels. The touch panel control lines are available on headers J2 and J4.

See section 3.4.2 (J2) for details about interfacing touch panels to the Sphere II. Electrical details are listed in sections 6.4.5 and 6.4.12.

4.7 Display Controller

The EP9315 includes an integrated LCD controller. This section describes how the Sphere II uses that controller to drive logic-level and LVDS LCD displays.

4.7.1 The EP9315 Display Controller

The EP9315 controller uses system memory for the display frame buffer. It can drive VGA (640x480) and SVGA (800x600) displays easily. Larger displays will work, with some possible tradeoffs in overall system performance imposed by the controller architecture.

Key features of the EP9315 controller as used on the Sphere II include:

- Support for 4, 8 and 16 bpp LCDs
- Frame buffer is in system DRAM
- Dual 32 x 32 display data FIFOs
- 256 x 24 bit color lookup table
- Hardware cursor (e.g. for mouse)
- Graphics acceleration for line draw, block copy with transparency and block fill

4.7.2 Using the LCD Display Signals

This section describes the features of the Sphere II used to control LCD displays

LCD Display Voltages

The Sphere II supplies 3.3 V or 5 V power to the LCD display. Select this voltage with JP4 (3.3.4). Please observe the cautions listed with the JP4 settings.

LCD Signals

The LCD signals are driven by the EP9315 controller. The Sphere II LCD signals are named LCD_Pnn, an expansion of the EP9315 convention, Pnn. *LCD_P0* through *LCD_P17*—as well as the pixel clock, vertical sync and horizontal sync—are all electrically buffered. See section 6.4.4 for electrical specifications.

The *PNL_RL* and *PNL_UD* signals are for active (TFT) displays that support changing the scan direction. This feature allows the display to be flipped right-to-left (*RL*) or up-and-down (*UD*) by changing the voltage on these signals. See section 6.4.4 for electrical specifications.

Creating LCD Display Cables

ADS has designed cables for a wide variety of displays. See the list of supported displays on the ADS support forums. Cable drawings for supported displays are available on request.

While ADS does not provide support to customers to create their own cables, designers with LCD display experience may be able to design their own. For those that do so, a key point to keep in mind is that the EP9315 LCD interface maps its display controller pins differently based on LCD technology and color palette size. Consult the EP9315 User's Manual for more information.

LVDS for LCD Displays

The Sphere II includes an LVDS (Low-Voltage Differential Signaling) driver suitable for driving some LCD displays. LVDS multiplexes digital signals together onto differential pairs, yielding the advantage of longer cable lengths, fewer wires and lower radiated noise.

LVDS signals are available on header J5. The table in section 3.4.5 illustrates how the display signals are multiplexed onto the LVDS differential pairs.

Electrical specifications for the LVDS transmitter are provided in section 6.4.4.

Brightness Control (Backlight)

While some LCDs, such as passive transflective displays, can be viewed in daylight without backlighting, most LCD displays include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays.

Panel backlights are driven by backlight inverters. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. Fortunately, most backlight inverters include control signals to dim and turn off the backlight.

The Sphere II supplies two signals for backlight control: BacklightPWM and /BacklightOn. The signals are found on both J3 and J4. BacklightPWM is a filtered PWM signal from the EP9315 that supplies an analog output voltage to control the intensity of the backlight. The /BacklightOn signal is an open-collector output controlled by the system controller CPLD that is used to turn the backlight on and off.

See section 6.4.4 for electrical specifications.

Contrast Control (Vee and Vcon)

Vee and Vcon are used to control the contrast of passive panels. Many passive panels require a positive or negative bias voltage in the range of fifteen to thirty volts to bias the passive LCD display.

Some displays include a Vee generator and simply require a low-voltage analog signal to control the contrast. The Vcon output is a PWM-controlled output that can be used for this purpose. Electrical specifications for Vee and Vcon are listed in section 6.4.4.

The Sphere II includes header J14 to bring in Vee and Vcon from an external source. ADS manufactures an adapter board that can be used for this purpose. Contact your ADS sales representative for details.

4.7.3 Developing Display Drivers

ADS provides display timings for supported displays on request. For displays not yet supported, ADS has a panel configuration service to create panel timings and cable drawings. Contact ADS Sales for further details.

4.8 EMI/RFI and ESD Protection

The Sphere II board incorporates a number of standard features that protect it from electrostatic discharge (ESD) and suppress electromagnetic and radio-frequency interference (EMI/RFI). Transient voltage suppressors, EMI fences, filters on I/O lines and termination of high-frequency signals are included standard on all systems. For details, see electrical specifications for subsystems of interest.

4.8.1 Agency Certifications

Many products using ADS single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. Because ADS supplies only the single-board computer and not fully integrated systems, ADS cannot provide meaningful system-level emissions test results.

The crystal frequencies (section 6.4.13) and electrical specifications listed in Chapter 6 may provide helpful information for agency certifications.

4.8.2 Protecting the Power Supply Inputs

It is the responsibility of the designer or integrator to provide filtering and surge protection on the input power lines. This is especially important if the power supply wires will be subject to EMI/RFI or ESD.

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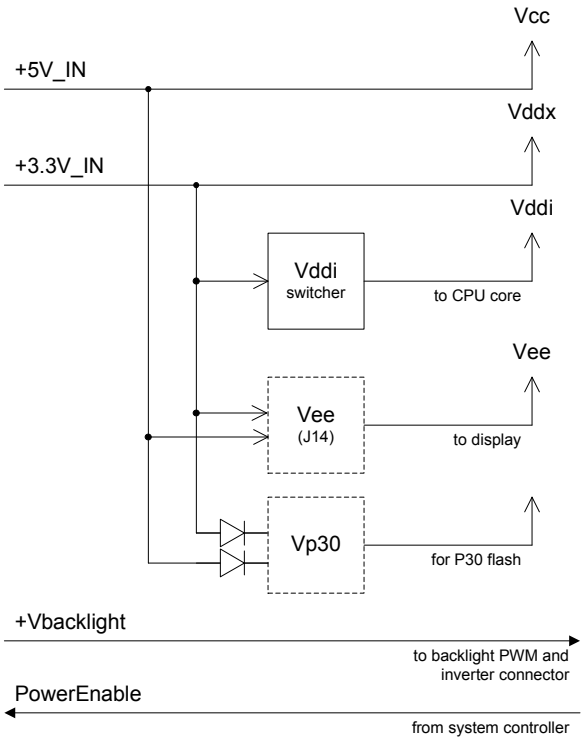
5 Power Supply

This chapter describes the architecture of the Sphere II power supply and factors affecting power consumption. For information about how much power the Sphere II consumes, consult the electrical specifications in section 6.4.2.

5.1 Power Supply Architecture

The Sphere II power supply is organized as shown in the following diagram. Dashed lines indicate options that may be included in some product configurations.



The Sphere II provides software control of Backlight Intensity and On/Off. Power for the backlight is routed through the board from header J17 and is typically 12 or 5 VDC. Vee can be provided by a converter circuit from ADS connected at header J14. See section 4.7.2 for further details about Vee and backlight control.

The PowerEnable signal is an output from the system controller that indicates when the system is running. The PowerEnable signal is available on headers J17 (pin 5) and J4 (pin 28).

Full specifications for the Sphere II power supply are listed in section 6.4.1.

5.2 Designing for Optimal Power Management

Designing a system for optimal power management requires careful attention to many details. This section provides some guidelines and tips for best power management.

5.2.1 Create a Power Budget for Peripherals

Embedded system designers using the Sphere II should have a clear understanding of how power usage will be allocated in the system they design. Designers should create a power budget that takes into account the types of devices that are expected to be used with the Sphere II.

The following lists detail some of the typical external loads that can be placed on the Sphere II power supplies. Baseline power consumption of the Sphere II is listed in section 6.4.2.

5.2.2 3.3 V Loads

3.3 V loads come from both onboard and external devices. Typical loads include the following:

Onboard:

- CPU core voltage (Vddi)
- System logic
- Ethernet

External:

- LCD Display
- CompactFlash cards

5.2.3 5 V Loads

Typical loads on the 5 V power supply include the following:

Onboard:

- IrDA transceiver
- CAN bus

External:

- Display
- USB devices
- Speaker(s)
- Some CompactFlash cards

6 System Specifications

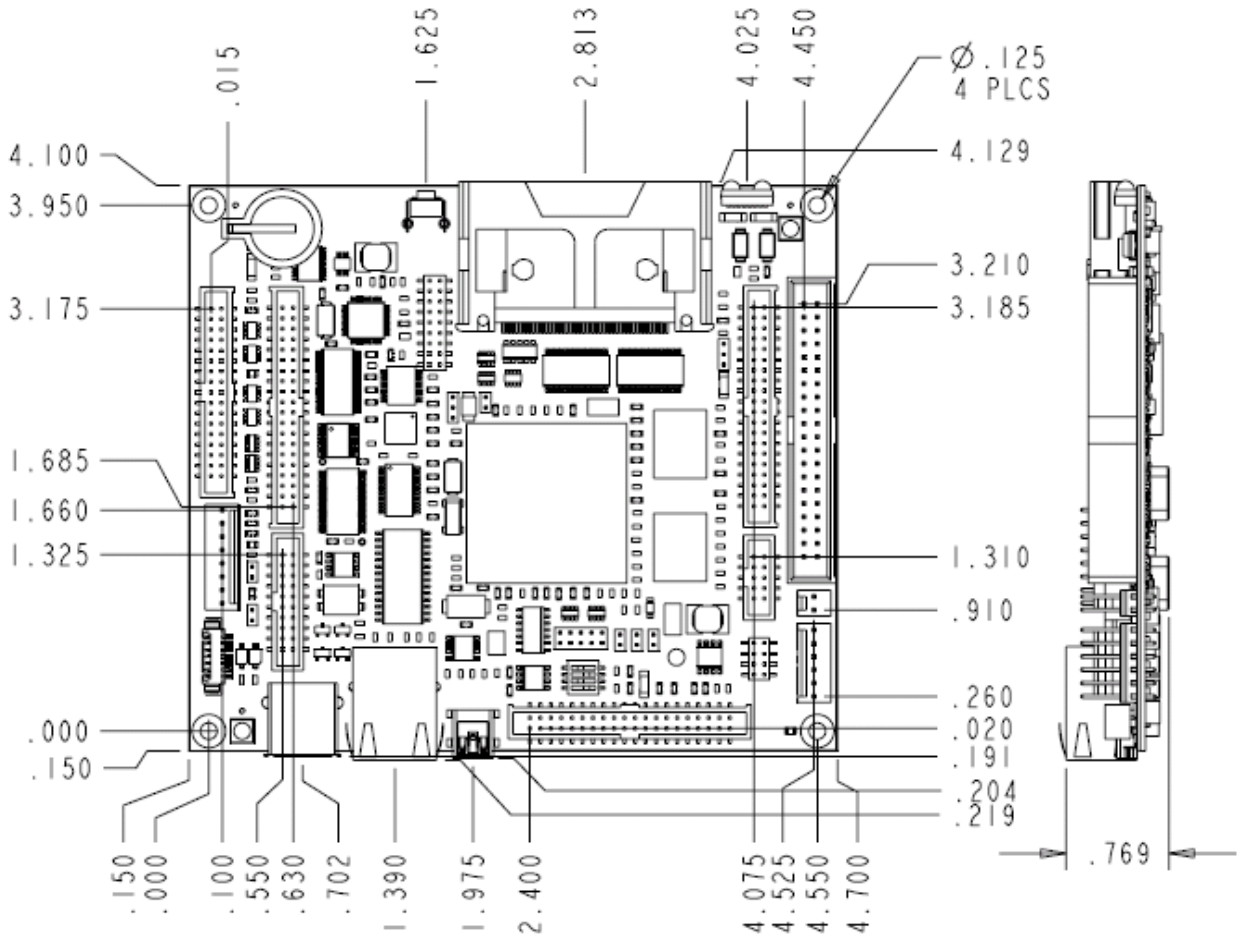
This section describes the mechanical, environmental and electrical specifications of the Sphere II single-board computer. It also lists the options available for volume production orders.

6.1 Mechanical Specifications

The Sphere II is 4.85 by 4.25 inches (123 x 108 mm) in size. This section describes the component dimensions and mounting of the board. Detailed drawings are available on the support forums (section 2.4), and 3D models are available from ADS in electronic format for production customers.

6.1.1 Mechanical Drawing

The following mechanical drawing specifies the dimensions of the Sphere II, as well as locations of key components on the board. All dimensions are in inches. This image is an excerpt from the full mechanical drawings, ADS document number 630119-20001.



6.1.2 Mounting Holes

Four holes are provided, one on each corner, for mounting. The diameter of the holes is 0.125 inches (3mm). Mounting holes are plated through and connected to the Sphere II ground plane.

For reliable ground connections, use locking washers (star or split) when securing a Sphere II in an enclosure. Make sure that washers do not extend beyond the limits of the pads provided.

6.1.3 Clearances

The Sphere II has a low profile. It can fit in an enclosure with inside dimensions as thin as 0.769 inch (19.5 mm).

Selection of connectors and wiring harnesses will determine height of final assembly.

6.2 Volume Production Options

The Sphere II has a number of production options detailed throughout this manual. This section describes some of those options, with an emphasis on those that affect the mechanical design of the board. These options are generally available only for volume production orders.

Connector Plating

ADS can populate headers with pin platings that match your requirements.

5 V Display Buffers

The Sphere II supports a wide range of LCD displays without modification. Standard systems use 3.3 V buffers on the display lines. Some LCD displays require 5 V data for reliable operation (e.g. a 5 V display with Vih>0.65*Vcc). See section 4.7 for details about the LCD controller and section 6.4.4 for electrical specifications.

Five-, Seven or Eight-Wire Touch Panel Header

A different header may need to be installed at J2 to support five-, seven- and eight-wire touch panels. See sections 3.4.2 and 4.6 for further details.

Serial 1: 3.3 V Logic-level

Serial 1 can be configured for 3.3 V logic-level operation. See section 4.4.1 for details.

Serial 1: RI1 connected to EGPIO_EX0

Pin 8 of header J13 (Serial 1 RI signal) can be electrically connected to EGPIO_EX0. The external circuit may need to provide an open-drain signal to drive the RqOnOff circuit, which is also connected to EGPIO_EX0. This connection allows the RI signal from modems to generate an interrupt to the processor.

Serial 2: Select Fixed Serial Mode and Eliminate JP3 Settings

Resistor packs can set a specific mode for Serial 2, eliminating the need to set the shunts on JP3

Serial 2: Remove IrDA Transceiver

If you choose to cable the IrDA signals on J12 to another transceiver, ADS must remove the onboard transceiver to prevent contention between the two receivers.

Serial 3: 3.3 V Logic-level

Serial 3 (4.4.1) can be configured for 3.3 V logic-level operation instead of RS-422/485.

Serial 3: EIA-422/485 Receiver Enable

ADS can configure the EIA-422/485 transceiver's receive-enable to be driven by GPIO3 or independently by GPIO1. See section 4.4.1 for details. Software drivers may need to be updated to support this functionality.

Isolate Mounting Holes from Ground Plane

Standard systems connect the mounting holes to the Sphere II digital ground plane. The mounting holes can be isolated from the digital ground plane by removing a surface-mount shunt at each mounting hole.

6.3 Environmental Specifications

The following are environmental specifications for the Sphere II single-board computer.

Symbol	Parameter	Min	Typ.	Max	Units
	Operating temperature	-40		+85	°C

6.4 Electrical Specifications

This section provides electrical specifications for the Sphere II single-board computer.

6.4.1 Main and Backup Power

The Sphere II runs from externally-provided 5 and 3.3 V DC power. The Sphere II generates additional voltages for onboard use as described in Chapter 5. The 5 V and 3.3 V supplies are available on the Sphere II output connectors and are limited to the current draws specified below.

The 5.0 and 3.3 V power supplies should come up at the same time. If one must come up before the other, bring the 5.0 V supply up first.

The system time is maintained by a DS1307 real-time clock chip. Supply backup power for the RTC chip with long-life 12.5 mm coin cell battery in socket B1 (Panasonic BR1225-1HC or equivalent).

Symbol	Parameter	Min	Typ.	Max	Units
System Power					
5V_IN	5.0 V power input, +/- 5%	4.75	5.0	5.25	V
3.3V_IN	3.3 V power input, +/- 5%	3.15	3.3	3.45	V
VDDI	Processor core voltage (6.4.12)		1.8		V
I (Vcc)	5.0 V available for display and external peripherals (note 1)			500	mA
I (Vddx)	3.3 V available for display, CompactFlash, external peripherals, etc. (Note 1)			500	mA
RTC Backup Power (4.2)					
V BATPOS	real-time clock battery backup	2.2	3.0	3.6	V
I BATPOS	RTC current (note 2)		300	500	nA

Notes:

1. The output power for the 5 and 3.3 V supplies is limited primarily by the external power supply, connectors and trace widths of the printed wiring board.
2. Vddx=0V, Vbatpos=3.2 V (source: DS1307 data sheet)

6.4.2 Power Consumption

The following table lists power consumption for the Sphere II.

Power consumption varies based on peripheral connections, components populated on the system, the level of processor activity and the LCD panel connected. Input voltage and temperature affect power consumption to a lesser extent.

LCD displays and backlights can add significantly to the total power consumption of a system. ADS development systems include the Sharp LQ64D343 5V TFT VGA display, which draws about one watt, and the Taiyo-Yuden LS520 backlight inverter, which draws about six watts at full intensity. By comparison, the Sphere II consumes less than 1.5 W.

Symbol	Parameter		Min	Typ.	Max	Units
I run	System power supply (note 3)	5.0 V		32		mA
				160		mW
		3.3 V		430		mA
				1400		mW

Notes: Power consumption was measured on a fully populated 64 MiB Sphere II with no peripheral connections under the following conditions:

3. System running the Windows CE desktop (<5% CPU utilization)

6.4.3 Reset Input

Absolute Maximum Ratings

Reset Input (RESET_IN)..... 3.6 V (note 4)

Symbol	Parameter	Min	Typ.	Max	Units
Reset_In (J12.2)					
Vrst	trigger voltage (note 5)		2.7		V
Vprst	pull-up voltage		Vddx		V
Rprst	pull-up resistance		47		kΩ

Notes:

4. The reset controller can support operating voltages up to 10 VDC. However, such high voltages on Vddx through the pull-up resistor may damage the system.
5. Short /Reset_In to GND to reset system

6.4.4 Display

LCD display panels have a wide range of voltage and data requirements. The Sphere II has a number of adjustable voltages to support these requirements, as well as controls for brightness (backlight) and contrast (passive panels). See section 4.7 for further details.

The LVDS signals are driven by the National Semiconductor DS90C363A LVDS transmitter. The LCD signals are mapped on LVDS header J5 as shown in section 3.4.5.

Symbol	Parameter	Min	Typ.	Max	Units
LCD (4.7.2)					
V pnl	LCD voltage (note 6)	3.3		5.0	V
P pnl_pwr	LCD power (note 7)			2	W
V pnl_data	LCD data voltage (note 8)	3.3	3.3	5.0	V
Scan Direction (active displays) (3.3.1, 3.3.2)					
R pnl_scan	Pull-up resistance		4.7		kΩ
V pnl_scan	Pull-up voltage	0	V pnl	V pnl	V
Contrast Control (passive displays) (3.4.14, 4.7.2, note 9)					
Vcon	Low-voltage contrast adjust (note 9)	0		1.3	V
Vee	(note 10)				V
Brightness Control (backlight, 4.7.2)					
R backlightOn	Pull-up		10		kΩ
V backlightOn	With pull-up (note 11)			12	V
	Pull-up resistor		47		kΩ
	No pull-up (production option, note 12)			30	V
V backlightPWM	PWM (note 13)	0		5	V
R backlightPWM	PWM series resistance (note 14)		2.2		kΩ
	PWM pull-up resistance		4.7		kΩ
LVDS (4.7.2)					
R term	Termination resistance, each pair		200		Ω
V lvds	Driver power supply		3.3		V

Notes:

6. Jumper JP4 (3.3.4) selects the display voltage.
7. Total power available depends on system power budget.
8. Systems are configured at the factory with buffers for 3.3 or 5 V panel data. Shunt resistors R201 and R202 select the voltage for those buffers. 5 V displays with Vih <= 0.6•Vpnl_pwr=3.0 V will work reliably with 3.3 V data. 3.3 V buffers can be run at 5 V for test purposes, but if your application requires 5 V data, read section 6.2 and contact ADS Sales to ensure the correct buffers are used for your display.
9. Vcon is the filtered, low-voltage PWM signal used to control Vee. It can be used directly with some passive displays to control contrast. Vcon and Vee are generated by the EP9315 "BRIGHT" PWM output. Vcon is the 3.3 V PWM signal RC filtered with a 40% (15k/10kΩ) voltage divider.
10. Vee is provided by an external adapter. See section 4.7.2, "Contrast Control (Vee and Vcon)", for details.
11. The "12 V" voltage is supplied at power header J17, pin 4. The BacklightOn signal is an open-collector output managed by the system controller CPLD.
12. As a production option, the pull-up resistor can be removed for use with an external pull-up resistor. The specification lists the maximum voltage rating of the transistor.
13. The standard configuration for BacklightPWM signal is as an open collector output with a 5 V pull-up. The output can also be factory configured as 5 or 12 V open collector or 3.3 V, push-pull logic output, with or without an output filter capacitor. The "12 V" voltage is supplied at power header J17, pin 4.
14. The backlight PWM output is driven by EP9315 PWMOUT.

6.4.5 Touch Panel Controller

The EP9315 includes a touch panel controller as described in section 4.6. All touch-panel signals are ESD and RF protected. Touch panel signals are located on headers J2 and J4. See section 6.4.12 (EP9315) for touch panel controller electrical specifications.

6.4.6 System Controller

A Xilinx XCR3064XL CPLD on the Sphere II provides logic for chip selects, power management and other system control functions. It is programmed at the factory using the JTAG interface (3.4.10).

Absolute Maximum Ratings

Input voltage, digital I/O pins (note 15) ..... -0.5 to 5.5 V

Output current, continuous,
digital I/O pins ..... -100 to 100 mA

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	Supply voltage		3.3		V
Digital Outputs					
Vol	Iol=8mA			0.4	V
Voh	Ioh=-8mA	2.4			V
Digital Inputs					
Vil	Low-level input voltage			0.8	V
Vih	High-level input voltage	2.0			V

Notes:

15. The XCR3064 has 5V-tolerant inputs.

6.4.7 Asynchronous Serial Ports

The Sphere II supports several asynchronous serial ports as described in section 4.4.1.

Serial ports 1 through 3 are controlled by the EP3915 processor.

EIA-232 signals are generated using charge pump devices (e.g. Sipex SP3222 and SP3243). Signals for 422/485 are buffered with the Maxim MAX491.

Ports configured for 3.3 V logic operation should be treated as EP9315 GPIOs. See section 6.4.12 for specifications.

IrDA signals from the EP9315 are converted to IrDA using a Vishay TFDU6102 infrared transceiver. The TFDU6102 includes a protection circuit that prevents the transmit output from being driven any longer than 80 µs at a time. See section 6.2 for details about using the signals on header J12 for external transceiver.

Symbol	Parameter	Min	Typ.	Max	Units
	Logic voltage, logic serial ports		3.3		V
EIA-432 (4.4.1)					
	Transmit voltage	±5.0	±5.4		V
	Receiver input voltage range	-25		+25	V
	Maximum baud rate	120	235		kbps
EIA-422/485 (4.4.1)					
	Transmitter voltage (note 16)		5.0		V
	Differential input threshold		0.2		V
	Termination resistor (JP8)		120		Ω
IrDA (4.4.1)					
VccRxIrda	Receiver voltage		3.3		V
	Receiver power series resistance		10		Ω
VccTxIrda	Transmitter voltage		3.3		V
	Transmitter series resistance		3.6		Ω
	Transmitter current		330	630	mA

Notes:

16. As a production option, ADS can populate a 3.3 V 422/485 transceiver.

6.4.8 USB

The Sphere II supports USB host and function operation as described in section 4.4.3.

USB Function Port

The USB function port is driven by the Philips PDIUSBD12 controller, while the USB host ports are driven by the EP9315 (6.4.12).

The USB function port runs at 1.5 Mbps and supports simulated disconnection of the USB cable through software control.

USB Host Port

The USB host port will source up to 2 amps before the current limit takes over.

6.4.9 Ethernet

The EP9315 includes an integrated 10/100 Ethernet controller as described in section 4.4.4. The Sphere II adds the Micrel KS8721BL Ethernet physical interface (PHY) and an RJ-45 socket to complete the Ethernet implementation. The Sphere II stores the MAC (Media Access Control) address in an EEPROM connected to the CPU via the I^2C bus (section 4.1.3).

6.4.10 CAN Bus

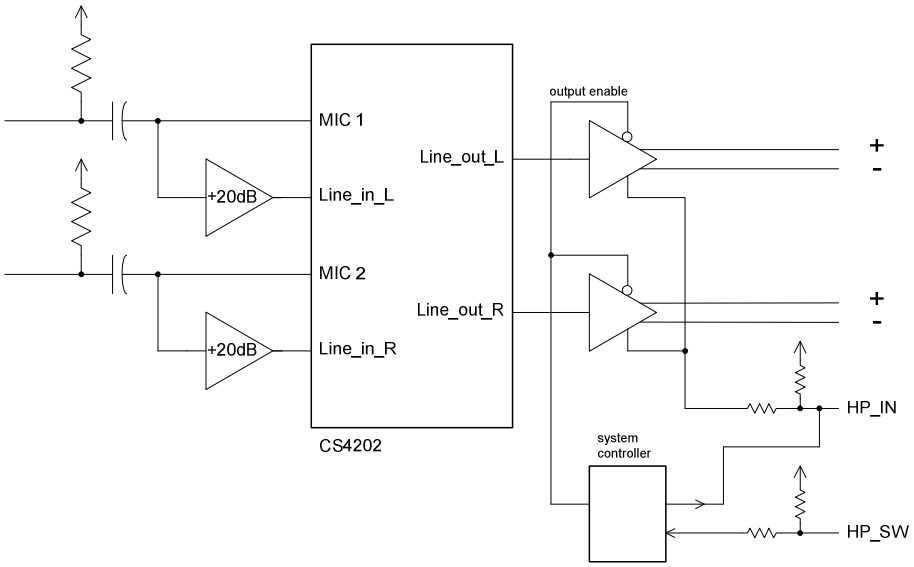
The Sphere II uses the SJA1000T CAN controller with a Philips PCA82C251 CAN transceiver for its CAN bus capabilities.

6.4.11 Audio

For its audio sub-system the Sphere II uses the Crystal CS4202, an AC'97 stereo codec with dual audio input and output channels. The Sphere II adds an output power amplifier (National LM4863LQ) and a microphone pre-amp with power for electret microphones.

The output amplifier supports differential and single-ended modes. When the HP_IN signal is greater than V(HP_IN), the amplifier is in single-ended mode; when lower, it is in differential mode. This system allows the HP_IN signal to be controlled by an inserted headphone plug, as described in section 4.3.2. The HP_SW allows programmatic control of the speaker mode.

The following diagram illustrates the relationship of the Sphere II signal amplifiers to the codec:



The Sphere II microphone circuitry can be factory configured to support "line in" inputs (1 Vrms with no electret pull-ups) and different input gain and filtering. If a special configuration is needed for your project, consult ADS Sales with information about your requirements.

Absolute Maximum Ratings

Vin_mic .....5 Vdc

Symbol	Parameter	Min	Typ.	Max	Units
DVdd	codec digital supply voltage		3.3		V
Avdd	codec analog supply voltage		5.0		V
fso	sample rate, output		48		kHz
fsi	sample rate, input (note 17)	8		44.1	kHz
Audio Input					
Vin_mic	signal input voltage		100		mV_{rms}
Gain_mic	pre-amp gain		20		dB
fo_mic	pre-amp low-pass cutoff (note 18)		3.4		kHz
Rin_mic	input impedance		12.5		kΩ
Cin_mic	DC blocking capacitor		1		µF
Vmicpwr	microphone power (MIC_L/R+)		5		V
Rmicpwr	microphone power, series resistance			3.2	kΩ

Symbol	Parameter	Min	Typ.	Max	Units
Audio Output					
Rl	speaker load	4	8		Ω
Vout	Zspkr=4Ω, differential mode			3.7	V_{rms}
Vdc	DC bias, differential mode		0.5		Avdd
Pspkr	output power, ea. channel (note 19)				
	differential, THD+N 1%, Rl 4Ω		1.0	2.2	W
	differential, THD+N 10%, Rl 4Ω		1.0	2.7	W
	differential, THD+N 1%, Rl 32Ω		1.0	0.34	W
	single-ended, THD+N 0.5%, Rl 32Ω		75	85	mW
	single-ended, THD+N 1%, Rl 8Ω			340	mW
	single-ended, THD+N 10%, Rl 8Ω			440	mW
R HP_IN	pull-up to Vcc			100	kΩ
V HP_IN	threshold voltage		4		V

Notes:

17. The output sample rate is fixed, but the input sample rate can be set to 8, 11.025, 22.05 or 44.1 kHz.
18. Pre-amp anti-aliasing filter rolls off at 3dB/octave (first-order filter)
19. Typical values are guaranteed to National Semiconductor's AOQL (Average Outgoing Quality Level). Operating above typical values for a sustained period of time may result in thermal shutdown of the amplifier.

6.4.12 EP9315 Processor (GPIO, I²C, SPI, Touch Panel)

The ARM core of the EP9315 is powered by low voltage supply Vddi (6.4.1) to achieve low power consumption at high clock rates. External interface pins of the EP9315 are powered by the Vddx (3.3 V) power supply.

Serial ports configured for 3.3 V logic operation run directly to the processor (section 4.4.1). These lines should be treated as digital I/Os and protected for over-current and over-voltage accordingly.

The EP9315 GPIO lines are powered by the Sphere II's "Vddx" supply. Most Sphere II GPIOs include a combination of series resistance and ESD protection. See the table in section 4.5.1 for values used.

Absolute Maximum Ratings

Input voltage, digital I/O pins..... -0.3 to 3.6 V

Output current per pin ..... +/-50 mA

Symbol	Parameter	Min	Typ.	Max	Units
RVdd	EP9315 digital I/O power		3.3		V
Digital Outputs					
Vol	Low-level output voltage, Iol=4mA			0.5	V
Voh	High-level output voltage, Ioh=-4mA	2.8			V
Ioh4	CF, UART, VEEPWM			4	mA
Ioh8	DD, IDE, I2C, ROW, COL			8	mA
Ioh12	GRNLED, SPI			12	mA
Digital Inputs					
Vil	Low-level input voltage			1.2	V
Vih	High-level input voltage	2.1			V
Rp	Input pull-up resistance (note 20)				kΩ
I2C Bus (4.4.6, note 21)					
Rbus	pull-up on SDA, SCK		1.82		kΩ
Vbus			3.3		V
	bus clock (note 22)		n/a		kHz
	buffer size (note 22)		n/a		byte
SPI Port (4.4.2)					
	Base bit rate, internal clock		3.6864		MHz
	Divisor for Internal clock	1		4096	
	Clock rate, external source			13	MHz
Touch Panel Controller (4.6, 6.4.5)					
Vdd	Supply voltage		RVdd		V
	A/D sample resolution		12		bit

Notes:

20. When configured as inputs, Cirrus Logic EP9315 digital I/Os enable 3.3V software pull-ups. Unconnected pins will read logic high when configured as inputs. The impedance of these pull-ups is not current ly published in the Cirrus Logic literature.
21. The I²C bus lines do not include surge protection. Consider adding protection if the bus will be exposed to external handling.
22. The EP9315 does not include a hardware I²C interface. Bus timing and data buffering is dependent on software drivers.

6.4.13 Crystal Frequencies

Agencies certifying the Sphere II for compliance for radio-frequency emissions typically need to know the frequencies of onboard oscillators. The following table lists the frequencies of all crystals on the board.

Crystal	Device	Typ.	Units
X1	AC'97 codec	24.576	MHz
X2	EP9315 core	14.7456	MHz
X3	EP9315 RTC	32.768	kHz
X4	RTC	32.768	kHz
X5	USB function controller	6.000	MHz
X6	CAN controller	16.000	MHz
X7	Ethernet PHY	25.000	MHz

6.4.14 CompactFlash

CompactFlash control logic is managed by the EP9315 microcontroller. The data and address signals run through bi-directional 74LVC16224x buffers to CompactFlash socket J9, while the EP9315 control signals connect directly to the CompactFlash socket. All CompactFlash signals are ESD protected.

The specifications below apply to the buffered data lines. See section 6.4.12 (EP9315) for electrical specifications of the control lines.

Absolute Maximum Ratings

Input voltage, port I/O pins ..... -0.5 to 6.5 V

Socket output current .....1.25 A

Output current, any pin ..... +/-50 mA

Total continuous current, all pins ..... +/-100 mA

Symbol	Parameter	Min	Typ.	Max	Units
Vddx	Data buffer power		3.3		V
CardVcc	Socket output voltage (note 23)	3.3	5.0	5.0	V
I CardVcc	Socket output current (note 24)			1	A
Rp	CD, VS and BVD pull-ups (note 25)				kΩ
Vp	CD, VS and BVD pull-up voltage		3.3		V
Vesd	ESD MIL-STD-883, method 3015	2000			V
	ESD machine model (C=200pF,R=0)	200			V
Digital Outputs					
Vol	Iol=0.1mA, Vcc=3.3V			0.2	V
	Iol=6mA, Vcc=3.0V			0.55	V
Voh	Ioh=-0.1mA, Vcc=3.3V	3.1			V
	Ioh=-6mA, Vcc=3.0V	2.4			V
Digital Inputs					
Vil	Low-level input voltage			0.8	V
Vih	High-level input voltage (note 26)	2.0		5.0	V

Notes:

23. The CompactFlash port supply voltage is selected programmatically by the system controller.
24. Current limits shown is based primarily on the power switch settings, but are also dictated by the external power supply, trace widths and the socket pins themselves.
25. These lines are pulled high by pull-ups internal to the EP9315.
26. The data lines are 5 V tolerant

7 Board Revision History

7.1 Identifying the board revision

The product revision number of the Sphere II is etched on the underside of the printed circuit board. That number is 170119-2000x, where "x" is the board revision.

7.2 Revision History

The following is an overview of the revisions of the Sphere II printed wiring board (PWB).

7.2.1 Revision 1

The following are differences from revision A of the ADS Sphere (170116-9000A), which is sometimes referred to as Sphere I.

New Features

Onboard battery socket for real-time clock

Support for Intel P30 flash

Production option to replace JP3 to set Serial 2 mode

Enhancements

Surface-mount headers for improved manufacturability

ESD protection on I^2C lines

Changes

Size is slightly larger to add battery holder and surface-mount headers.

Height profile is 0.100 inches (2.5 mm) smaller

Placement and spacing of headers is slightly different.

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