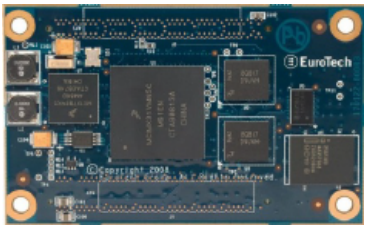
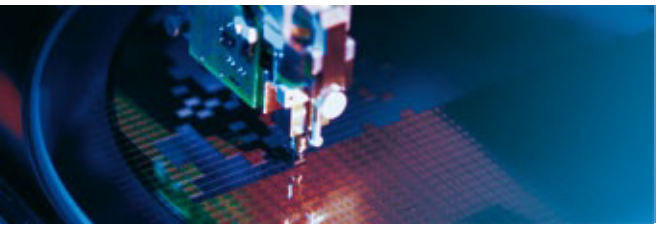
DESIGN–IN GUIDE





Turbo G5 Module

Rev. 1 - April 2009

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Revision History

Issue no.	*PWB*	*Date*	*Comments*
0		Feb-2009	Created from (100122-8002B) Turbo G5 PB Design Specification (Jan-2009)
1		Apr-2009	Initial release

For contact details, see page 71.

Contents

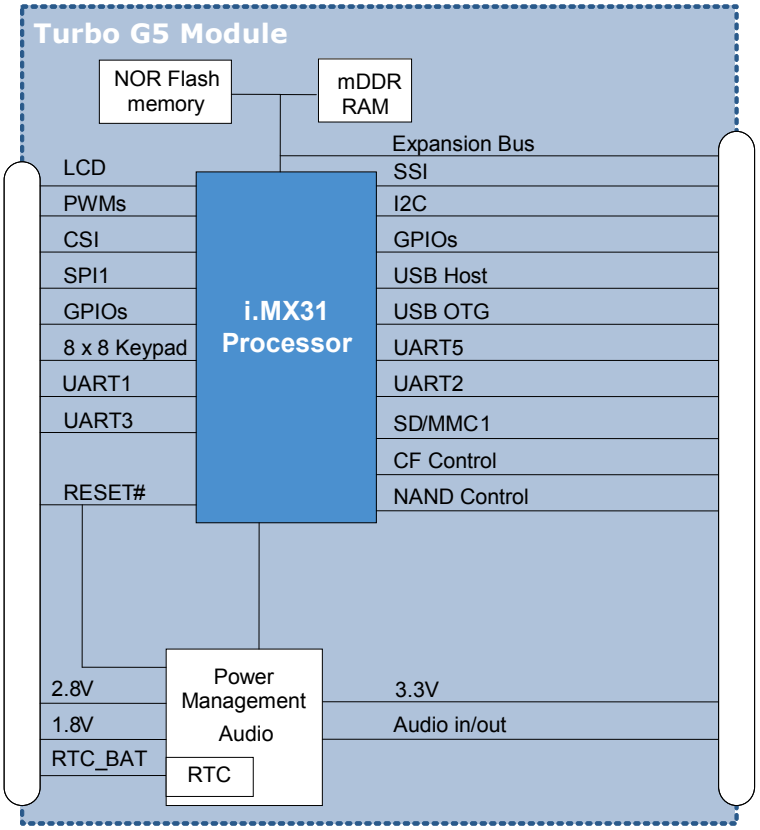
Introduction

The Turbo G5 is a full-featured, general-purpose computing module based on the Freescale™ i.MX31 multimedia applications processor. An application-specific carrier board integrates with the Turbo G5 module for a complete system. With unique customization capabilities, the processor module integrates readily with a wide range of carrier boards to meet customers' specific design requirements.

This guide provides details about the various features of the Turbo G5 module and guidelines for carrier board design. It extends the information provided in the Turbo G5 Development System User Manual and is intended for hardware design engineers and software developers. Design details apply to the revision listed in Appendix C – Board Revision, page 68.

Block Diagram

The following diagram illustrates the system organization of the Turbo G5 module. This module is highly-configurable and supports a variety of hardware interface options. Those hardware interfaces shown in the diagram are an example of one possible *Interface Set*. For further details about *Interface Sets*, see Hardware Interface Options, page 17.



Handling Your Board Safely

Anti-Static Handling

The Turbo G5 module contains CMOS devices that could be damaged by electrostatic discharge (ESD). Observe industry-standard electronic handling procedures when handling the module. Where possible, work on a grounded anti-static mat. At a minimum, touch an electrically-grounded object before handling the module or touching any components on the module.

Packaging

Please ensure that, should a module need to be returned to Eurotech, it is adequately packed, preferably in the original packing material.

Electromagnetic Compatibility

The Turbo G5 module is classified as a component with regard to the European Community Electromagnetic Compatibility (EMC) regulations. Because Eurotech supplies only the single-board computer and not fully integrated systems, Eurotech cannot provide meaningful system-level emissions test results. It is the responsibility of the user to ensure that systems using the module are compliant with the appropriate EMC standards.

RoHS Compliance

The European RoHS Directive (Restriction on the use of certain Hazardous Substances – Directive 2002/95/EC) limits the amount of six specific substances within the composition of the product. The Turbo G5 module fully complies with the RoHS directive. A full *RoHS Compliance Materials Declaration Form* for the Turbo G5 module is included as Appendix B – RoHS Compliance, page 67. Further information regarding RoHS compliance is available on the Eurotech web site at www.eurotech.com.

Conventions

The following table lists the symbols used in this document.

Symbol	Explanation
	Note – information that requires your attention
	Warning – proceeding with a course of action may damage your equipment or result in loss of data

The following table describes the conventions for registers used in this document.

Symbol	Explanation
RW	readable and writable register
W	write only register
R	read only register

The following table describes the conventions for signal names used in this document.

Convention	Explanation
GND	digital ground plane
#	active low signal

The following table describes the abbreviations for direction and electrical characteristics of a signal used in this document.

Type	Explanation
I	signal is an input to the system
O	signal is an output from the system
IO	signal may be input or output
P	power and ground
OD	open-drain
GPIO	general-purpose input and output
GPI	general-purpose input
GPO	general-purpose output
AI	analog input
AO	analog output
3.3	3.3 V signal level
2.8	2.8 V signal level
1.8	1.8 V signal level
PWM	Pulse width modulation
nc	no connection
reserved	use is reserved to Eurotech

Features

Turbo G5 Module

Processor

Turbo G5 bases its architecture on the 32-bit Freescale i.MX31 ARM RISC processor. This multimedia applications processor offers high-performance processing optimized for low power consumption.

The following are key features of the processor:

- Maximum clock rate of 532 MHz
- 133 MHz DDR memory bus
- 16 KB instruction and 16 KB data L1 cache
- 128 KB L2 cache
- 16 KB embedded SRAM
- Vector Floating Point hardware unit
- Hardware Video Acceleration (encode)
- Integrated 2-D and 3-D graphics with support for OpenGL-ES and Direct3D-Mobile

Mobile Double Data Rate RAM

Mobile Double Data Rate RAM (mDDR-RAM) is used on the Turbo G5 module for system main memory and frame buffer memory. Standard modules include 128 MB with an increased memory of 256 MB available as a volume production option.

Flash Memory

Flash memory provides non-volatile data storage on the Turbo G5 module. The standard configuration is 32 MB using an x16 NOR flash memory device. An increased flash memory of 64 MB is available as a volume production option. Eurotech systems store the operating system, applications, and system configuration settings in the on-board flash. This flash memory is also the default boot device. For additional boot options, see Boot Interface Selection, page 13.

Real-Time Clock

The Turbo G5 module includes a real-time clock (RTC) function. It retains the system date and time when the system is powered down as long as backup power is provided to the module. For general specifications, see Real-Time Clock, page 65.

Expandability via Carrier Board

The Turbo G5 module is highly-configurable and supports a variety of hardware interface options. The following interfaces are supported by the Turbo G5 module:

- one parallel LCD (up to 18-bit)
- two PWM
- two SD/MMC
- one CompactFlash®
- one PCMCIA
- five serial ports
- one I2C (master or slave)
- two SPI (master or slave)
- one Camera Sensor (up to 16-bit)
- two SSI (Synchronous Serial Interface) for I2S or AC97 implementation
- one 4-wire touchscreen controller
- one 5-wire touchscreen controller
- two USB 2.0 Host
- one USB 2.0 Client
- one USB OTG
- one NAND flash
- one Keypad (up to 8x8)
- one “1-wire” for battery, security device, or serial EEPROM communication
- one SIM (Subscriber’s Identification Module)
- one ATA for IDE or ATAPI drives
- one CAPTURE/COMPARE timer input
- one Tamper Detection Switch
- many GPIOs
- one 16- or 32-bit expansion interface for Ethernet, CAN, FPGA, etc.

Notes:

Due to iMX31 I/O multiplexing considerations, not all interfaces may be supported simultaneously.

Some external circuitry may be needed on the carrier board.

Some interfaces require a custom BSP. For descriptions of these interfaces, see Other Interfaces, page 43.

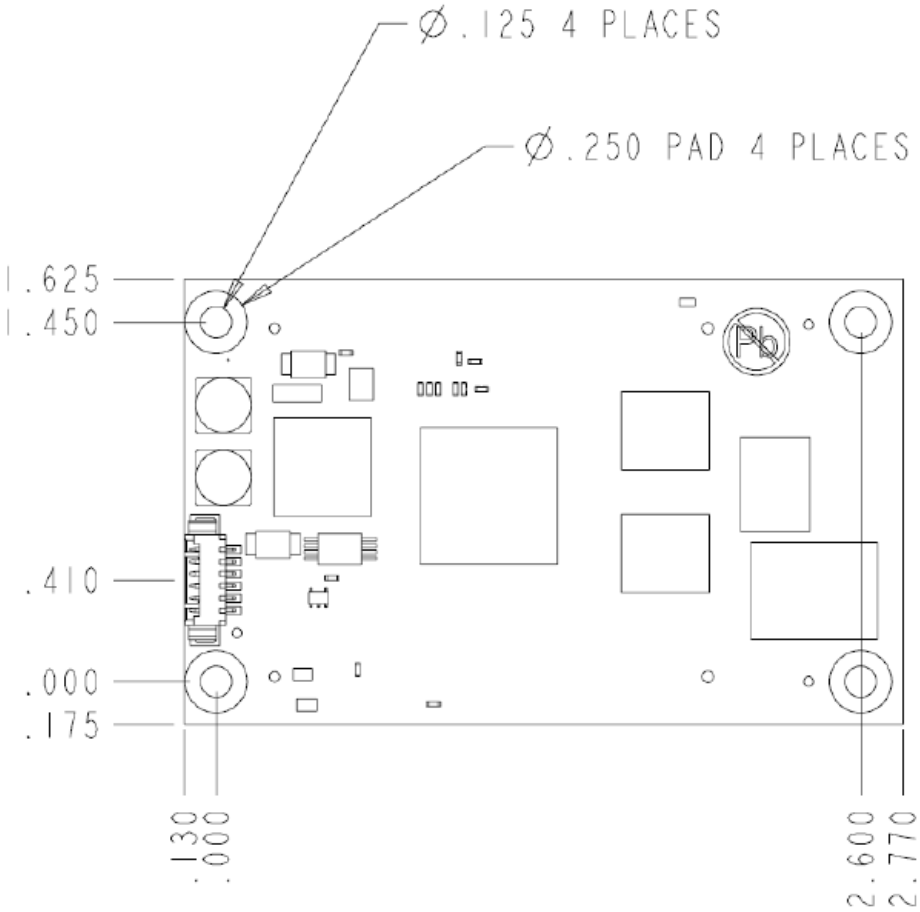
Power Supply

The Turbo G5 module requires a single power supply with a nominal voltage of 3.3 V. The module generates all other necessary power supplies locally and provides 1.8 V and 2.8 V to the carrier board.

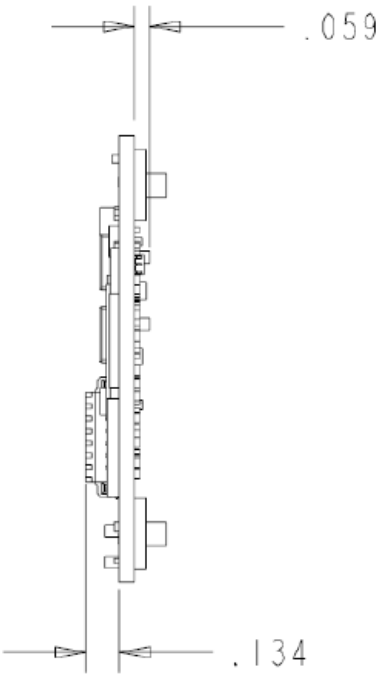
Mechanical

Locations of key components on the module are presented in the following diagrams. All dimensions are in inches.

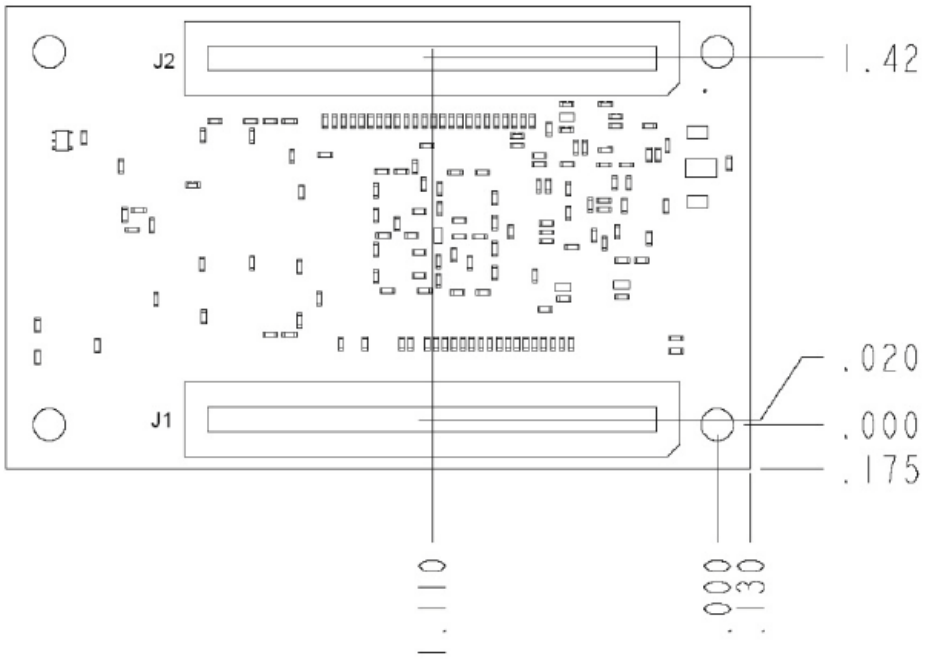
The first view illustrates the top side of the module.



The second view illustrates the side view of the module.



The third view illustrates the bottom side of the module.



Mounting Holes

Four holes located in the corners of the module enable mounting on the carrier board. The module ground plane connects electrically to the mounting holes. For reliable ground connections, use locking washers when securing a module to a carrier board. Make sure that washers do not extend beyond the limits of the pads provided.

Installing and Removing the Turbo G5 Module

The Turbo G5 module connects to a carrier board through two high-density, surface mount sockets. The following procedures describe how to install and remove the module from a carrier board.

Warning: Observe industry-standard electronic handling procedures when handling the module. The connectors expose signals on the system bus that do not have ESD protection.

Installing the Turbo G5 Module

Follow these steps to install a module onto a carrier board:

1. Connect a grounding wrist strap to your hands.
2. Place the carrier board on an ESD mat.
3. Holding the module by the edges with the processor facing up, align connector J1 and connector J2.
4. Gently press downward on the edge of the module to engage the two connectors on the underside of the module.

Removing the Turbo G5 Module

Follow these steps to detach a module from a carrier board:

1. Connect a grounding wrist strap to your hands.
2. Place the carrier board with module on an ESD mat.
3. Gently lift the edges until the module releases from the two connectors.

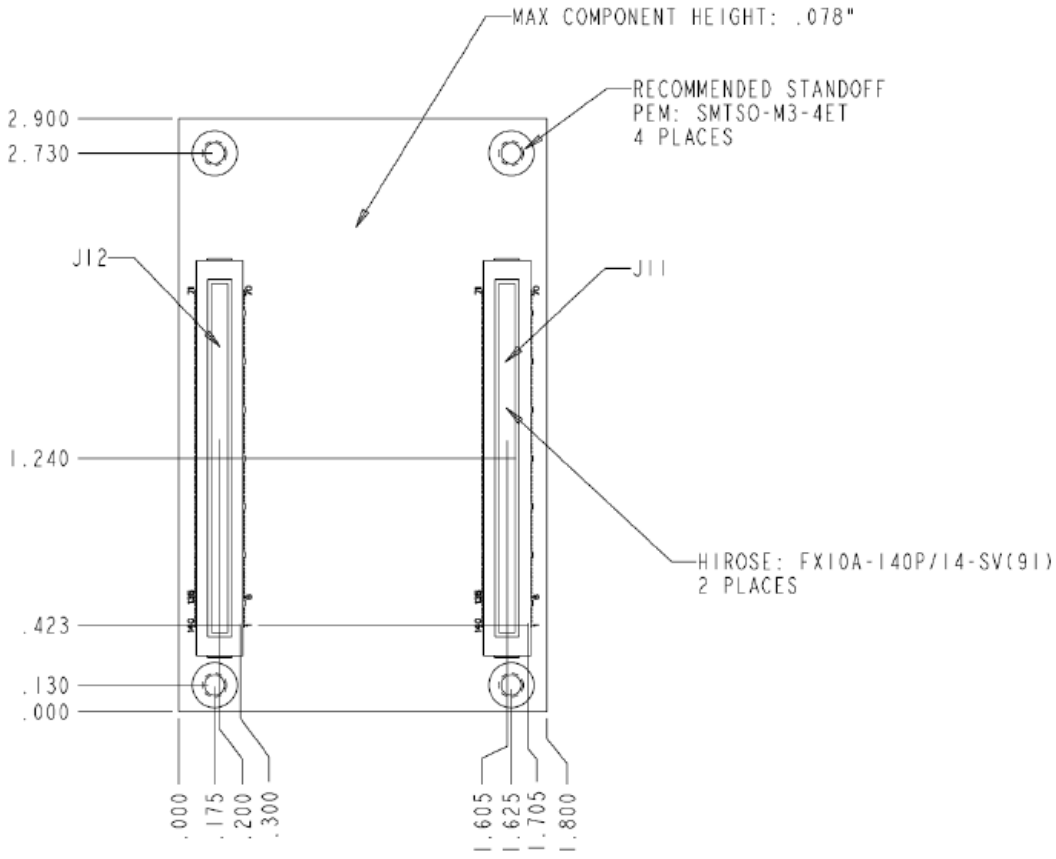
Carrier Board Design Considerations

This section describes the necessary considerations required for a successful Turbo G5 module-based system.

Mechanical

To ensure proper mating with the Turbo G5 module, every compatible Turbo G5 carrier board must provide a mechanically-constrained area in which to install the module.

The following mechanical drawing specifies all necessary details.



According to the preceding drawing, a compatible carrier board design requires the following three mechanical features:

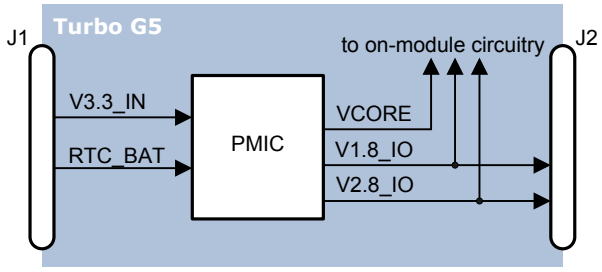
1. Height-restricted area with a maximum component height of 0.078 inches. The area is rectangular-shaped with dimensions as shown in the drawing.
2. Four plated mounting holes electrically connected to the common signal reference (GND).
   Use holes that accommodate metric M3 screws. Eurotech recommends soldering one surface mount metal standoff in each mounting hole, as shown in the drawing.
3. Two connectors for power and signal connections between the module and the carrier board.
   Connector J11 interfaces with the module's J1 connector, while connector J12 interfaces to the module's J2 connector. The coordinates of each connector's origin is at the respective pin 1, as shown in the drawing. For the pinouts of the two connectors, see Docking Connectors, page 47.

Power and Power Management

Today's mobile applications demand high-end graphics and extensive computations with minimal power consumption. Power management is especially critical in high-performance systems where power is at a premium. The Turbo G5 module is designed specifically for low-power, computationally-intensive multimedia applications. This section provides details about the power supply architecture and power management.

Turbo G5 Module Power Supply Architecture

The following diagram illustrates the power supply architecture of the Turbo G5 module.



The module requires one main input voltage, referenced as V3.3_IN, supplied by the carrier board. An on-module Power-Management IC (PMIC) generates the core voltage and all other voltages required by the i.MX31 processor and supporting circuitry.

The module has two interface power domains: 1.8 V and 2.8 V. Each signal available on the module connectors belongs to one of the two power domains. Voltage level-shifting circuitry may be required on a carrier board for proper system integration. The module provides power supply outputs from each of the power domains, referenced as V1.8_IO and V2.8_IO, to reference the carrier board and to power the level-shifting circuitry. For detailed specifications, see Power Specification, page 63.

In addition to the main input voltage, the Turbo G5 module requires backup power for its RTC function. For general specifications, see Real-Time Clock, page 65.

Turbo G5 Carrier Board Power Supply

The Turbo G5 carrier board power supply and distribution scheme depends on your specific system requirements for power supply voltage range, as well as your required peripheral set.

Note: When power is turned on, your carrier board power supply design must meet the following two requirements:

- V3.3_IN must reach $V_{V3.3\_IN\ min}$ monotonically.
- V3.3_IN must reach $V_{V3.3\_IN\ min}$ in less than 50 ms.

For specifications for V3.3_IN, see Power Supply, page 63.

Power Management

To reduce power consumption, the Turbo G5 module uses several power management techniques including dynamically changing the processor's frequency based on the application demand. In addition, the iMX31 processor supports several "active" power-saving modes reducing power consumption when the system is not at full operation. The processor also supports one "inactive" mode, referenced as Sleep mode, in which the processor is static in a low power state and the mDDR RAM is in Self Refresh mode. For the power consumption in Sleep mode, see Power Specification, page 63.

The power management signal P_EN generated by the Turbo G5 module is very important for your carrier board design. This signal is available on connector J1, pin 86 and is used to enable power to the peripheral circuitry on the carrier board. A low logic-level indicates that the module is in Sleep mode. Conversely, a high logic-level on P_EN indicates the module is in one of its "active" modes. Utilizing the P_EN signal in a carrier board design helps reduce the Sleep power consumption of the system.

Boot Interface Selection

The Turbo G5 module supports two boot interface options. Selection of a boot interface option is made using the state of the UBOOT# signal (connector J2, pin 104) during the low-to-high transition of the RESET# signal.

The following table defines the boot options.

Boot Option	UBOOT#
Flash Boot	1 (default)
Serial Boot	0

Flash Boot

If Flash Boot is selected, the module will boot from one of the following three devices, depending on its manufacturing option: on-module NOR flash, on-carrier-board NAND flash, or on-carrier-board SD/MMC flash card.

Flash Device	Location
NOR on Chip Select 0	Module (standard option)
8-bit NAND (Large Block Device) 8-bit NAND (Small Block Device) 16-bit NAND (Large Block Device) 16-bit NAND (Small Block Device) SD/MMC card	Carrier board (volume production options)

Serial Boot

If Serial Boot is selected, the module will execute protocol for boot using its UART1 or its USB Client interfaces. For further details, contact your local Eurotech representative.

JTAG

The Turbo G5 module provides all required signals for JTAG interface support on J1: Docking Connector, page 47. This interface is available for factory programming and test, as well as for software debugging. It is not supported for application use.

A 10kΩ pull-up resistor to 2.8 V on the module's TDO signal (connector J1, pin 132) is required.

Often the carrier board includes additional devices with JTAG interfaces which must be accessible for test or debugging purposes. One example is a CPLD. The following are two design approaches to such a requirement.

JTAG Design Approach 1

Keep different JTAG interfaces separate, and provide separate JTAG connectors for the Turbo G5 module and the additional devices on the carrier board. This is a straight-forward approach which is recommended if board space and cost constraints are met.

JTAG Design Approach 2

Daisy-chain the Turbo G5 module and the additional JTAG devices on the carrier board. This approach is more economical; however, it adds complexity and could make some JTAG solutions inoperable due to their lack of support for multiple JTAG devices chain. Verify with your JTAG solutions vendor that the JTAG chain can be usable in all intended modes for the particular application. The following important issues must be addressed for a successful JTAG daisy chain design:

- The module's JTAG interface operates with 2.8 V signal levels only. Voltage level-shifting might be required depending on the additional JTAG device's requirements. Notice that adding buffers has an impact on setup and hold timing of the JTAG interface and should be carefully examined.

- The SJC_MOD signal (connector J1, pin 6) selects one of two modes for the iMX31 JTAG interface. In these modes, the iMX31 is represented as different numbers of JTAG devices. The modes are selected based on the state of the SJC_MOD signal during the low-to-high transition of the JTAG reset signal TRST#. Mode 0 (SJC_MOD = '0' during the low-to-high transition of TRST#) is used for software debugging, and it also could be used for factory programming. In this mode, the processor itself provides four JTAG daisy-chained TAP controllers. The JTAG chain is not IEEE1149.1 compliant so accessing other JTAG devices on the carrier board could be impaired while the processor is in this mode. Mode 1 (SJC_MOD = '1' during the low-to-high transition of TRST#) is used for boundary scan purposes. In this mode, the processor provides one JTAG TAP controller. The JTAG chain is IEEE1149.1 compliant.

For additional information, refer to the i.MX31 and i.MX31L Applications Processors Reference Manual, rev. 2.4, 12/2008.

Hardware Interface Options

Most of the iMX31 I/O pads can be configured to work in more than one functional mode, often part of a different interface. The number of hardware interfaces simultaneously used is always less than the number of hardware interfaces supported by the processor specification. System software, usually the operating system (OS), determines the end-use mode for each I/O pad. The Turbo G5 module exposes most of this flexibility enabling integration with a wide range of application-specific carrier boards.

In every application-specific carrier board design, the system requirements determine the number and type of required interfaces. However, the first step of the design process must be a feasibility check to ensure that the required number and type of interfaces meet the following constraints:

- The Turbo G5 module can directly provide the required interfaces.
- The required interfaces can function simultaneously.

Following this approach will yield an optimal system solution in terms of BOM cost, risk, development time, and power consumption.

Example:

If the system requirements demand five UART interfaces, the Turbo G5 module can accommodate that requirement directly. However, if a USB Client interface is required in addition to the five UARTs then extra controller logic will be necessary on the carrier board to implement either a UART or USB Client functionality. Extra controller logic is required because the Turbo G5's UART4 and USB Client functions are mutually exclusive. That is the module can provide either five UART interfaces or up to four UART interfaces and one USB Client interface.

There are many possible combinations of I/O pads configured for a particular Turbo G5 module end-use mode. Each such combination defines an *Interface Set*. Because the number of possible *Interface Sets* is large, a large number of customized Board Support Packages (BSPs) are required. In order to minimize the effort of supporting multiple BSPs, Eurotech has constructed the so-called "Standard Turbo G5 BSP", referenced as Standard BSP. The Standard BSP is capable of supporting a number of pre-defined *Interface Sets*, if means of proper hardware identification are provided. Each *Interface Set* that is not supported by the Standard BSP will require a custom BSP.

The following table depicts three possible hardware *Interface Sets* that have been given random names: Main, 2 x SD, and ATA.

Interface Set		
Standard BSP Support		Custom BSP Support
Main	2 x SD	ATA
1 x SD	2 x SD	1 x SD
1 x CF		1 x CF
1 x PWM	2 x PWM	1 x PWM
4 x UART	4 x UART	3 x UART
	1 x 1-wire interface	
1 x I^2C	1 x I^2C	
1 x SPI	1 x SPI	1 x SPI
1 x LCD	1 x LCD	1 x LCD
1 x CSI	1 x CSI	
1 x USB HOST	1 x USB HOST	1 x USB HOST
1 x USB OTG		1 x USB OTG
1 x AC97	1 x PMIC Audio	1 x AC97
1 x NAND	1 x NAND	1 x NAND
DIO: 7 x GPIO 5 x GPI 2 x GPO		16 x GPIO
8 x 8 Keypad	8 x 8 Keypad	4 x 4 Keypad
		1 x ATA
1 x Touchscreen	1 x Touchscreen	1 x Touchscreen
2 x Ethernet	2 x Ethernet	
2 x CAN 2.0	2 x CAN 2.0	

"Main" and "2 x SD" *Interface Sets* are supported by the Standard BSP. A carrier board design based on these two *Interface Sets* will be supported by the same OS binary image. The "ATA" *Interface Set* requires a custom OS binary image.

Each *Interface Set* is a combination of discrete interfaces. The Standard BSP supports *Interface Sets* that are built of Turbo G5-standard interfaces only. For a full list of the Turbo G5-standard interfaces, see Standard Interfaces on page 19. If your application requires a custom BSP, contact your local Eurotech representative.

Expansion Bus

The iMX31 WEIM interface is available on the module connectors as a general-purpose expansion bus. The Expansion Bus provides the following features:

- 26-bit address bus
- 16-bit data bus
- WEIM chip select signals 1, 3, 4 and 5

Note: A special 32-bit WEIM mode is available as a volume production option. This option enables 32-bit multiplexed address/data accesses using the iMX31 CS3# signal. If your application requires this option, contact your local Eurotech representative.

The Expansion Bus is used to provide access to several Standard Interfaces and features that are required by the Standard BSP. These include CompactFlash, NAND flash, CAN, and Ethernet, as well as required memory-mapped registers. For further details about these registers, see System Registers and Memory Map, page 58.

Also, the Expansion Bus provides powerful expansion capability especially for systems designed to work with a custom BSP. The type of device controllers that can be connected to this bus is virtually unlimited. Examples include other processors, FPGAs, and ASICs.

Standard Interfaces

The hardware interfaces described in this section are building blocks of any *Interface Set* designed to work with the Standard BSP. For a complete description of *Interface Sets*, see Hardware Interface Options, page 13. All interface signals are available on J1: Docking Connector, page 47 and J2: Docking Connector, page 52.

For details about System Registers, see Standard Carrier Board, page 57.

Note: Only *Turbo G5 Standard Carrier Board* designs, that are ones that will rely on the Standard BSP, must comply with the full specification of hardware interfaces as provided in this section. Custom carrier board designs have more flexibility because they require a specialized custom BSP.

Example:

The SDMMC1 interface can be a part of either a standard or custom carrier board; however, only the standard carrier board design requires that the interface's "card detect" signal is routed to the Turbo G5 module's GPIO3_0, as well as that the GPIO System Register is implemented and its GPI5 bit is connected to the interface's "write protect" signal.

LCD Interface - LCD

The Turbo G5 module supports one RGB digital LCD interface of up to 18 data bits, as described in the following table.

Turbo G5 Signal Name	LCD Interface Use
LD0..17	RGB digital data
FPSHIFT	Sample clock
HSYNC	Line sync
VSYNC3	Frame sync
DRDY0	Data valid

Requirements

- PWM2
  The PWM2 output is reserved for backlight brightness control.
- SYS_ID0 System Register bit: LCD
  One designated SYS_ID0 System Register bit, LCD, identifies the presence or absence of the LCD interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bits: LCD_ON and LCDBL_ON
  Two designated PCTRL System Register bits are required. LCD_ON controls the LCD power supply switch, while LCDBL_ON controls the backlight power state, if needed. For descriptions of these bits, see Power Control Register, page 61.

Exceptions

- PWM2 cannot be used as a general-purpose PWM interface.

PWM1 Interface – PWM1

The Turbo G5 module supports the Pulse Width Modulation (PWM) output, as described in the following table.

Turbo G5 Signal Name	PWM1 Interface Use
PWMO	PWM1

Requirements

- SYS_ID0 System Register bit: PWM1
  One designated SYS_ID0 System Register bit, PWM1, identifies the presence or absence of the PWM1 interface. For a description of this bit, see System Identification Registers, page 59.

Exceptions

- PWM1 is mutually exclusive with the following interfaces:
  - DIO
  - ATA

PWM2 Interface – PWM2

The Turbo G5 module supports the Pulse Width Modulation (PWM) output, as described in the following table.

Turbo G5 Signal Name	PWM2 Interface Use
CONTRAST	PWM2

Requirements

- SYS_ID0 System Register bit: PWM2
  One designated SYS_ID0 System Register bit, PWM2, identifies the presence or absence of the PWM2 interface. For a description of this bit, see System Identification Registers, page 59.
  Exceptions
- PWM2 is mutually exclusive with the LCD.
  When the LCD interface is present, PWM2 is used for LCD backlight intensity control.

I²C Interface – I2C

The Turbo G5 module supports the I2C interface, as described in the following table.

Turbo G5 Signal Name	I2C Interface Use
I2C_SCL	Clock
I2C_SDA	Data

Requirements:

- SYS_ID1 System Register bit: I2C
  One designated SYS_ID1 System Register bit, I2C, identifies the presence or absence of the I²C interface. For a description of this bit, see System Identification Registers, page 59.
- Pull-up Resisters
  Both signals must be pulled up to 1.8V using 1kΩ resistors.

Exceptions:

- I2C is mutually exclusive with the ATA interface.

Secure Digital/MultiMediaCard Interface 1 – SDMMC1

The Turbo G5 module supports the Secure Digital/MultiMediaCard (SD/MMC) interface for memory and I/O expansion, as described in the following table.

Turbo G5 Signal Name	SDMMC1 Interface Use
SD1_CLK	Clock
SD1_CMD	Command
SD1_D0	Data 0
SD1_D1	Data 1
SD1_D2	Data 2
SD1_D3	Data 3
GPIO3_0	Card detect

Requirements

- SYS_ID0 System Register bit: SDMMC1
  One designated SYS_ID0 System Register bit per SD/MMC interface is required. SDMMC1 identifies the presence or absence of the SDMMC1 interface. For a description of this bit, see System Identification Registers, page 59.
- Voltage translation
  If voltage translation is needed for the SDMMC1 interface, Eurotech recommends the use of a Texas Instruments® TXS0108E buffer or similar device.
- GPIO3_0
  Signal GPIO3_0 is used as the card detect for the SDMMC1 interface. This signal is active low-level and must always be pulled-up, even if the interface is not required.
- GPIN5
  The write protect switch for SDMMC1 is accessible using the GPIO System Register bit GPIN5. For a description of this bit, see GPIO Register, page 62. Depending on the input circuit, this signal may need to be pulled-up or pulled-down.

Exceptions

- None

Secure Digital/MultiMediaCard Interface 2 – SDMMC2

The Turbo G5 module supports the Secure Digital/MultiMediaCard (SD/MMC) interface for memory and I/O expansion, as described in the following table.

Turbo G5 Signal Name	SDMMC2 Interface Use
PC_CD2_B	Clock
PC_CD1_B	Command
PC_WAIT	Data 0
PC_READY	Data 1
PC_VS1	Data 2
PC_PWRON	Data 3
GPIO3_1	Card detect

Requirements

- SYS_ID0 System Register bit: SDMMC2
  One designated SYS_ID0 System Register bit per SD/MMC interface is required. SDMMC2 identifies the presence or absence of the SDMMC2 interface. For a description of this bit, see System Identification Registers, page 59.
- Voltage translation
  If voltage translation is needed for the SDMMC2 interface, Eurotech recommends the use of a Texas Instruments® TXS0108E buffer or similar device.
- GPIO3_1
  Signal GPIO3_1 is used as the card detect for the SDMMC2 interface. This signal is active low-level and must always be pulled-up, even if the interface is not required.
- GPIN6
  The write protect switch for SDMMC2 is accessible using the GPIO System Register bit GPIN6. For a description of this bit, see GPIO Register, page 62. Depending on the input circuit, this signal may need to be pulled-up or pulled-down.

Exceptions

- SDMMC2 is mutually exclusive with CF.

CompactFlash® Interface - CF

The Turbo G5 module supports one CompactFlash® (CF) interface for memory and I/O expansion. The Turbo G5 module provides designated control signals for the CF interface, as described in the following table. The CF interface also uses a part of the Expansion Bus.

Turbo G5 Signal Name	CF Interface Use	
PC_CD1_B	CD1#	see CompactFlash® specification
PC_CD2_B	CD2#	
PC_WAIT	WAIT#	
PC_READY	READY	
IOIS16	IOCS16#	
PC_RST	RESET	
A15	CE1#	
A14	CE2#	
EB1	IORD#	
OE	IOWR#	
LBA	OE#	
RW	WE#	
EB0	REG#	
A0..10 (shared)	A0..10	
D0..15 (shared)	D0..15	
PC_PWRON	Socket power sense	
PC_RW	Buffer control	
PC_POE	Buffer control	

Requirements:

- SYS_ID0 System Register bit: CF
  One designated SYS_ID0 System Register bit, CF, identifies the presence or absence of the CF interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bit: CF_ON
  One designated PCTRL System Register bit, CF_ON, controls the CF interface power supply switch, if needed. For a description of this bit, see Power Control Register, page 61.
- CTRL System Register bit: CF_RST
  One designated CTRL System Register bit, CF_RST, resets the CF interface. For a description of this bit, see Control Register, page 62.
- Buffer
  Use a Texas Instruments® SN74LV4320A buffer or similar device.

Exceptions:

- CF is mutually exclusive with SDMMC2.

Serial Interface 1 - UART1

The Turbo G5 module supports the UART1 interface, as described in the following table.

Turbo G5 Signal Name	UART1 Interface Use
RXD1	RxD
TXD1	TxD
RTS1	CTS
CTS1	RTS
DTR_DTE1	DTR
DSR_DTE1	DSR
RI_DTE1	RI
DCD_DTE1	DCD

Requirements:

- SYS_ID0 System Register bit: UART1
  One designated SYS_ID0 System Register bit, UART1, identifies the presence or absence of the UART1 interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bit: COM1_EN
  One designated PCTRL System Register bit, COM1_EN, controls power to the UART1 interface, if needed. For a description of this bit, see Power Control Register, page 61.

Exceptions

- None

Note: The i.MX31 processor uses the naming convention for DCE, while the Turbo G5 module uses the naming convention for DTE. In J2: Docking Connector, page 52 the RTS/CTS names switch. Use the function listed in the Interface Use column for a carrier board design.

Serial Interface 2 - UART2

The Turbo G5 module supports the UART2 interface, as described in the following table.

Turbo G5 Signal Name	UART2 Interface Use
RXD2	RxD
TXD2	TxD
RTS2	CTS
CTS2	RTS

Requirements:

- SYS_ID0 System Register bit: UART2
  One designated SYS_ID0 System Register bit, UART2, identifies the presence or absence of the UART2 interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bit: COM2_EN
  One designated PCTRL System Register bit, COM2_EN, controls power to the UART2 interface, if needed. For a description of this bit, see Power Control Register, page 61.
- RTS2
  If UART2 is not used or if RTS/CTS control is not used, RTS2 should not be left floating.

Exceptions

- None

Note: The i.MX31 processor uses the naming convention for DCE, while the Turbo G5 module uses the naming convention for DTE. In J2: Docking Connector, page 52 the RTS/CTS names switch. Use the function listed in the Interface Use column for a carrier board design.

Serial Interface 3 - UART3

The Turbo G5 module supports the UART3 interface, as described in the following table.

Turbo G5 Signal Name	UART3 Interface Use
CSPI3_MOSI	RxD
CSPI3_MISO	TxD
CSPI3_RDY	RTS
CSPI3_SCLK	CTS

Requirements:

- SYS_ID0 System Register bit: UART3
  One designated SYS_ID0 System Register bit, UART3, identifies the presence or absence of the UART3 interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bit: COM3_EN
  One designated PCTRL System Register bit, COM3_EN, controls power to the UART3 interface, if needed. For a description of this bit, see Power Control Register, page 61.
- RXD3 and RTS3
  RXD3 and RTS3 should not be left floating if neither of the following options is used: SPI3, UART3, 4WTS, or 5WTS.

Exceptions

- UART3 is mutually exclusive with the following interfaces:
  - 4WTS
  - 5WTS
  - SPI3

Note: The i.MX31 processor uses the naming convention for DCE, while the Turbo G5 module uses the naming convention for DTE. In J2: Docking Connector, page 52 the RTS/CTS names switch. Use the function listed in the Interface Use column for a carrier board design.

Serial Interface 4 - UART4

The Turbo G5 module supports the UART4 interface, as described in the following table.

Turbo G5 Signal Name	UART4 Interface Use
USBOTG_DATA3	RxD
USBOTG_DATA4	TxD
USBOTG_DATA0	RTS
USBOTG_DATA5	CTS

Requirements:

- SYS_ID0 System Register bit: UART4
  One designated SYS_ID0 System Register bit, UART4, identifies the presence or absence of the UART4 interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bit: COM4_EN
  One designated PCTRL System Register bit, COM4_EN, controls power to the UART4 interface, if needed. For a description of this bit, see Power Control Register, page 61.
- RXD4 and RTS4
  If UART4 and USBO/USBC/USBH2 are not used, RXD4 and RTS4 should not be left floating.

Exceptions

- UART4 is mutually exclusive with the USBO/USBC/USBH2 interface.

Note: The i.MX31 processor uses the naming convention for DCE, while the Turbo G5 module uses the naming convention for DTE. In J2: Docking Connector, page 52 the RTS/CTS names switch. Use the function listed in the Interface Use column for a carrier board design.

Serial Interface 5 - UART5

The Turbo G5 module supports the UART5 interface, as described in the following table.

Turbo G5 Signal Name	UART5 Interface Use
PC_BVD1	RxD
PC_BVD2	TxD
PC_VS2	CTS
PC_RST	RTS

Requirements:

- SYS_ID0 System Register bit: UART5
  One designated SYS_ID0 System Register bit, UART5, identifies the presence or absence of the UART5 interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bit: COM5_EN
  The designated PCTRL System Register bit, COM5_EN, controls power to the UART5 interface, if needed. For a description of this bit, see Power Control Register, page 61.
- RXD5 and RTS5
  If UART5 is not used, RXD5 and RTS5 should not be left floating.

Exceptions

- The UART5 hardware flow control, CTS and RTS, is mutually exclusive with CF.

Note: The i.MX31 processor uses the naming convention for DCE, while the Turbo G5 module uses the naming convention for DTE. In J2: Docking Connector, page 52 the RTS/CTS names switch. Use the function listed in the Interface Use column for a carrier board design.

SPI1 Master – SPI1M

The Turbo G5 module supports the SPI Master interface, as described in the following table.

Turbo G5 Signal Name	SPI1 Master Interface Use
CSPI1_SCLK	Clock
CSPI1_SS0	Enable
CSPI1_MISO	Data input
CSPI1_MOSI	Data output

Requirements:

- SYS_ID1 System Register bit: SPI1
  One designated SYS_ID1 System Register bit, SPI1, identifies the presence or absence of the SPI1M interface. For a description of this bit, see System Identification Registers, page 59.
- CSPI1_MISO
  If SPI1M is not used, CSPI1_MISO should not be left floating.

Exceptions:

- SPI1M is mutually exclusive with SPI1S.

Camera Sensor Interface - CSI

The Turbo G5 module supports a digital camera sensor interface (CSI) of up to 16 data bits, as described in the following table.

Turbo G5 Signal Name	CSI Use
CSI_D0..15	Digital data
CSI_MCLK	Master clock
CSI_PIXCLK	Pixel clock
CSI_HSYNC	Horizontal (line) sync
CSI_VSYNC	Vertical (frame) sync

Requirements:

- SYS_ID1 System Register bit: CSI
  One designated SYS_ID1 System Register bit, CSI, identifies the presence or absence of the CSI interface. For a description of this bit, see System Identification Registers, page 59.
- CSI can be programmed in various modes depending on the imaging sensor with which it couples. The Standard Interface CSI is designed to work with 8-bit ITU.BT 656 type sensor interface with embedded SAV/EAV. This interface requires that the imager's control registers are accessible using the I^2C interface.

Exceptions:

- CSI is mutually exclusive with ATA.

AC97 Audio and Touchscreen Controller Combo – AC97

The Turbo G5 module supports an AC97 audio CODEC/touchscreen controller, as described in the following table. This interface also uses the i.MX31 SSI4 port.

Turbo G5 Signal Name	AC97Use
SCK4	Clock
SFS4	Frame
SRXD4	Data receive
STXD4	Data transmit
GPIO1_1	Pen interrupt
GPIO1_2	AC97 interrupt

Requirements:

- SYS_ID1 System Register bit: AC97
  One designated SYS_ID1 System Register bit, AC97, identifies the presence or absence of an AC97 audio CODEC/touchscreen controller. For a description of this bit, see System Identification Registers, page 59.
- AC97 Audio CODEC/Touchscreen Controller
  One Wolfson Microelectronics® WM9712 CODEC / touchscreen controller chip is required on the carrier board connected to SSI4.
- PCTRL System Register bit: AUD_ON
  One designated PCTRL System Register bit, AUD_ON, controls the carrier board audio power amplifier On/Off control, if needed. For a description of this bit, see Power Control Register, page 61.
- CTRL System Register bit: AC97_RST
  One designated CTRL System Register bit, AC97_RST, resets the CODEC/touchscreen controller chip. For a description of this bit, see Control Register, page 62.
- GPIO1_1
  Signal GPIO1_1 is used as an interrupt input from the touchscreen controller.
- GPIO1_2
  Signal GPIO1_2 is used as an interrupt input from the CODEC.

Exceptions:

- AC97 is mutually exclusive with the following interfaces:
  - PMICA
  - I2S
  - 4WTS
  - 5WTS

PMIC Audio - PMICA

The Turbo G5 module supports an alternative audio interface through an on-module PMIC chip, as described in the following table.

Turbo G5 Signal Name	PMICA Use
SCK4	Do not connect!
SFS4	Do not connect!
SRXD4	Do not connect!
STXD4	Do not connect!
MICL	Microphone input, Left
MICR	Microphone input, Right
LOUTL	Line-output, Left
LOUTR	Line-output, Right

Requirements:

- SYS_ID1 System Register bit: PMICA
  One designated SYS_ID1 System Register bit, PMICA, identifies the presence or absence of the PMIC Audio. For a description of this bit, see System Identification Registers, page 59.
- The Turbo G5 module must be configured for the PMICA option.
- SSI4
  SSI4 signals should be unconnected on the carrier board.
- PCTRL System Register bit: AUD_ON
  One designated PCTRL System Register bit, AUD_ON, controls the carrier board audio power amplifier On/Off control, if needed. For a description of this bit, see Power Control Register, page 61.

Exceptions:

- PMICA is mutually exclusive with the following interfaces:
  - AC97
  - I2S

4-wire Touchscreen Controller – 4WTS

The Turbo G5 module supports a 4-wire touchscreen controller (4WTS), as described in the following table.

Turbo G5 Signal Name	4WTS Use
CSPI3_SCLK	Clock
CSPI3_SS0	Enable
CSPI3_MISO	Data: Input (default) / Output
CSPI3_MOSI	Data: Output (default) / Input
GPIO1_1	Pen interrupt

Requirements:

- SYS_ID0 System Register bit: 4WTSC
  One designated SYS_ID0 System Register bit, 4WTSC, identifies the presence or absence of the 4-wire touchscreen controller. For a description of this bit, see System Identification Registers, page 59.
- Touchscreen Controller
  One Texas Instruments ® ADS7846 touchscreen controller chip is required on the carrier board connected to CSPI3 signals (SPI3).
- GPIO1_1
  Signal GPIO1_1 is used as an interrupt input from the touchscreen controller.
- CSPI3_MISO
  CSPI3_MISO should not be left floating if neither of the following options is used: SPI3M, SPI3S, UART3, 4WTS and 5WTS.

Exceptions:

- 4WTS is mutually exclusive with the following interfaces:
  - UART3
  - AC97
  - SPI3M
  - SPI3S

5-wire Touchscreen Controller – 5WTS

The Turbo G5 module supports a 5-wire touchscreen controller (5WTS), as described in the following table.

Turbo G5 Signal Name	5WTS Use
CSPI3_SCLK	Clock
CSPI3_SS0	Enable
CSPI3_MISO	Data: Input (default) / Output
CSPI3_MOSI	Data: Output (default) / Input
GPIO1_1	Pen interrupt

Requirements:

- SYS_ID0 System Register bit: 5WTPC
  One designated SYS_ID0 System Register bit, 5WTPC, identifies the presence or absence of 5-wire touchscreen controller. For a description of this bit, see System Identification Registers, page 59.
- Touchscreen Controller
  One Texas Instruments ® ADS7845 touchscreen controller chip is required on the carrier board connected to CSPI3 signals (SPI3).
- GPIO1_1
  Signal GPIO1_1 is used as an interrupt input from the touchscreen controller.
- CSPI3_MISO
  CSPI3_MISO should not be left floating if neither of the following options is used: SPI3M, SPI3S, UART3, 4WTS and 5WTS.

Exceptions:

- 5WTS is mutually exclusive with the following interfaces:
  - UART3
  - AC97
  - SPI3M
  - SPI3S

USB Host - USBH

The Turbo G5 module supports a USB 2.0 Host interface, as described in the following table.

Turbo G5 Signal Name	USB Host Interface Use
USBH2_CLK	ULPI Clock
USBH2_DIR	ULPI Direction
USBH2_NXT	ULPI Next
USBH2_STP	ULPI Stop
USBH2_D0..7	ULPI Data

Requirements:

- SYS_ID0 System Register bit: USBH
  One designated SYS_ID0 System Register bit, USBH, identifies the presence or absence of the USB Host. For a description of this bit, see System Identification Registers, page 59.
- ULPI Transceiver
  One Philips® ISP1504 ULPI transceiver chip is required on the carrier board.
- PCTRL System Register bit: USBH_EN
  One designated PCTRL System Register bit, USBH_EN, controls the ULPI transceiver power state (enabled/disabled). For a description of this bit, see Power Control Register, page 61.
- CTRL System Register bit: USBH_RST
  One designated CTRL System Register bit, USBH_RST, resets the ULPI transceiver. For a description of this bit, see Control Register, page 62.

Exceptions:

- USBH is mutually exclusive with the SSI6.

USB On-The-Go, Client, or Second Host – USBO, USBC, or USBH2

The Turbo G5 module supports one USB 2.0 OTG interface, as described in the following table. Under software control, this interface can function as an On-The-Go, a Client, or a second Host interface.

Turbo G5 Signal Name	USBO/C/H2 Use
USBO_CLK	ULPI Clock
USBO_DIR	ULPI Direction
USBO_NXT	ULPI Next
USBO_STP	ULPI Stop
USBO_D0..7	ULPI Data

Requirements:

- SYS_ID0 System Register bit: USBO
  One designated SYS_ID0 System Register bit, USBO, identifies the presence or absence of the USBO/C/H2 interface. For a description of this bit, see System Identification Registers, page 59.
- ULPI Transceiver
  One Philips® ISP1504 ULPI transceiver chip is required on the carrier board.
- PCTRL System Register bit: USBO_EN
  One designated PCTRL System Register bit, USBO_EN, controls the ULPI transceiver power state (enabled/disabled). For a description of this bit, see Power Control Register, page 61.
- CTRL System Register bit: USBO_RST
  One designated CTRL System Register bit, USBO_RST, resets the ULPI transceiver. For a description of this bit, see Control Register, page 62.

Exceptions:

- USBO, USBC and USBH2 are mutually exclusive.
- USBO and UART4 are mutually exclusive.
- USBC and UART4 are mutually exclusive.
- USBH2 and UART4 are mutually exclusive.

NAND Flash Interface - NANDF

The Turbo G5 module supports one NAND flash storage device on the carrier board with an 8- or 16-bit interface. As a volume production option, the NAND flash chip can be supported as a boot-up media. For further details about the boot options, see Boot Interface Selection, page 15. The NAND flash interface requires parts of the Expansion Bus, as well as the designated signals listed in the following table.

Turbo G5 Signal Name	NANDF Use
NFCE	Chip enable
NFALE	Address latch enable
NFCLE	Command latch enable
NFnRE	Read enable
NFnWE	Write enable
NFRnB	Ready/busy
NFnWP	Write protect

Requirements:

- SYS_ID1 System Register bit: NANDF
  One designated SYS_ID1 System Register bit, NANDF, identifies the presence or absence of a NAND flash device. For a description of this bit, see System Identification Registers, page 59.
- NAND Flash
  One Micron® MT29F1G08 NAND flash chip or a similar device is required on the carrier board.

Exceptions

- None

Ethernet 1 – ETH1

The Turbo G5 module supports a 10/100 Ethernet interface. This ETH1 interface requires parts of the Expansion Bus, as well as the designated signals listed in the following table.

Turbo G5 Signal Name	ETH1 Use
GPIO1_3	Interrupt input

Requirements:

- SYS_ID1 System Register bit: ETH1
  One designated SYS_ID1 System Register bit, ETH1, identifies the presence or absence of the Ethernet 1 interface. For a description of this bit, see System Identification Registers, page 59.
- Ethernet Controller
  One SMSC® LAN9116 Ethernet controller chip is required on the carrier board. Its registers are accessible using 16-bit read and write cycles within physical address range 0xB6000000..0xB60000FE. The chip's FIFOs are accessible using 16-bit read and write cycles within physical address range 0xB6000100..0xB6000106.
- CTRL System Register bit: ETH1_RST
  One designated CTRL System Register bit, ETH1_RST, resets the Ethernet controller chip. For a description of this bit, see Control Register, page 62.

Exceptions

- None

Ethernet 2 – ETH2

The Turbo G5 module supports a 10/100 Ethernet interface. This ETH2 interface requires parts of the Expansion Bus, as well as the designated signals listed in the following table.

Turbo G5 Signal Name	ETH2 Use
GPIO1_4	Interrupt input

Requirements:

- SYS_ID1 System Register bit: ETH2
  One designated SYS_ID1 System Register bit, ETH2, identifies the presence or absence of the Ethernet 2 interface. For a description of this bit, see System Identification Registers, page 59.
- Ethernet Controller
  One SMSC® LAN9116 Ethernet controller chip is required on the carrier board. Its registers are accessible using 16-bit read and write cycles within physical address range 0xB6800000..0xB68000FE. The chip's FIFOs are accessible using 16-bit read and write cycles within physical address range 0xB6800100..0xB6800106.
- CTRL System Register bit: ETH2_RST
  One designated CTRL System Register bit, ETH2_RST, resets the Ethernet controller chip. For a description of this bit, see Control Register, page 62.

Exceptions

- None

8x8 Keypad - KEYPAD

The Turbo G5 module supports an 8x8 keypad, as described in the following table.

Turbo G5 Signal Name	KEYPAD Use
KEY_COL0..7	Columns
KEY_ROW0..7	Rows

The Turbo G5 module configures the KEY_ROWn lines as inputs with software pull-ups enabled and configures the KEY_COLn lines as outputs set to "1" (logic-level high). The Turbo G5 module detects, de-bounces, and decoding one or multiple keys pressed simultaneously on the keypad.

Requirements:

- SYS_ID1 System Register bit: 8X8KP
  One designated SYS_ID1 System Register bit, 8X8KP, identifies the presence or absence of a keypad. For a description of this bit, see System Identification Registers, page 59.

Exceptions:

- KEYPAD is mutually exclusive with ATA.

CAN 1 – CAN1

The Turbo G5 module supports a CAN 2.0B interface. This CAN1 interface requires parts of the Expansion Bus, as well as the designated signals listed in the following table.

Turbo G5 Signal Name	CAN1 Use
GPIO3_30	Interrupt input

Requirements:

- SYS_ID1 System Register bit: CAN1
  One designated SYS_ID1 System Register bit, CAN1, identifies the presence or absence of the CAN 1 interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bit: CAN_ON
  One designated PCTRL System Register bit, CAN_ON, controls the CAN1 and CAN2 interfaces' power supply switch, if needed. For a description of this bit, see Power Control Register, page 61.
- CAN Controller
  One Philips® SJA1000T CAN controller chip is required on the carrier board. It is accessible using 16-bit read and write cycles within physical address 0xB7000000 for address latching and 0xB7000004 for data.
- CTRL System Register bit: CAN1_RST
  One designated CTRL System Register bit, CAN1_RST, resets the CAN controller. For a description of this bit, see Control Register, page 62.

Exceptions:

- CAN1 is mutually exclusive with ATA.

CAN 2 – CAN2

The Turbo G5 module supports a CAN 2.0B interface. This CAN2 interface requires parts of the Expansion Bus, as well as the designated signals listed in the following table.

Turbo G5 Signal Name	CAN2 Use
GPIO3_31	Interrupt input

Requirements:

- SYS_ID1 System Register bit: CAN2
  One designated SYS_ID1 System Register bit, CAN2, identifies the presence or absence of the CAN 2 interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bit: CAN_ON
  One designated PCTRL System Register bit, CAN_ON, controls the CAN1 and CAN2 interfaces' power supply switch, if needed. For a description of this bit, see Power Control Register, page 61.
- CAN Controller
  One Philips® SJA1000T CAN controller chip is required on the carrier board. It is accessible using 16-bit read and write cycles within physical address 0xB7800000 for address latching and 0xB7800004 for data.
- CTRL System Register bit: CAN2_RST
  One designated CTRL System Register bit, CAN2_RST, resets the CAN controller. For a description of this bit, see Control Register, page 62.

Exceptions:

- CAN2 is mutually exclusive with ATA.

1-Wire Interface – 1WI

The Turbo G5 module supports a 1-wire interface, as described in the following table. It provides a low-speed, single-wire bidirectional communication bus.

Turbo G5 Signal Name	1WI Use
GPIO2_17	Main

Requirements:

- SYS_ID1 System Register bit: 1WI
  One designated SYS_ID1 System Register bit, 1WI, identifies the presence or absence of the 1-Wire interface. For a description of this bit, see System Identification Registers, page 59.

Exceptions:

- 1WI is mutually exclusive with DIO.

Digital I/O Interface - DIO

The Turbo G5 supports a Digital I/O (DIO) interface, as described in the following table.

Turbo G5 Signal Name	DIO Use
GPIO1_6	General-purpose input/output
GPIO1_7	General-purpose input/output
GPIO1_8	General-purpose input/output
GPIO1_9	General-purpose input/output
GPIO1_25	General-purpose input/output
GPIO1_26	General-purpose input/output
GPIO2_17	General-purpose input/output

This DIO interface and the corresponding Eurotech DIO driver provide digital I/O signals in a unified driver interface. Each signal is represented as a bit in a 32-bit DIO register. The following table defines the DIO word bit-mapping.

Bit	Host Device		Function	I/O Mode
	Module	Carrier Board		
0	i.MX31		GPIO1_6	IO
1	i.MX31		GPIO1_8	IO
2	i.MX31		GPIO1_9	IO
3	i.MX31		GPIO2_17	IO
4		PCTRL	LED1	O
5		PCTRL	LED2	O
6		PCTRL	LED3	O
7		GPIO	GPO0	O
8		GPIO	GPO1	O
9		GPIO	GPI0	I
10		GPIO	GPI1	I
11		GPIO	GPI2	I
12		GPIO	GPI3	I
13		GPIO	GPI4	I
14	i.MX31		GPIO1_7	IO
15	i.MX31		GPIO1_25	IO
16	i.MX31		GPIO1_26	IO
17..31				not available

Requirements:

- SYS_ID1 System Register bit: DIO
  One designated SYS_ID1 System Register bit, DIO, identifies the presence or absence of the DIO interface. For a description of this bit, see System Identification Registers, page 59.
- PCTRL System Register bits: LED1..3
  Three designated PCTRL System Register bits, LED1..3, control three individual LED outputs, if needed. For descriptions of these bits, see Power Control Register, page 61.
- GPIO System Register bits: GPO0 and GPO1
  Two designated GPIO System Register bits, GPO0 and GPO1, control two individual digital outputs, if needed. For descriptions of these bits, see GPIO Register, page 62.
- GPIO System Register bits: GPI0..4
  Five designated GPIO System Register bits, GPI0..4, control five individual digital inputs, if needed. For descriptions of these bits, see GPIO Register, page 62.

Exceptions:

- DIO interface is mutually exclusive with the following interfaces:
  - PWM1
  - 1WI
  - TDET
  - TCAP
  - TCOMP

Other Interfaces

The hardware interfaces described in this section are part of the Turbo G5 module. However, use of any one of these interfaces defines an *Interface Set* requiring support by a custom BSP. For a complete description of the *Interface Sets*, see Hardware Interface Options, page 13. All interface signals are available on J1: Docking Connector, page 47 and J2: Docking Connector, page 52.

In addition to the following interfaces, the Expansion Bus provides powerful expansion capability for systems designed to work with a custom BSP. The type of device controllers that can be connected to this bus is virtually unlimited. Examples include other processors, FPGAs, and ASICs.

For further details about the following interfaces and custom BSP options, contact your local Eurotech representative.

ATA - ATA

Advanced Technology Attachment (ATA) provides connection to hard disk and optical disk drives.

SPI1 in Slave Mode – SPI1S

SPI1 interface can support SPI Slave mode.

SPI3 in Master Mode – SPI3M

SPI3 interface can provide a second SPI Master mode.

SPI3 in Slave Mode – SPI3S

SPI3 interface can support SPI Slave mode.

I^2S – I2S

I2S interface provides connection to a CODEC. I2S is another mode of a SSI interface.

Second SSI – SSI6

SSI6 can provide a second SSI interface.

SIM - SIM

The Turbo G5 module can support a Subscriber Identification Module interface, as described in the following table.

Turbo G5 Signal Name	SIM Use
GPIO2_0	Card Vcc enable
GPIO2_1	Transmit data
GPIO2_2	Receive data
GPIO2_3	Card detect
GPIO3_2	Clock
GPIO3_2	Reset

CSI with “non-standard sensor”

CSI can be programmed in various modes depending on the imaging sensor with which it couples. Any sensor that does not provide an 8-bit ITU.BT 656 type interface with embedded SAV/EAV and I2C control is referred to as a “non-standard sensor”.

Keypad with “non-standard key arrangement”

Any keypad that is not arranged as an 8x8 key scan matrix is referred to as having a “non-standard key arrangement”. This includes designating particular KEY_COLx and KEY_ROWx lines for individual keys, as well as implementation of scroll-wheels or sliders.

Timer Capture and Timer Compare – TCAP and TCOMP

The Turbo G5 module offers a 32-bit general-purpose timer with the following capabilities:

- The timer value can be captured in a register when the programmed compare value is reached or when an event trigger is applied to GPIO1_7.
- The timer can generate an event on GPIO1_8 when the programmed compare value is reached.

Tamper Detect

The Turbo G5 module offers Tamper Detect logic that can issue a security violation if GPIO1_6 is asserted.

Interfaces Suitability Table

The following table enumerates all interfaces presented in Standard Interfaces, page 19 and Other Interfaces, page 43. Each row represents one interface with the name of the interface in the first column and its abbreviation in the second column. The third column lists abbreviations of interfaces that cannot be used simultaneously with the interface given in the first column. All interfaces that are not Standard Interfaces are abbreviated in **bold** type face.

Interface Name	Abbr.	Exception
LCD Interface	LCD	PWM2
PWM1 Interface	PWM1	DIO, **ATA**
PWM2 Interface	PWM2	LCD
Secure Digital/MultiMediaCard Interface 1	SDMMC1	
Secure Digital/MultiMediaCard Interface 2	SDMMC2	CF
CompactFlash® Interface	CF	SDMMC2
Serial Interface 1	UART1	
Serial Interface 2	UART2	
Serial Interface 3	UART3	4WTS, 5WTS, **SPI3**
Serial Interface 4	UART4	USBO
Serial Interface 5	UART5	CF (RST/CTS only)
I^2C Interface	I2C	**ATA**
SPI1 Master	SPI1M	**SPI1S**
Camera Sensor Interface	CSI	**ATA**
AC97 Audio and Touchscreen Controller Combo	AC97	PMICA, 4WTS, 5WTS
PMIC Audio	PMICA	AC97
4-wire Touchscreen Controller	4WTS	UART3, AC97, **SPI3M, SPI3S**
5-wire Touchscreen Controller	5WTS	UART3, AC97, **SPI3M, SPI3S**
USB Host	USBH	**SSI6**
USB On-The-Go	USBO	UART4, USBC, USBH2
USB Client	USBC	UART4, USBO, USBH2
USB Second Host	USBH2	UART4, USBC, USBO
NAND Flash Interface	NANDF	
Ethernet 1	ETH1	
Ethernet 2	ETH2	
CAN 1	CAN1	**ATA**

Interface Name	Abbr.	Exception
CAN 2	CAN2	**ATA**
8x8 Keypad	KEYPAD	**ATA**
1-Wire Interface	1WI	DIO
Digital I/O Interface	DIO	PWM1, 1WI, **TD**, **TCAP**, **TCOMP**
ATA	**ATA**	PWM1, I2C, CSI, CAN1, CAN2, KEYPAD
Timer Capture	**TCAP**	DIO
Timer Compare	**TCOMP**	DIO
Tamper Detect	**TDET**	DIO
I^2S	**I2S**	AC97, PMICA
SIM	**SIM**	
SPI1 in Slave Mode	**SPI1S**	SPI1M
SPI3 in Master Mode	**SPI3M**	**SPI3S**, 4WTS, 5WTS, UART3
SPI3 in Slave Mode	**SPI3S**	**SPI3M**, 4WTS, 5WTS, UART3
Second SSI	**SSI6**	USBH

Docking Connectors

The following tables describe the electrical signals available on the connectors of the module. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions, and references to related sections.

J1: Docking Connector

Module connector: 140-pin socket, 0.5 mm, Hirose FX10A-140S/14-SV(91)

Carrier board connector: 140-pin header, 0.5 mm, Hirose FX10A-140P/14-SV(91)

The Turbo G5 module connector J1 mates to the carrier board.

Group	Name	Pin	Type	Description	
				Standard	Alternate
Input power	V3.3_IN	1	PI	Power supply input	
	V3.3_IN	2	PI		
	V3.3_IN	3	PI		
	V3.3_IN	4	PI		
Common	GND	11	P	Common reference for all signals	
	GND	21	P		
	GND	31	P		
	GND	41	P		
	GND	51	P		
	GND	61	P		
	GND	80	P		
	GND	90	P		
	GND	100	P		
	GND	110	P		
	GND	120	P		
	GND	130	P		
	GND	137	P		
	GND	138	P		
	GND	139	P		
	GND	140	P		
Reserved	nc	37		Reserved for future expansion	
	nc	67			
	nc	88			

Group	Name	Pin	Type	Description	
				Standard	Alternate
PMICA	MICL	5	AI	Audio microphone inputs	Audio line-inputs
	MICR	136	AI		
	LOUTL	135	AO	Audio line-outputs	
	LOUTR	134	AO		
Fusebox	FVDD	42	PI	Fusebox power	
Other	P_EN	86	O-1.8	Power state indicator: '1' – active state '0' – sleep state	
	CLKO	89	O-1.8	Output clock	
JTAG	SJC_MOD	6	I-2.8	i.MX31 JTAG interface	
	DE#	17	IO-2.8		
	TMS	16	I-2.8		
	TCK	33	I-2.8		
	TDI	125	I-2.8		
	TDO	132	O-2.8		
	TRST#	109	I-2.8		
	RTCK	118	O-2.8		
SSI4	SCK4	26	I-1.8	SSI clock	
	SFS4	122	O-1.8	SSI sync	
	STXD4	13	O/IO-1.8	SSI data out	GPIO1_19
	SRXD4	123	I/IO-1.8	SSI data in	GPIO1_20
I2C / ATA	I2C1_CLK	15	OD-1.8	I^2C clock	
	I2C1_DATA	119	OD-1.8	I^2C data	
USBO / USBC / USBH2 / UART4	USBOTG_NXT	128	I-1.8	USB*x* ULPI NXT	
	USBOTG_DIR	129	I-1.8	USB*x* ULPI DIR	
	USBOTG_STP	24	O-1.8	USB*x* ULPI STP	
	USBOTG_CLK	12	I-1.8	USB*x* ULPI CLK	
	USBOTG_D0	18	IO/O-1.8	USB*x* ULPI D0	UART4 RTS
	USBOTG_D1	127	IO-1.8	USB*x* ULPI D1	
	USBOTG_D2	8	IO-1.8	USB*x* ULPI D2	
	USBOTG_D3	121	IO/I-1.8	USB*x* ULPI D3	UART4 RXD
	USBOTG_D4	14	IO/O-1.8	USB*x* ULPI D4	UART4 TXD
	USBOTG_D5	126	IO/I-1.8	USB*x* ULPI D5	UART4 CTS
	USBOTG_D6	9	IO-1.8	USB*x* ULPI D6	
	USBOTG_D7	124	IO-1.8	USB*x* ULPI D7	

Group	Name	Pin	Type	Description	
				Standard	Alternate
USBH / SSI6	USBH2_NXT	104	I-1.8	USBH ULPI NXT	SCK6
	USBH2_DIR	105	I-1.8	USBH ULPI DIR	SFS6
	USBH2_STP	36	O-1.8	USBH ULPI STP	
	USBH2_CLK	32	I-1.8	USBH ULPI CLK	
	USBH2_D0	35	IO-1.8	USBH ULPI D0	
	USBH2_D1	108	IO-1.8	USBH ULPI D1	
	USBH2_D2	38	IO-1.8	USBH ULPI D2	
	USBH2_D3	102	IO-1.8	USBH ULPI D3	
	USBH2_D4	39	IO-1.8	USBH ULPI D4	
	USBH2_D5	101	IO-1.8	USBH ULPI D5	
	USBH2_D6	40	IO-1.8	USBH ULPI D6	STXD6
	USBH2_D7	99	IO-1.8	USBH ULPI D7	SRXD6
UART2	RXD2	87	I/IO-2.8	UART2 RXD	GPIO1_27
	TXD2	68	O/IO-2.8	UART2 TXD	GPIO1_28
	RTS2	112	I-2.8	UART2 CTS	
	CTS2	69	O-2.8	UART2 RTS	
UART5	PC_BVD1	20	I-1.8	UART5 RXD	
	PC_BVD2	115	O-1.8	UART5 TXD	
	PC_RST	19	O-1.8	UART5 RTS	
	PC_VS2	116	I-1.8	UART5 CTS	
Expansion Bus	EA0	60	O-1.8	Address bus Notice: EA0..EA10 are shared with the CF interface	
	EA1	81	O-1.8		
	EA2	55	O-1.8		
	EA3	83	O-1.8		
	EA4	56	O-1.8		
	EA5	76	O-1.8		
	EA6	57	O-1.8		
	EA7	73	O-1.8		
	EA8	59	O-1.8		
	EA9	79	O-1.8		
	EA10	58	O-1.8		
	EA11	78	O-1.8		
	EA12	66	O-1.8		
	EA13	74	O-1.8		
	EA14	62	O-1.8		
	EA15	77	O-1.8		

Group	Name	Pin	Type	Description	
				Standard	Alternate
Expansion Bus	EA16	63	O-1.8	Address bus Notice: EA0..EA10 are shared with the CF interface	
	EA17	72	O-1.8		
	EA18	70	O-1.8		
	EA19	75	O-1.8		
	EA20	64	O-1.8		
	EA21	71	O-1.8		
	EA22	53	O-1.8		
	EA23	84	O-1.8		
	EA24	65	O-1.8		
	EA25	91	O-1.8		
Expansion Bus	ED0	47	IO-1.8	Data bus Notice: ED0..ED15 are shared with the CF interface	
	ED1	92	IO-1.8		
	ED2	50	IO-1.8		
	ED3	95	IO-1.8		
	ED4	43	IO-1.8		
	ED5	93	IO-1.8		
	ED6	49	IO-1.8		
	ED7	94	IO-1.8		
	ED8	44	IO-1.8		
	ED9	96	IO-1.8		
	ED10	48	IO-1.8		
	ED11	97	IO-1.8		
	ED14	45	IO-1.8		
	ED12	46	IO-1.8		
	ED13	85	IO-1.8		
	ED15	98	IO-1.8		
	WAIT#	52	I-1.8	End current bus cycle (optional): ‘0’ – do not end ‘1’ - end	
SDMMC1	SD1_CLK	34	O/IO-1.8	SDMMC1 CLK	GPIO2_27
	SD1_CMD	107	IO-1.8	SDMMC1 CMD	GPIO2_26
	SD1_D0	30	IO-1.8	SDMMC1 D0	GPIO2_28
	SD1_D1	111	IO-1.8	SDMMC1 D1	GPIO2_29
	SD1_D2	28	IO-1.8	SDMMC1 D2	GPIO2_30
	SD1_D3	103	IO-1.8	SDMMC1 D3	GPIO2_31

Group	Name	Pin	Type	Description	
				Standard	Alternate
CF	PC_CE1#	54	O-1.8	CE1#	
	PC_CE2#	82	O-1.8	CE2#	
	PC_POE#	23	O-1.8	Data buffer enable	
	PC_RW#	117	O-1.8	Data buffer direction	
	IOIS16#	22	I-1.8	16-bit CF port	
CF / SDMMC2	PC_VS1	25	IO-1.8	not used for CF	SDMMC2 D2
	PC_CD1#	27	I/IO-1.8	CF CD1#	SDMMC2 CMD
	PC_CD2#	113	I/O-1.8	CF CD2#	SDMMC2 CLK
	PC_WAIT#	29	I/IO-1.8	CF WAIT#	SDMMC2 D0
	PC_PWRON	106	I/IO-1.8	CF power sense	SDMMC2 D3
	PC_READY	114	I/IO-1.8	CF READY	SDMMC2 D1
Digital In / Out / SSI6	GPIO1_7	7	IO/I-1.8	GPIO	CAPTURE
	GPIO1_8	133	IO/O-1.8	GPIO	COMPARE
	GPIO1_25	10	IO-1.8	GPIO	SCK6
	GPIO1_26	131	IO-1.8	GPIO	SFS6

J2: Docking Connector

Module connector: 140-pin socket, 0.5 mm, Hirose FX10A-140S/14-SV(91)

Carrier board connector: 140-pin header, 0.5 mm, Hirose FX10A-140P/14-SV(91)

The Turbo G5 module connector J2 mates to the carrier board.

Group	Name	Pin	Type	Description	
				Standard	Alternate
Output power	V18_IO	1	PO-1.8	Power supply output	
	V18_IO	2	PO-1.8		
	V18_IO	3	PO-1.8		
	V18_IO	4	PO-1.8		
	V28_IO	70	PO-2.8		
	V28_IO	71	PO-2.8		
Input power	RTC_BAT	6	PI	RTC backup power	
Common	GND	11	P	Common reference for all signals	
	GND	21	P		
	GND	31	P		
	GND	41	P		
	GND	51	P		
	GND	61	P		
	GND	80	P		
	GND	90	P		
	GND	100	P		
	GND	110	P		
	GND	120	P		
	GND	137	P		
	GND	138	P		
	GND	139	P		
	GND	140	P		
Other	RESET#	28	I/OD-1.8	System reset	
	UBOOT#	104	I-1.8	UART1 boot select (optional)	
	POWER_FAIL	124	I-1.8	Power fail interrupt (optional)	
	VPRES_DET	5	I	Voltage detect interrupt (optional)	

Group	Name	Pin	Type	Description	
				Standard	Alternate
CSI / ATA	CSI_MCLK	109	IO-1.8	CSI master clock	GPIO3_16
	CSI_PIXCLK	30	IO-1.8	CSI pixel clock	GPIO3_19
	CSI_HSYNC	34	IO-1.8	CSI hsync	GPIO3_18
	CSI_VSYNC	108	IO-1.8	CSI vsync	GPIO3_17
	CSI_D0	19	I/IO-1.8	CSI data0	GPIO3_26
	CSI_D1	116	I/IO-1.8	CSI data1	GPIO3_27
	CSI_D2	26	I/IO-1.8	CSI data2	GPIO3_28
	CSI_D3	111	I/IO-1.8	CSI data3	GPIO3_29
	CSI_D4	36	I/IO-1.8	CSI data4	GPIO3_4
	CSI_D5	107	I/IO-1.8	CSI data5	GPIO3_5
	CSI_D6	44	I/IO-1.8	CSI data6	GPIO3_6
	CSI_D7	106	I/IO-1.8	CSI data7	GPIO3_7
	CSI_D8	35	I/IO-1.8	CSI data8	GPIO3_8
	CSI_D9	103	I/IO-1.8	CSI data9	GPIO3_9
	CSI_D10	38	I/IO-1.8	CSI data10	GPIO3_10
	CSI_D11	105	I/IO-1.8	CSI data11	GPIO3_11
	CSI_D12	37	I/IO-1.8	CSI data12	GPIO3_12
	CSI_D13	98	I/IO-1.8	CSI data13	GPIO3_13
	CSI_D14	43	I/IO-1.8	CSI data14	GPIO3_14
	CSI_D15	99	I/IO-1.8	CSI data15	GPIO3_15
NANDF	NFCE	67	O/IO-1.8	Flash Chip Enable	GPIO1_15
	NFALE	72	O/IO-1.8	Flash Address Latch Enable	GPIO1_12
	NFCLE	69	O/IO-1.8	Flash Command Latch Enable	GPIO1_13
	NFRE#	73	O/IO-1.8	Flash Read Enable	GPIO1_11
	NFWE#	68	O/IO-1.8	Flash Write Enable	GPIO1_10
	NFRB#	66	I/IO-1.8	Flash Ready/Busy	GPIO1_16
	NFWP#	77	O/IO-1.8	Flash Write Protect	GPIO1_14

Group	Name	Pin	Type	Description	
				Standard	Alternate
LCD	FPSHIFT	42	O-1.8	LCD interface	
	HSYNC	39	O-1.8		
	VSYNC3	97	O-1.8		
	DRDY0	96	O-1.8		
	LD0	55	O-1.8		
	LD1	95	O-1.8		
	LD2	50	O-1.8		
	LD3	93	O-1.8		
	LD4	59	O-1.8		
	LD5	92	O-1.8		
	LD6	58	O-1.8		
	LD7	91	O-1.8		
	LD8	64	O-1.8		
	LD9	88	O-1.8		
	LD10	60	O-1.8		
	LD11	94	O-1.8		
	LD12	62	O-1.8		
	LD13	84	O-1.8		
	LD14	63	O-1.8		
	LD15	87	O-1.8		
	LD16	65	O-1.8		
	LD17	85	O-1.8		
	PWM2	56	O-1.8	Backlight contrast control	
Expansion Bus	BCLK	46	O-1.8	Expansion Bus control	
	CS1#	89	O-1.8		
	CS3#	74	O-1.8		
	CS4#	49	O-1.8		
	CS5#	79	O-1.8		
Expansion Bus / CF	EB0#	53	O-1.8	Expansion Bus control Required for CF REG#	
	EB1#	83	O-1.8	Expansion Bus control Required for CF IORD#	
	LBA#	81	O-1.8	Expansion Bus control Required for CF OE#	
	OE#	40	O-1.8	Expansion Bus control Required for CF IOWR#	
	RW#	45	O-1.8	Expansion Bus control Required for CF WE#	

Group	Name	Pin	Type	Description	
				Standard	Alternate
SPI1	CSPI1_SCLK	10	O/I-1.8	SPI1 Master: clock output	SPI1 Slave: clock input
	CSPI1_SS0	76	O/I-1.8	SPI1 Master: select0 output	SPI1 Slave: select0 input
	CSPI1_SS1	78	O/I-1.8	SPI1 Master: select1 output	SPI1 Slave: select1 input
	CSPI1_SS2	18	O/I-1.8	SPI1 Master: select2 output	SPI1 Slave: select2 input
	CSPI1_MISO	75	I/O-1.8	SPI1 Master: receive input	SPI1 Slave: transmit output
	CSPI1_MOSI	52	O/I-1.8	SPI1 Master: transmit output	SPI1 Slave: receive input
	CSPI1_RDY	47	I-1.8	SPI1 Master: ready (optional)	
UART3 / SPI3	CSPI3_SCLK	54	I/IO-1.8	UART3 CTS	SPI3 Master: clock output SPI3 Slave: clock input
	CSPI3_SS1	136	IO-1.8	Not used	SPI3 Master: select1 output SPI3 slave: select1 input
	CSPI3_MISO	82	O/IO-1.8	UART3 TXD	SPI3 Master: receive input SPI3 Slave: slave output
	CSPI3_MOSI	27	I/IO-1.8	UART3 RXD	SPI3 Master: transmit output SPI3 Slave: receive input
	CSPI3_RDY	86	O/I-1.8	UART3 RTS	SPI3 Master: ready (optional)
UART1	RXD1	132	I/IO-2.8	UART1 RXD	GPIO2_4
	TXD1	22	O/IO-2.8	UART1 TXD	GPIO2_5
	RTS1	133	I/IO-2.8	UART1 CTS	GPIO2_6
	CTS1	12	O/IO-2.8	UART1 RTS	GPIO2_7
	DSR1	134	I/IO-2.8	UART1 DSR	GPIO2_13
	DTR1	135	O/IO-2.8	UART1 DTR	GPIO2_12
	DCD1	121	I/IO-2.8	UART1 DCD	GPIO2_15
	RI1	48	I/IO-2.8	UART1 RI	GPIO2_14

Group	Name	Pin	Type	Description	
				Standard	Alternate
Keypad	KEY_COL0	13	O-2.8	Column driver	
	KEY_COL1	127	O-2.8		
	KEY_COL2	23	O-2.8		
	KEY_COL3	123	O-2.8		
	KEY_COL4	29	O/IO-2.8	Column driver	GPIO2_22
	KEY_COL5	129	O/IO-2.8	Column driver	GPIO2_23
	KEY_COL6	15	O/IO-2.8	Column driver	GPIO2_24
	KEY_COL7	128	O/IO-2.8	Column driver	GPIO2_25
	KEY_ROW0	7	I-2.8	Row sense	
	KEY_ROW1	130	I-2.8		
	KEY_ROW2	8	I-2.8		
	KEY_ROW3	131	I-2.8		
	KEY_ROW4	33	I/IO-2.8	Row sense	GPIO2_18
	KEY_ROW5	119	I/IO-2.8	Row sense	GPIO2_19
	KEY_ROW6	9	I/IO-2.8	Row sense	GPIO2_20
	KEY_ROW7	126	I/IO-2.8	Row sense	GPIO2_21
In / Out	GPIO1_0	20	IO-1.8	GPIO	
	GPIO1_1	112	IO/I-1.8	GPIO	Touchscreen interrupt
	GPIO1_2	17	IO/I-1.8	GPIO	AC97 interrupt
	GPIO1_3	113	IO/I-1.8	GPIO	Ethernet1 interrupt
	GPIO1_4	24	IO/I-1.8	GPIO	Ethernet2 interrupt
	GPIO1_6	114	IO/I-1.8	GPIO	Tamper detect
	GPIO1_9	118	IO/O-1.8	GPIO	PWM1 output
	GPIO2_0	25	IO-2.8	GPIO	
	GPIO2_1	115	IO-2.8	GPIO	
	GPIO2_2	14	IO-2.8	GPIO	
	GPIO2_3	125	IO-2.8	GPIO	
	GPIO2_17	117	IO-1.8	GPIO	1-wire interface
	GPIO3_0	32	IO/I-1.8	GPIO	SD1 CD#
	GPIO3_1	101	IO/I-1.8	GPIO	SD2 CD#
	GPIO3_2	16	IO-2.8	GPIO	
	GPIO3_3	122	IO-2.8	GPIO	
	GPIO3_30	57	IO/I-1.8	GPIO	CAN1 interrupt
	GPIO3_31	102	IO/I-1.8	GPIO	CAN2 interrupt

Standard Carrier Board Requirements

The design of the Turbo G5 module enables integration with a wide range of application-specific carrier boards supporting many possible combinations of hardware interfaces. For further details about these combinations, see Hardware Interface Options, page 17.

Standard Carrier Board

A *Turbo G5 Standard Carrier Board* is one that is supported by the Standard BSP. The Turbo G5 development system carrier board is one example of a *Turbo G5 Standard Carrier Board*.

To qualify as a *Turbo G5 Standard Carrier Board*, a carrier board must meet the following requirements:

- The carrier board must include only hardware interfaces compatible with one of the Interface Sets supported by the Standard BSP.
  For a complete description of these interfaces, see Standard Interfaces, page 19.
- The carrier board must support functionality for hardware identification and control. This support circuitry must include a minimum of two and as many as five memory-mapped System Registers: SYS_ID0, SYS_ID1, PCTRL, CTRL, and GPIO. Implementation of the former two System Registers is mandatory. Implementation of the latter three System Registers is needed only if any of their bits are required by the *Interface Set*. In this case, the implementation of only the required bits is mandatory, not the entire register functionality.

Typically, the five required registers are implemented by a CPLD on the carrier board. The following sections provide details about each of these registers.

System Registers and Memory Map

These features must be provided on the carrier board by memory-mapped registers accessible using the Expansion Bus.

Expansion Bus Memory Map

The following table defines the Expansion Bus memory map.

Register Identification	Register Name	Address
SYS_ID0 (note 1, 2)	System Identification 0	0xB4000000
SYS_ID1 (note 1, 2)	System Identification 1	0xB4000004
PCTRL (note 1, 2)	Power Control	0xB4000008
CTRL (note 1, 2)	Control	0xB400000C
GPIO (note 1, 2)	General-purpose inputs and general-purpose outputs	0xB4000010
ETH1 (note 3)	Ethernet 1	0xB6000000..0xB60000FE
ETH1 (note 3)	Ethernet 1 FIFO Access	0xB6000100..0xB6000106
ETH2 (note 3)	Ethernet 2	0xB6800000..0xB68000FE
ETH2 (note 3)	Ethernet 2 FIFO Access	0xB6800100..0xB6800106
CAN1_ADDR (note 1, 4)	CAN #1 Address Latch	0xB7000000
CAN1_DATA (note 1, 4)	CAN #1 Data	0xB7000004
CAN2_ADDR (note 1, 4)	CAN #2 Address Latch	0xB7800000
CAN2_DATA (note 1, 4)	CAN #2 Data	0xB7800004

Notes:

1. All accesses must be at a 32-bit address boundary.
2. Represents a register on the carrier board typically implemented by a CPLD.
3. Represents internal registers of an Ethernet controller on the carrier board. Address decoding typically is implemented by a CPLD on the carrier board. All accesses must be at a 16-bit address boundary.
4. Represents internal registers of a CAN controller on the carrier board. Address decoding typically is implemented by a CPLD on the carrier board.

System Identification Register 0 – SYS_ID0

Information about which *Interface Set* a particular *Turbo G5 Standard Carrier Board* supports is conveyed by two System Registers: SYS_ID0 and SYS_ID1.

SYS_ID0 is accessible as a 16-bit read access from physical address 0xB4000000. Each register bit marks the presence or absence of a particular pre-defined interface. A logic-level high indicates the hardware interface is included on the carrier board, while a logic-level low indicates the carrier board does not include the interface.

The following table defines the SYS_ID0 System Register on the carrier board.

SYS_ID0 (0xB4000000)			
Bit	Bit Name: Identify presence of	Mode	Default State
0	UART1	R	Depends on HW configuration
1	UART2	R	Depends on HW configuration
2	UART3	R	Depends on HW configuration
3	UART4	R	Depends on HW configuration
4	UART5	R	Depends on HW configuration
5	SDMMC1	R	Depends on HW configuration
6	SDMMC2	R	Depends on HW configuration
7	CF	R	Depends on HW configuration
8	LCD	R	Depends on HW configuration
9	AC97	R	Depends on HW configuration
10	4WTSC	R	Depends on HW configuration
11	5WTSC	R	Depends on HW configuration
12	PWM1	R	Depends on HW configuration
13	PWM2	R	Depends on HW configuration
14	USBH	R	Depends on HW configuration
15	USBO	R	Depends on HW configuration

System Identification Register 1 – SYS_ID1

Information about which *Interface Set* a particular *Turbo G5 Standard Carrier Board* supports is conveyed by two System Registers: SYS_ID0 and SYS_ID1.

SYS_ID1 is accessible as a 16-bit read access from physical address 0xB4000004. Each register bit marks the presence or absence of a particular pre-defined interface. A logic-level high indicates the hardware interface is included on the carrier board, while a logic-level low indicates the carrier board does not include the interface.

The following table defines the SYS_ID1 System Register on the carrier board.

SYS_ID1 (0xB4000004)			
Bit	Bit Name: Identify presence of	Mode	Default State
0	SPI1	R	Depends on HW configuration
1	I2C	R	Depends on HW configuration
2	CSI	R	Depends on HW configuration
3	1WI	R	Depends on HW configuration
4	NANDF	R	Depends on HW configuration
5	8X8KP	R	Depends on HW configuration
6	ETH1	R	Depends on HW configuration
7	ETH2	R	Depends on HW configuration
8	CAN1	R	Depends on HW configuration
9	CAN2	R	Depends on HW configuration
10	DIO	R	Depends on HW configuration
11	PMICA	R	Depends on HW configuration
12	reserved	R	0
13	reserved	R	0
14	reserved	R	0
15	reserved	R	0

Power Control Register – PCTRL

The power control (PCTRL) System Register provides discrete control signals to select hardware interfaces on a *Turbo G5 Standard Carrier Board*. It is accessible as a 16-bit read access from physical address 0xB4000008. Each register bit enables or disables power to the interface. A logic-level high turns power on, while a logic-level low turns off power.

The following table defines the PCTRL System Register on the carrier board.

PCTRL (0xB4000008)				
Bit	Bit Name	Bit Function: Enable or On = 1	Mode	Default State
0	COM1_EN	UART1 external power control	RW	0
1	COM2_EN	UART2 external power control	RW	0
2	COM3_EN	UART3 external power control	RW	0
3	COM4_EN	UART4 external power control	RW	0
4	COM5_EN	UART5 external power control	RW	0
5	USBH_EN	USBH ULPI transceiver enable	RW	0
6	USBO_EN	USBO ULPI transceiver enable	RW	0
7	CAN_ON	CAN1 and CAN2 power control	RW	0
8	LCD_ON	LCD interface power control	RW	0
9	LCDBL_ON	LCD backlight power control	RW	0
10	AUD_ON	Audio power amplifier power control	RW	0
11	CF_ON	CF power control	RW	0
12	LED1	User LED1 power control	RW	0
13	LED2	User LED2 power control	RW	0
14	LED3	User LED3 power control	RW	0
15	reserved		R	0

Control Register – CTRL

The control (CTRL) System Register provides discrete reset signals to select hardware interfaces on a *Turbo G5 Standard Carrier Board* and information about firmware and board revisions. It is accessible as a 16-bit read access from physical address 0xB400000C. A logic-level high on each register bit resets the specified interface.

The following table defines the CTRL System Register on the carrier board.

CTRL (0xB400000C)				
Bit	Bit Name	Bit Function: Reset= 1	Mode	Default State
0	USBH_RST	USB Host ULPI reset	RW	0
1	USBO_RST	USB OTG ULPI reset	RW	0
2	CAN1_RST	CAN1 reset control	RW	0
3	CAN2_RST	CAN2 reset control	RW	0
4	AC97_RST	AC97 codec reset control	RW	0
5	ETH1_RST	Ethernet1 reset control	RW	0
6	ETH2_RST	Ethernet2 reset control	RW	0
7	CF_RST	CompactFlash reset	RW	0
8..11	FRM_REV[0..3]	Firmware revision	R	Firmware revision
12..15	BRD_REV[0..3]	Board revision	R	Board revision

GPIO Register – GPIO

The GPIO System Register provides general-purpose inputs (GPI) and general-purpose outputs (GPO) on the carrier board.

The following table defines the GPIO System Register on the carrier board.

GPIO (0xB4000010)				
Bit	Bit Name	Bit Function	Mode	Default State
0..7	GPO[0..7]	General-purpose outputs	RW	00000000
8	GPI0	General-purpose input	R	Current state of input
9	GPI1	General-purpose input	R	Current state of input
10	GPI2	General-purpose input	R	Current state of input
11	GPI3	General-purpose input	R	Current state of input
12	GPI4	General-purpose input	R	Current state of input
13	GPI5	General-purpose input or SD1_WP#	R	Current state of input
14	GPI6	General-purpose input or SD2_WP#	R	Current state of input
15	GPI7	General-purpose input	R	Current state of input

System Specification

Power Specification

This section includes power specifications for the Turbo G5 module.

Power Supply

Note: When power is turned on, V3.3_IN must meet the following two requirements:

- V3.3_IN must reach $V_{V3.3\_IN}$ min monotonically.
- V3.3_IN must reach $V_{V3.3\_IN}$ min in less than 50 ms.

Absolute Maximum Ratings

Input supply voltages 4.65 V

DC Electrical Characteristics

Symbol	Parameter	Min	Typ.	Max	Units
Module Power Input					
$V_{V3.3\_IN}$	Supply voltage	3.0	3.3	3.6	V
$P_{V3.3\_IN\ SLEEP}$	Sleep power consumption		30		mW
Fusebox					
V_{FVDD}	Read supply voltage		float or 0		V
	Write supply voltage	3.0		3.3	V
$I_{FVDD\ PROG}$	Current to program one Fusebox bit		35	60	mA
Module Power Outputs					
$V_{V1.8\_IO}$	1.8 V domain output voltage	1.7	1.8	1.9	V
$I_{V1.8\_IO}$	1.8 V domain output current			300	mA
$V_{V2.8\_IO}$	2.8 V domain output voltage	2.6	2.8	2.9	V
$I_{V2.8\_IO}$	2.8 V domain output current			100	mA
VPRES_DET Interrupt(optional)					
V_{IN}	Input voltage range	0		20	V
V_{TH}	Threshold, low to high			3.9	V
	Threshold, high to low	3.5			V
RTC					
V_{RTC_BAT}	RTC supply voltage	1.5		3.5	V
I_{RTC_BAT}	RTC current consumption, V33_IN = 0V		6	7	uA

Electrical Specification

The following specifications are taken from the i.MX31 and i.MX31L Multimedia Applications Processors Data Sheet, rev. 4.1, 11/2008 and are provided for reference.

Symbol	Parameter		Min	Typ.	Max	Units
GPIO						
V_{OH}	High-level output voltage		$0.8*V_{DOMAIN}$			V
V_{OL}	Low-level output voltage				$0.2*V_{DOMAIN}$	V
I_{OH_S}	High-level output current, slow slew rate	Std drive	-2			mA
		High drive	-4			mA
		Max drive	-8			mA
I_{OH_F}	High-level output current, fast slew rate	Std drive	-4			mA
		High drive	-6			mA
		Max drive	-8			mA
I_{OL_S}	Low-level output current, slow slew rate	Std drive	2			mA
		High drive	4			mA
		Max drive	8			mA
I_{OL_F}	Low-level output current, fast slew rate	Std drive	4			mA
		High drive	6			mA
		Max drive	8			mA
V_{IH}	High-level input voltage		$0.7*V_{DOMAIN}$		V_{DOMAIN}	V
V_{IL}	Low-level input voltage		0		$0.3*V_{CORE}$	V
DDR IO						
V_{OH}	High-level output voltage		$0.8*V_{DOMAIN}$			V
V_{OL}	Low-level output voltage				$0.2*V_{DOMAIN}$	V
I_{OH}	High-level output current	Std drive	-3.6			mA
		High drive	-7.2			mA
		Max drive	-10.8			mA
I_{OL}	Low-level output current	Std drive	3.6			mA
		High drive	7.2			mA
		Max drive	10.8			mA
V_{IH}	High-level input voltage		$0.7*V_{DOMAIN}$	V_{DOMAIN}	V_{DOMAIN} + 0.3	V
V_{IL}	Low-level input voltage		-0.3	0	$0.3*V_{DOMAIN}$	V

General Specification

This section provides general specifications for the Turbo G5 module.

Crystal Frequencies

Agencies certifying Turbo G5 for compliance for radio-frequency emissions typically need to know the frequencies of on-system oscillators. The following table lists the frequencies of all crystals on the Turbo G5 module.

Crystals	Device	Typ.	Units
OS1	iMX31 processor	26	MHz
X1	PMIC	32.768	kHz

Real-Time Clock

The Turbo G5 module includes a real-time clock (RTC) function. For a description of this function, see Real-Time Clock, page 8.

Symbol	Parameter	Min	Typ.	Max	Units
V_{RTC_BAT}	RTC supply voltage	1.5		3.5	V
I_{RTC_BAT}	RTC current consumption, V33_IN = 0V		6	7	uA

Environmental Specification

The Turbo G5 module is available in a commercial operating temperature.

Parameter	Min	Typ.	Max	Units
Commercial operating temperature (note 5)	0		+70	°C

Notes:

5. Contact your local Eurotech representative for extended temperature options.

Appendix A – Reference Information

Product Information

Product notices, updated drivers, support material:

www.eurotech.com

Freescale

Information about the iMX31 processor and PMIC:

www.freescale.com

USB

Universal Serial Bus specification and product information:

www.usb.org

SDIO Card

SD Card Association and SDIO specification:

www.sdcard.org

MMC Card

JEDEC MMC 4.0 specification:

www.jedec.org

Appendix B – RoHS Compliance

EUROTECH

The Restriction of the use of certain Hazardous Substances (RoHS) Directive came into force on 1st July 2006. This product shall be designed using RoHS compliant components, and manufactured to comply with the RoHS Directive.

Eurotech has based its material content knowledge on a combination of information provided by third parties and auditing our suppliers and sub-contractor's operational activities and arrangements. This information is archived within the associated Technical Construction File. Eurotech has taken reasonable steps to provide representative and accurate information, though may not have conducted destructive testing or chemical analysis on incoming components and materials.

Additionally, packaging used by Eurotech for its products complies with the EU Directive 2004/12/EC in that the total concentration of the heavy metals cadmium, hexavalent chromium, lead and mercury do not exceed 100ppm.

Appendix C – Board Revision

This guide applies to the current revision of the module as given in the following section.

Identifying the Board Revision

The revision number of the Turbo G5 module is located on the bottom side of the printed wiring board. That number is 170122-800Rx, where "x" is the board revision.

Turbo G5 Module Revision History

The following is an overview of the revisions to the Turbo G5 module.

Revision 2

Prototype

Revision 3

Initial release

Revision A

Production release

Appendix D – Development System

Turbo G5 development systems are designed to get the developer up and running quickly. This configuration allows you to become familiar with the Turbo G5 functionality prior to customization for your specific application.

The development system includes the Turbo G5 module, the Eurotech carrier board, and supporting peripheral devices. To provide flexibility and allow development across a broad spectrum of end-use applications, the Eurotech carrier board maximizes the Turbo G5 functionality and implements many industry-standard interfaces.

For a complete description of the Turbo G5 development system, refer to the Turbo G5 Development System User Manual.

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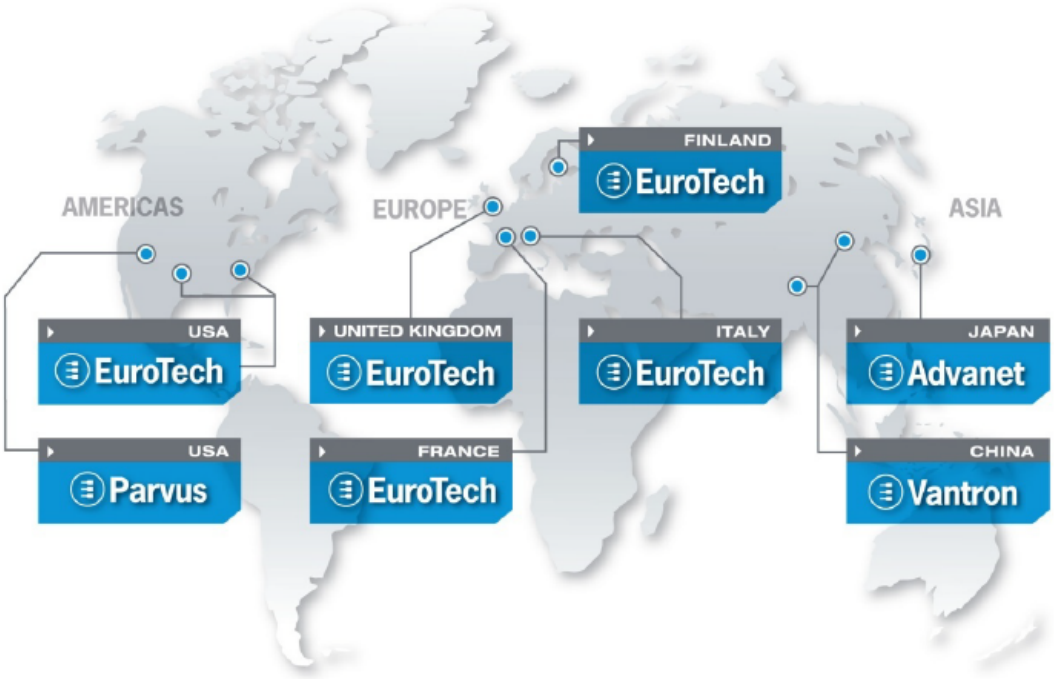

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