



Catalyst XL

High-Performance Module

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Revision History

<i>Issue no.</i>	<i>PWB</i>	<i>Date</i>	<i>Comments</i>
A		Dec-2010	Based on Catalyst Module Design-In Guide (Eurotech document # 110122-2003) Thermal Design section added
B		Aug 2011	Design Checklist and Related Documents sections added References to Programmer Reference documents added THERM_ALERT, RESET#, and FP_RESET# signals clarified Details about display cable requirements, GPIO, power requirements, and carrier board design added

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For contact details, see page [67](#).

Contents

Introduction.....	5
Handling Your Board Safely	6
Conventions.....	6
Features	8
Design Checklist.....	10
Development Kit	14
Related Documents	14
Software Specification.....	15
Operating System Support.....	15
BIOS.....	15
Software Development Kit.....	15
Everyware™ Software Framework	15
Hardware Specification	16
Block Diagram	16
Core Processor.....	16
Intel Atom Processor	17
Intel System Controller Hub US15W	17
Trusted Platform Management (optional)	18
Embedded Controller	18
Memory.....	18
Synchronous DRAM.....	18
Non-Volatile Memory.....	19
External Memory Interfaces	19
Communications	20
PCI Express.....	21
USB	21
Secure Digital and MultiMediaCard	22
I ² C Bus.....	22
System Management Bus	23
Display and User Interface.....	24
LVDS Display and Backlight Control.....	24
Serial Digital Video Out	25
Inputs and Outputs.....	26
Low Pin Count Bus.....	26
Reset Signals.....	26
System Management	27
General-Purpose Input and Output	27
Intel High Definition Audio	28
Power Requirements	28
Low Power States	28
Power Supply Architecture	29
Power State Signals	32

Mechanical Specifications	38
Mechanical Design	38
Insertion and Removal	38
Mounting Holes	38
Mechanical Drawing	39
Total Stack Height	40
Thermal Management	41
Carrier Board Design	43
Design Guidelines	43
Design Constraints	43
EMI/RFI Protection	44
Routing Guidelines	44
Power Planes	45
Requirements and Recommendations	46
Test and Debug	47
Connectors	48
Identifying Connectors	48
Signal Headers	49
J1: Docking Connector: Data	49
J2: Docking Connector: Power	56
J3: ITP Debug Port	57
System Specifications	58
Performance	58
Power	58
Power Consumption	58
Power Supply	59
Electrical	60
Reset Circuitry	60
Intel High Definition Audio	60
Embedded Controller	61
Clock Generator	62
General	62
Crystal Frequencies	62
Real-Time Clock	62
Environmental	63
Appendix A – Reference Information	64
Appendix B – RoHS Compliance	65
Appendix C – Board Revision	66
Eurotech Worldwide Presence	67

Introduction

The Catalyst XL is a high-performance, low-power module based on the Intel® Atom™ processor Z5xxP/PT. It uses an integrated two-chip solution comprised of the Intel Atom processor and Intel® System Controller Hub US15WP/PT (Intel® SCH US15W). The Intel Atom processor utilizes the low-power Intel micro architecture, while the Intel SCH US15W contains an integrated 2D/3D graphics controller supporting hardware-accelerated graphics display and video processing capabilities. The Catalyst XL allows embedded users to gain higher performance with greater energy efficiency.

An application-specific carrier board integrates with the Catalyst XL for a total production solution. This flexible, modular architecture enables easy customization and quick time-to-market. A Eurotech carrier board is available that implements several industry-standard interfaces allowing development across a broad spectrum of end-use applications. This design provides a reference for unique carrier boards optimized for high-performance, low-power applications such as ruggedized handheld, multimedia, medical, point of service, and industrial designs.

The Catalyst XL supports the following interfaces:

- LVDS display
- Serial Digital Video Output
- Backlight with control signals for intensity and on/off
- Integrated system BIOS with external BIOS support
- IDE/PATA interface
- Two PCIe x 1 lane
- Eight USB 2.0 ports
- Three SD/MMC interfaces
- SMBus
- I²C bus with I²C master device
- LPC bus
- Two general-purpose inputs and outputs
- Intel® High Definition Audio

This guide provides details about the various features of the Catalyst XL and about how they create a system that meets your application needs. It extends the information provided in the *Catalyst XL Development Kit User Manual (Eurotech document #110122-3001)* and is intended for hardware design engineers. Design details are provided as guidelines for custom carrier board design.

The information in this guide applies to the latest revision of the Catalyst XL, as listed in [Appendix C – Board Revision](#), page 66.

Handling Your Board Safely

Anti-Static Handling

The Catalyst XL contains CMOS devices that could be damaged by electrostatic discharge (ESD). Observe industry-standard electronic handling procedures when handling the module. Where possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the module or touching any components on the module.

Packaging

Please ensure that, should a module need to be returned to Eurotech, it is adequately packed, preferably in the original packing material.

Electromagnetic Compatibility



The Catalyst XL is classified as a component with regard to the European Community Electromagnetic Compatibility (EMC) regulations. Because Eurotech supplies only the single-board computer and not fully integrated systems, Eurotech cannot provide meaningful system-level emissions test results. It is the responsibility of the user to ensure that systems using the module are compliant with the appropriate EMC standards.

RoHS Compliance

The European RoHS Directive (Restriction on the use of certain Hazardous Substances – Directive 2002/95/EC) limits the amount of six specific substances within the composition of the product. The Catalyst XL fully complies with the RoHS directive. A full *RoHS Compliance Materials Declaration Form* for the Catalyst XL is included as [Appendix B – RoHS Compliance](#), page 65. Further information regarding RoHS compliance is available on the Eurotech web site at www.eurotech.com.

Conventions

The following table lists the symbols that are used in this guide.

Symbol	Explanation
	Note – information that requires your attention
	Warning – proceeding with a course of action may damage your equipment or result in loss of data

The following table describes the conventions that specify signal names.

Convention	Explanation
GND	Digital ground plane
#	Active low signal
+	Positive signal in differential pair
-	Negative signal in differential pair

The following table describes the abbreviations that specify direction and electrical characteristics of a signal.

Type	Explanation
I	Signal is an input to the system
O	Signal is an output from the system
IO	Signal may be input or output
P	Power and ground
A	Analog signal
OD	Open-drain
CMOS	3.3 V CMOS
LVC MOS	1.05 V CMOS
LVTTL	Low Voltage TTL
3.3	3.3 V signal level
5	5 V signal level
IDE	5 V tolerant signal
HDA	3.3 V (default) or 1.5 V signal
HCSL	Host Clock Signal Level
LVDS	Low Voltage Differential Signaling
PCIe	PCI Express signal
PWM	Pulse Width Modulation
nc	No connection
reserved	Use is reserved to Eurotech

Some signals include termination on the Catalyst XL. The following table describes the abbreviations that specify the signal termination.

Termination	Explanation
PU	Pull-up resistor to the specified voltage
PD	Pull-down resistor
R	Series resistor
C	Series capacitor

Features

Processor

- Intel® Atom™ processor Z5xxP/PT
- Clock rates from 1.1 GHz to 1.6 GHz
- Intel® System Controller Hub US15WP/PT
- Front side bus from 400 MHz to 533 MHz

Integrated System Functions

- Embedded Controller
- Trusted Platform Management (optional)

Memory

- 512 MB, 1 GB, or 2 GB DDR-2 DRAM
- Integrated system BIOS with external BIOS support
- Battery-backed real-time clock
- External memory support
 - IDE/PATA disk drive
 - USB disk drive
 - SD/MMC card
 - PCI Express card

Communications

- Two PCI Express one lane slots
- Eight USB 2.0 ports
 - Up to six host ports operating at low, full, and high speeds
 - Two host ports operating at high speed only
 - One client port operating at high speed
- Three Secure Digital and MultiMediaCard interfaces
- I²C bus with I²C master device
- System Management Bus

User Interface and Display

- Two independent display outputs
 - LVDS with resolutions up to 1366 x 768 at 85 Hz, 8-bit color per lane
 - Serial Digital Video Output with resolutions up to 1280 x 1024 at 85 Hz, full color
- Backlight interface with control signals for intensity and power

Inputs and Outputs

- Low Pin Count bus for general-purpose I/O expansion
- Two general-purpose inputs and outputs

Audio Interface

- Intel® High Definition Audio supporting up to two external audio codecs

Power Supply

- 3.3 V and 5 V main power inputs
- Low power consumption
- ACPI power management

Mechanical

- 67 mm x 100 mm dimensions
- Less than 10 mm total stack height

Environmental

- Extended operating temperature
- No external cooling required
- RoHS compliant

Design Checklist

Eurotech provides a host of services to ensure that your product is up and running from the first prototype release. We recommend the following process for every Catalyst XL carrier board design:

Kickoff Stage

During the Kickoff Stage, you will develop your block diagram and identify any customizations your application may require.

Gather your reference materials

Eurotech provides several documents that include key information for designing a custom carrier board. Use the following resources and ask questions:

- Catalyst XL Design-In Guide
- Catalyst XL Development Kit User Manual
- Carrier Board Routing Guidelines
- 3D CAD models
- Reference Carrier Board Schematic
- Reference Carrier Board Bill of Materials

Define your requirements

Define your system's requirement. Be sure to include requirements such as the product features, the input power, the type of transient protection on the power supply, connectivity to the module, and all I/O to your system.

Create a block diagram

Create a block diagram of your proposed design. This step helps to formulate the best way to connect different devices to the module.

Identify customizations

Identify any customizations that your application requires. Examples of customizations are custom LCD panel timings and backlight control, custom module configurations, or supporting a device that is not included on Eurotech's standard carrier board. Customizations may require updates to the BIOS.

Utilize the Catalyst XL Development Kit

Utilize the Catalyst XL Development Kit for validating your proposed design. For example, if a USB device is to be used on USB port 6, test that device by connecting it to USB port 6 on the Catalyst XL Development Kit. This testing also allows you to validate your OS image with all required drivers loaded.

Kickoff review

Early in the development of your carrier board, meet with your Eurotech representative to review your block diagram and discuss customizations. Incorporate any changes into your design.

Preliminary Design Stage

During the Preliminary Design Stage, you will finalize your block diagram, agree on customizations, and begin your preliminary schematic.

 Use the reference schematic

Use Eurotech's reference carrier board schematic as a starting point for your design. This schematic includes many commonly used interfaces. Using the same connectivity to the module will minimize the time spent in debugging your design.

 Select components from the reference bill of materials

Select the same components as those used in Eurotech's reference carrier board bill of materials. Eurotech selects components that are optimized for embedded systems based on quality, low-power consumption, availability, reliability, and industrial temperature options. Selecting the same components also allows you to use the drivers Eurotech has already integrated with the OS builds.

 Follow the design requirements and recommendations

Follow the design requirements and recommendations listed in [Carrier Board Design](#), page 43 of this design-in guide. This section provides details about circuitry to include on the carrier board.

 Preliminary design review

Stay in contact with your Eurotech representative during your preliminary design. Together, finalize your block diagram and agree on customizations needed. Continue to ask questions as you move towards finalizing your design.

Critical Design Stage

During the Critical Design Stage, you will finalize your schematic making sure that you have met all the module's electrical, thermal, and mechanical design requirements.

 Implement power supply sequencing

Implement the exact power supply sequencing described in [Power Requirements](#), page 28 of this design-in guide. The module has very specific power-on sequence requirements in order to power-up and operate correctly. Power sequencing the multiple voltage rails, as described in this section, is CRITICAL. If your design does not meet these requirements, the module will not boot.

- Provide a system-level reset*

Buffer and use the system reset signal RESET# (J1 B56), described in [Inputs and Outputs](#), page 26, to reset all devices on the carrier board. The embedded controller controls the de-assertion of this signal with appropriate timings relative to power being stable. Timing requirements for power stable to reset de-asserted and reset de-asserted to device available are critical.
- Create a power budget*

Create a power budget that takes into account the current requirement of the module, as specified in [Power](#), page 58, and of the devices that are used with the module. Design your power supply to handle the maximum current requirement.
- Determine thermal management*

Determine what type of thermal management is required for your design. Use your power budget and the information provided in [Thermal Management](#), page 41 of this design-in guide to design a heat spreader, if necessary.
- Follow the module's mechanical requirements*

Follow the exact mechanical requirements given in [Mechanical Design](#), page 38 for mounting holes placement, position of the board-to-board connectors, and stack height on your carrier board design.
- Use advanced layout and high-speed routing techniques*

Follow the design constraints and routing guidelines described in [Carrier Board Design](#), page 43 of this design-in guide. Adhering to good design practices for high-speed PCB design is essential. You should have your schematic 95% complete, especially the high-speed signals and buses of the module, power sequencing, and system reset, before you start board layout. Meet with your Eurotech representative to review your schematic before you begin layout. After your layout is complete, meet again to review your complete design.
- Have a strategy to debug your design*

Review your strategy to bring-up and to debug your design. Ensure that you have included the necessary support in your design. The maintenance serial port is extremely important in bring-up of a new design. Eurotech highly recommends including an external connection to SMC_UART_RX (J1 B57) and SMC_UART_TX (J1 B106) on your carrier board.
- Critical design review*

Do an in-depth review of your finished design, including final schematic and board layout, to ensure that you have met all the requirements described in this checklist and throughout this design-in guide. Again, ask your Eurotech representative questions.

Prototype Bring-up Stage

Eurotech provides assistance in bringing-up your prototype at your site or ours. We have several tools that can assist the process including "stand-alone" BIOS releases, BIOS modifications to meet specific platform or test requirements, and power monitoring applications for the module. The "stand-alone" BIOS sets up the internal functions of the module and basic I/O functions. It is not dependent on any specific carrier board, devices, or circuits. This BIOS provides "basic" level functionality and can be used as a tool in the bring-up or debug of your unique carrier board.

- Begin with the basics*

Begin by checking basic functionality such as power, reset, and clocks. Verify that the power sequencing is as it should be and that the voltage regulator outputs are at nominal levels. Check that the system reset signal is asserted and deasserted according to the power sequencing requirements. Ensure all clocks necessary for bring-up are running properly.

- Start with minimal devices*

Minimize the number of devices required for bring-up. Using Eurotech's "debug" set of firmware is a good start. This firmware can be used (on case-by-case) basis as a debug and bring-up tool for your specific design prototyping or in the debugging phases of your development. It disables all NON-Critical-to-BOOT functions to simplify the system functionality to base level. After you have verified this base level, enable each subsystem as needed. Adding one device at a time will help determine which subsystem, if any, is having problems.

- Utilize the maintenance port*

Utilize the maintenance port output to identify problems during bring-up. This port provides important debug information including BIOS POST codes and error messages that enable you to monitor the operation of the module.

- Use your Catalyst XL Development Kit*

Use your Catalyst XL Development Kit to isolate problems. If a problem occurs during bring-up of your carrier board, try to duplicate the problem on the development kit.

- Prototype bring-up review*

Review your bring-up process and share lessons learned with your Eurotech representative.

Acceptance of Customizations

Eurotech is committed to your design success. Using our support services throughout the development cycle ensures a complete and robust solution with which to move forward.

- Customization Acceptance*

Meet with your Eurotech representative to discuss acceptance of any customizations and to plan the steps toward production of your Catalyst XL design.

Development Kit

The Catalyst XL Development Kit is designed to get the developer up and running quickly. The development kit includes the Catalyst XL, a standard development kit carrier board, and supporting peripheral devices. To provide flexibility and allow development across a broad spectrum of end-use applications, the carrier board maximizes the Catalyst XL functionality and implements many industry-standard interfaces. This configuration allows you to become familiar with the Catalyst XL functionality prior to customization for your specific application. In addition, the standard development kit carrier board provides a reference for custom carrier board design.

For a complete description of the Catalyst XL Development Kit, refer to the *Catalyst XL Development Kit User Manual* (Eurotech document 110122-3001).

Related Documents

This guide provides details about the various features of the Catalyst XL and about how it creates a system that meets your application needs. It extends the information provided in the *Catalyst XL Development Kit User Manual* and is intended for hardware design engineers. Design details are provided as guidelines for custom carrier board design.

The following documents are also important resources for the Catalyst XL.

Document	
Catalyst XL Development Kit User Manual	110122-3001
Catalyst Development Kit Carrier Reference Schematic	110122-3002
Catalyst Development Kit Carrier Reference BOM	110122-3003
Catalyst XL CE Pro WES Development Kit Quick Start	110122-3004
Catalyst XL LiveUSB Development Kit Quick Start	110122-3006
Catalyst XL Carrier Board Routing Guidelines	110122-2004
Catalyst Module Installation and Removal	110122-2014
Catalyst System Management Programmer Reference	110122-2021
Catalyst SMBus Programmer Reference	110122-2022
Catalyst I ² C Bus Programmer Reference	110122-2023
Catalyst Module Display Adapter User Manual	110122-4000

Check the Eurotech support site (<http://support.eurotech-inc.com/>) for errata reports and for the latest releases of these documents.

Software Specification

Eurotech provides an application-ready platform including BIOS, operating system, and development environment. This section gives a brief description of the software support available for the Catalyst XL. For additional details, contact your local Eurotech representative.

Operating System Support

The Catalyst XL is compatible with the following operating systems:

- Windows® XP Professional
- Windows XP Embedded
- Windows Embedded Standard
- Windows CE 6.0
- Wind River Linux
- Select real-time operating systems

For details about available support of each operating system, contact your local Eurotech representative.

BIOS

The Catalyst XL incorporates a custom system BIOS developed by Eurotech.

Software Development Kit

Eurotech has developed a Software Development Kit (SDK) and its Application Programming Interface (API) for the following functions:

- System Management
- SMBus
- I²C bus

For details about the availability of these SDKs, contact your local Eurotech representative.

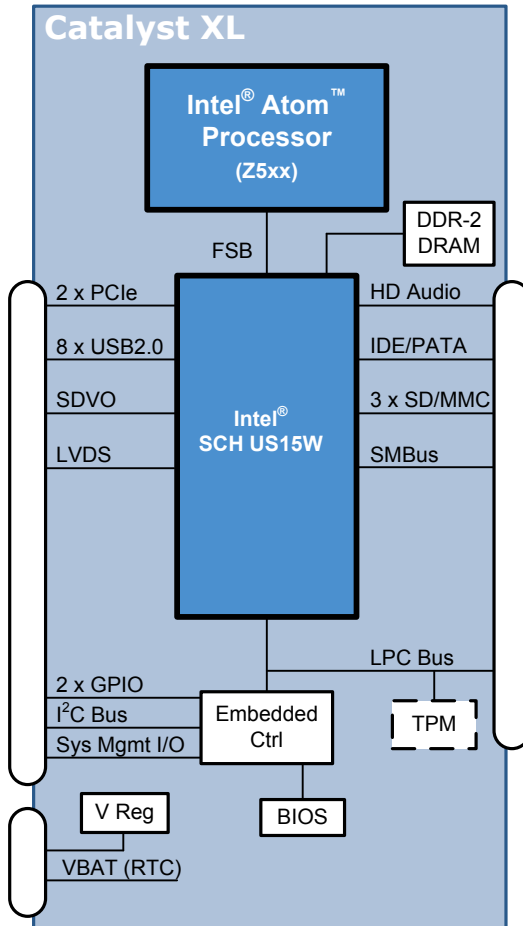
Everyware™ Software Framework

Everyware Software Framework (ESF) is an inclusive software framework that puts a middleware layer between the operating system and the OEM application. It provides industry-standard interfaces that shorten development time, simplify coding, and allow software to be ported from one Eurotech hardware platform to another. The Catalyst XL supports ESF. If your application requires ESF, contact your local Eurotech representative. Information about ESF is available at <http://esf.eurotech.com>.

Hardware Specification

Block Diagram

The following diagram illustrates the system organization of the Catalyst XL. Notice that the data connector has been divided into two sections for this illustration. The TPM is shown with dotted lines indicating that this is an optional feature.



Core Processor

The Catalyst XL bases its architecture on an integrated two-chip solution comprised of the Intel Atom processor Z5xxP/PT and Intel System Controller Hub US15WP/PT. In addition, the Catalyst XL fully integrates system functions that include system management and control implemented by an advanced chip level solution, tightly integrated power management controls, system BIOS firmware memory, and optional Trusted Platform Management (TPM) for industry-standard secure data encryption. This fully integrated and flexible feature set increases product readiness and compliance. The following sections describe the functionality and feature set of this processor technology as it relates to the Catalyst XL architecture.

Intel Atom Processor

At the core of the Catalyst XL is the Intel Atom processor Z5xxP/PT that incorporates the low-power Intel micro architecture. The Intel Atom processor executes the x86 instruction set along with extensions for SSE, SSE2, and SSE3. This processor is built on a 45 nm process using a high-K substrate.

The following are key features of the Intel Atom processor:

- Multi-threading support using Hyper-Threading Technology
- Intel Virtualization Technology
- “In-order execution” instruction pipeline and simplified decode/branch prediction
- Macro-operations that extend per clock effective instruction execution pipeline width to 2-wide and execute up to four instructions per clock cycle when combined with Hyper-Threading Technology
- Extended dynamic power management using new enhanced Intel SpeedStep[®] technology “C6” low-power states

See [Performance](#), page 58 for further details about the processor performance.

External Interrupts

The Catalyst XL provides several sources for external interrupts capable of generating a processor interrupt when the system is in power state S0. The following table lists each interrupt source with a description of its function.

Interrupt Signal	J1 Pin	Function
IDE_IRQ	A53	IDE/PATA interrupt
GPIO1	A108	System control interrupt or
GPIO2	A3	non-maskable system management interrupt
LPC_SERIRQ	A39	LPC bus interrupt
SMB_ALERT#	A33	Non-maskable system management interrupt or additional capability as wake event
PCIE_WAKE#	B55	Standard I/O device wake event signal
PCIE Port 1		PCIe message-based interrupts
PCIE Port 2		

Notice that the GPIO1, GPIO2, and SMB_ALERT# signals have multiple functions. You can access these functions through the BIOS.

Intel System Controller Hub US15W

The Intel Atom processor operates in conjunction with the Intel SCH US15W. This companion device provides a wide range of capabilities that include a 2D/3D graphics controller, PCIe, USB, SD/MMC, Intel HD Audio support, IDE/PATA, SMBus, and a RTC function. Subsequent sections describe each capability.

Trusted Platform Management (optional)

The optional on-module TPM function is compliant with the Trusted Computer Group specification version 1.2. This function provides public key generation, public key storage encryption/decryption, storage of hashes, key endorsement, and TPM initialization. As an option, the TPM is included on the LPC bus.

Embedded Controller

An embedded controller included on the Catalyst XL performs three main functions: standard firmware hub (FWH) logic emulation, ACPI power management, and hardware monitoring. See [Embedded Controller](#), page 61 for electrical specifications for the external I/O signals provided by the embedded controller.

Combined with the system BIOS memory, the embedded controller provides logic emulation of standard FWH functions. It connects to the Intel SCH US15W using the LPC bus and to the system BIOS memory using a serial peripheral interface (SPI). See [Non-Volatile Memory](#), page 19 for a description of the system BIOS memory.

As a second function, the embedded controller supports ACPI power management. It functions, in conjunction with an on-module power switch, to control proper sequencing of voltages ensuring proper start-up, shutdown, and power saving transitions. To manage the input power voltages, the embedded controller provides power state signals to the carrier board and receives a power valid signal from the carrier board. See [Power Requirements](#), page 28 for further details about power management.

Lastly, the embedded controller provides hardware monitoring for voltage and temperature. Voltage monitoring measures the input power and on-module voltage regulators. Temperature monitoring measures temperatures on the Intel Atom processor die and near the memory chips. You can also monitor temperatures on your carrier board by connecting an external temperature sensor to the embedded controller I²C bus provided on connector J1. See [I²C Bus](#), page 22 for further details about the I²C bus.

The Catalyst System Management API provides a software interface for temperature monitoring. For details about this API, refer to the *Catalyst System Management Programmer Reference (Eurotech document #110122-2021)*.

Memory

The Catalyst XL combined with a carrier board provides a variety of storage capabilities. The following sections describe the different types of memory supported and provide details about implementation.

Synchronous DRAM

Double Data Rate Synchronous DRAM (DDR-2) is used on the Catalyst XL for system main memory and frame buffer memory. Modules are available with 512 MB, 1 GB, or 2 GB DDR-2 DRAM. The data bus supports 64-bit accesses with a maximum burst bandwidth of 4.2 GB/s (8 B @ 533 MHz). The memory bus operates at the same frequency as the front side bus. See [Performance](#), page 58 for specifications.

The Intel Atom processor supports unified memory architecture in which the integrated 2D/3D graphics controller memory is “unified” with the system main memory. The default frame buffer is 4 MB with options in the BIOS Setup for selecting an 8 MB option. Extended graphics memory space is available up to 256 MB. The graphics driver controls this size based on usage.

Non-Volatile Memory

The Catalyst XL includes non-volatile memory for system BIOS storage and a real-time clock (RTC) functionality. The system BIOS options include an on-module system BIOS memory with an external BIOS device supported on a carrier board.

BIOS and Configuration Data

A serial interface flash memory device stores the BIOS boot firmware, BIOS Setup settings, and module configuration data on the Catalyst XL. Standard configuration is 1 MB. The flash device performs logically as a firmware hub (FWH) and connects to the on-module embedded controller using a serial peripheral interface (SPI). This system BIOS memory supports pre-programmability at the device level, in-circuit programming on module, and updates using a run-time flash utility. In addition, programmable write protection is available using multiple flash sectors.

As an alternate FWH implementation, the Catalyst XL supports an external BIOS option on the carrier board. The external device connects to the LPC bus. Two signals, CLK_LPC_FWH (J1 pin A36) and FWH_WP# (J1 PIN A2) are reserved for the optional external BIOS option. The signal CLK_LPC_FWH provides the clock for the external BIOS memory. Connect this signal to one load on the carrier board. See [Design Guidelines](#), page 43 for routing guidelines.

The input signal, THERM_ALERT, can be used to support booting the Catalyst XL from an external device. THERM_ALERT is pulled up on the module, but if it is held low when the system comes out of reset, the external BIOS device assumes the FWH ID 0 location and the system boots from that device. See [System Management](#), page 27 for timing details.

Real-Time Clock

The Intel SCH US15W includes a RTC function. It retains the system date and time when the system is powered down as long as the 3.3 V “always” power or backup power is provided to the chip. See [Power Supply Architecture](#), page 29 for further details about the RTC backup power.

The Catalyst System Management API provides a software interface for controlling the RTC function. For details about this API, refer to the *Catalyst System Management Programmer Reference (Eurotech document #110122-2021)*.

External Memory Interfaces

Four types of external memory interfaces provide mass storage options on a carrier board. The Intel SCH US15W supplies the signals for an IDE/PATA interface, eight USB ports, three SD/MMC interfaces, and two PCIe x 1 lane that can connect external memory to the Catalyst XL. Connector J1 provides the signals for each option. Include support circuitry and connectors on your carrier board.

The high-speed differential and single-ended signals associated with these external memory interfaces require strict routing constraints on the carrier board. See [Design Guidelines](#), page 43 for routing guidelines.

IDE/PATA Disk Drive

The Catalyst XL provides an IDE/Parallel ATA (PATA) interface for mass storage supporting up to two devices: one master and one slave. A common application is to connect this interface to a 2.5-inch IDE/PATA disk drive.

The following table lists supported IDE/PATA Standards and Modes.

IDE/PATA Standard	Transfer Modes Supported	Transfer Rate (Mbps)
ATA-1 (ATA, IDE)	PIO modes 0, 1, 2	3.3, 5.2, 8.3
	Single-word DMA modes 0, 1, 2	2.1, 4.2, 8.3
	Multi-word DMA mode 0	4.2
ATA-2, ATA-3 (EIDE, Fast ATA)	PIO modes 3, 4	11.1, 16.6
	Multi-word DMA modes 1, 2	13.3, 16.6
ATA/ATAPI-4 (Ultra DMA, Ultra ATA)	Ultra DMA modes 0, 1, 2 (a.k.a. Ultra DMA/33)	16.7, 25.0, 33.3
ATA/ATAPI-5 (Ultra-DMA, Ultra ATA)	Ultra DMA modes 3, 4 (a.k.a. Ultra DMA/66)	44.4, 66.7
ATA/ATAPI-6 (Ultra-DMA, Ultra ATA)	Ultra-DMA mode 5 (a.k.a. Ultra DMA/100)	100 (reads), 89 (writes)

USB Mass Storage Device

A USB mass storage device can connect to one of eight USB ports on the Catalyst XL. Any USB device that has USB drivers installed on the Catalyst XL can connect to the USB host ports. See [USB](#), page 21 for a description of these ports.

SD Cards

You can use a SD/MMC interface to implement a SD/MMC socket on a carrier board providing mass storage. See [Secure Digital and MultiMediaCard](#), page 22 for details about using the SD/MMC interfaces.

PCIe Memory Card

A PCIe x1 memory card can connect to one of two PCIe x1 lane available on the Catalyst XL. See [PCI Express Bus](#), page 21 for a description of the PCIe capability.

Communications

The Catalyst XL supports several industry-standard channels for communication with peripheral and peer devices on the carrier board. These include PCIe, USB, SD/MMC, SMBus, and I²C bus. The Intel SCH US15W provides the PCIe, USB, SD/MMC and SMBus signals, and the embedded controller supplies the I²C signals. The Catalyst XL does not limit flexibility by integrating fixed function I/O components. All communication signals are available on connector J1 providing flexibility and ease of implementation on the carrier board. This allows development of a unique carrier board optimized for your requirements.

PCI Express

A key capability of the Catalyst XL is its PCI Express (PCIe) support. The Intel SCH US15W includes two PCIe one lane ports (PCIe x 1) that support 2.5 Gbps bandwidth in each direction. These high-speed differential pairs require strict routing constraints on the carrier board and AC coupling. See [Design Guidelines](#), page 43 for routing guidelines.

The following table shows the mapping of connector J1 to the Intel SCH US15W's PCIe ports.

Connector J1 Pin	Connector J1 Signal Name	Intel SCH US15W PCIe Port
A99, A98 B95, B94	PCIE1_PET+, PCIE1_PET- PCIE1_PER+, PCIE1_PER-	1
B99, B98 A95, A94	PCIE2_PET+, PCIE1_PET- PCIE2_PER+, PCIE2_PER-	2

An on-module clock generator supplies the PCIe clocks for each bus. Additional input signals, PCIEx_CLKREQ#, control each reference clock. On the carrier board, these signals connect to the PCIe slots indicating the presence of a PCIe device. When activated, this signal enables the PCIe clock for the device. See [Clock Generator](#), page 62 for electrical specifications.

USB

USB Host

The Intel SCH US15W provides eight Universal Serial Bus (USB) ports. Six ports, USB0-5, function as general-purpose USB host ports and include over-current detection inputs. These ports support the USB 2.0 specification operating at low (1.5 Mbps), full (12 Mbps) and high (480 Mbps) speeds. Use these ports to connect to devices external to the carrier board. USB mouse and keyboard are the most common client devices, but you can connect any USB device that has USB drivers installed on the Catalyst XL.

The two remaining USB ports, USB6 and USB7, operate at high speed only and do not support general-purpose USB host operation. These ports do not support the USB 1.1 specification, and connector J1 does not provide the associated over-current detection signals. When possible, connect these ports to devices on the carrier board.

In order to create a fully functioning USB host port, include the host power supply, current limiter circuits, EMI chokes, and over-voltage protection on your carrier board. See [Design Guidelines](#), page 43 for routing guidelines. The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The carrier board must supply the 5 V power required by client devices. Use a power switch with the corresponding over-current detection for each port.

USB Client or USB Host

As an optional configuration, USB2 is capable of operating as a USB client port at high speed only. USB client devices are self-powered or can receive power from the host computer. Since the USB cable does not power the Catalyst XL, it does not need a power input. However, the USB input power is useful for sensing when a USB cable is connected. Use the input signal USB_CLIENT (J1 pin B53) to detect a USB cable connection. When a client is connected, this pin should be connected to a 4.7kΩ pull-up resistor to 3.3 V on the carrier board. When the port is used as a host port or no client is connected, this signal should be actively driven low on the carrier board.

Secure Digital and MultiMediaCard

The Catalyst XL includes three Secure Digital and MultiMediaCard (SD/MMC) interfaces for memory and I/O expansion. You can use these interfaces to implement a SD/MMC socket on a carrier board providing mass storage or to develop customer unique add-in cards. SD/MMC2 provides 8-bit operation, while SD/MMC0 and SD/MMC1 provide 4-bit operation.

These SD/MMC interfaces support the following specifications:

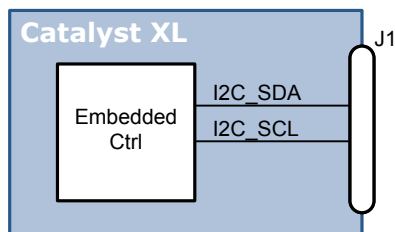
- MMC 4.0 specification allowing clock frequencies up to 48 MHz and bus widths of 1, 4, or 8 bits.
- SDIO 1.1 specification allowing clock frequencies up to 24 MHz and bus widths of 1 or 4 bits.

In addition to the SD/MMC signals, connector J1 includes signals to control SD/MMC support circuitry on the carrier board. Each interface includes signals to control a power FET and to drive a LED. See [Design Guidelines](#), page 43 for routing guidelines.

I²C Bus

I²C (Inter-IC) bus is a multi-master, "two-wire" synchronous serial bus for communications between integrated circuits (ICs) and for addressing peripherals in a system. Connector J1 includes an external connection to the I²C bus of the Catalyst XL embedded controller. This bus is intended for communication between the embedded controller and the temperature monitoring circuitry on the carrier board; however, it can be used to communicate with other I²C devices. The Catalyst XL must act as the bus master.

The following diagram illustrates the I²C architecture on the Catalyst XL.



When possible, use the SMBus to communicate with devices on the carrier board instead of the I²C bus. When this bus is used on your carrier board, power all devices connected to it using the 3.3 V "Always" (V3.3A) power or isolate the devices from the bus when powered off. Notice that the module does not include termination on this I²C bus. Include 10kΩ pull-up resistors to V3.3A on the carrier board.

The Catalyst I²C bus API provides a software interface for controlling the I²C bus. For details about this API, refer to the *Catalyst I²C Bus Programmer Reference (Eurotech document #110122-2031)*.

System Management Bus

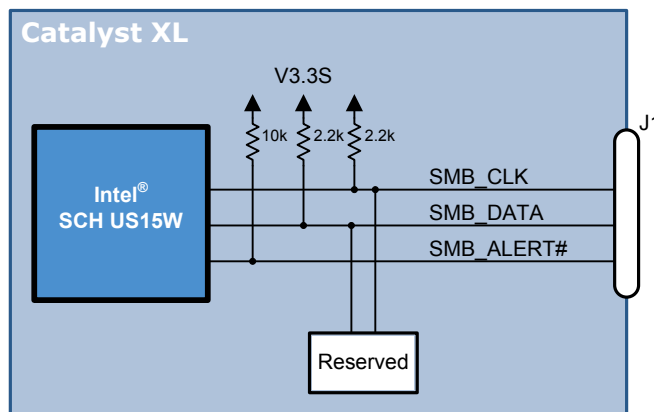
System Management Bus (SMBus) follows the same operating principles as I²C. Similar to I²C, SMBus is a “two-wire” bus allowing multiple devices to communicate with each other. Devices function as bus masters and bus slaves. SMBus enables communication between devices and allows connection of devices that require legacy software accessibility thru standard SMB addressing.

The Catalyst XL provides an external connection on connector J1 to its SMBus with the Intel SCH US15W acting as bus master. This bus supports the System Management Bus Specification, Version 1.0. In addition, the module supports hardware alerting on the SMBus using the I/O signal SMB_ALERT#.



Note: SMBus is not compatible with all I²C devices. Review the device data sheet carefully before connecting an I²C device to the SMBus.

The following diagram illustrates the SMBus architecture on the Catalyst XL.



Notice that the module includes pull-up resistors to V3.3S on the SMBus. On your carrier board, power all devices connected to this bus using the V3.3S power or isolate the devices from the bus when powered off.

The following table lists the addresses of the SMBus devices on the Catalyst XL.

Module Device	Address	Function
Reserved	0101 0010	Write
	0101 0011	Read
Reserved	1101 0010	Write
	1101 0011	Read

The Catalyst SMBus API provides a software interface for controlling the SMBus. For details about this API, refer to the *Catalyst SMBus Programmer Reference (Eurotech document #110122-2022)*.

Display and User Interface

The Intel SCH US15W includes an integrated 2D/3D graphics controller supporting hardware-accelerated graphics display and video processing capabilities. The controller provides two independent display outputs. A 4-channel LVDS output drives the primary display, while a Serial Digital Video Out (SDVO) drives a secondary display. In addition, the Catalyst XL provides discrete backlight control signals.

This section summarizes the Catalyst XL graphics display and video processing capabilities. Display resolutions are specified at the maximum refresh rate and color depth. Higher resolutions may be possible at lower refresh rates and color depths. This relationship is due primarily to the increased processing bandwidth required at higher output resolutions.

LVDS Display and Backlight Control

LVDS Display

The growing demand for higher resolution displays has been met with design limitations on the interface between the LCD and graphics controller. Increased resolution LCDs require an increased clock speed, a larger number of data lines, and a higher power consumption. LVDS serial data transmission addresses these issues by providing a high-speed, low-power interface on a single pair of wires per channel. The Intel SCH US15W supplies a LVDS output to drive a primary display.

The following table summarizes the LVDS display output capabilities.

Feature	LVDS Display
Resolution	Single display up to 1366 x 768 at 85 Hz, 8-bit per lane or dual display up to 1280 x 768 at 85 Hz, 8-bit per lane
Configurations	Extended Display Identification Data (EDID) and non-EDID
Operation	Extended desktop or clone mode
Display parameter	Centering, scaling, and rotation

The LVDS display output consists of four LVDS data pairs, as well as a LVDS pixel clock, supporting 18-bit and 24-bit color. If your application requires transmission over a display cable greater than 7 inches, include an LVDS buffer/repeater on your carrier board to boost the data and pixel clock signals. Use controlled impedance cables that target $97 \Omega \pm 20\%$. Cables should not introduce major impedance discontinuities that cause signal reflections. The differential pairs also require strict routing constraints on the carrier board. See [Design Guidelines](#), page 43 for routing guidelines.

Additional capabilities include the discrete signal L_VDDEN (J1 pin A32) that controls power to the display and an I²C interface (L_DDC_DATA on J1 pin B28, L_DDC_CLK on J1 pin A29) for communication with the LCD Display Data Channel (DDC).

Backlight

Most LCDs include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Backlight inverters drive the panel backlights. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. To reduce power consumption, most backlight inverters include control signals to dim and turn off the backlight.

To support these features, the Intel SCH US15W supplies three backlight control signals and an I²C bus (L_CTLB_DATA on J1 pin B25, L_CTLA_CLK on J1 pin B29) for communication with the backlight. The following table describes the three backlight control signals.

Signal	J1 Pin	Type	Description
L_BKLTCTL	B33	O-PWM	Controls the intensity of the backlight
L_BKLTEN	B32	O	Turns power to the backlight on or off
L_BKLTSEL0_GPIO#	B58	O	Selects backlight control (PWM vs. I ² C)

The Catalyst System Management API provides a software interface for controlling the backlight brightness. For details about this API, refer to the *Catalyst System Management Programmer Reference (Eurotech document #110122-2021)*.

Serial Digital Video Out

In addition to the LVDS display output, the Intel SCH US15W drives a secondary display on the SDVO. SDVO allows for an additional video output using a PCIe x16 slot implemented on a carrier board or a direct connection to an on-board device. This secondary output supports external devices that convert the SDVO protocol to DVI, HDMI, LVDS Analog-CRT, and TV-Out interfaces. Contact your local Eurotech technical support for recommended Intel/HP SDVO cards.

The following table summarizes the SDVO capabilities.

Feature	SDVO Interface
Resolution	Single display up to 1280 x 1024 at 85 Hz, full color or dual display up to 1280 x 768 at 85 Hz, full color
Configurations	EDID and non-EDID
Operation	Extended desktop or clone mode
Formats	DVI and HDMI formats with panning and device hot plug, LVDS formats with scaling, and TV-Out in NTSC, PAL and SECAM SD formats

The SDVO includes seven high-speed differential pair signals. Routing the high-speed differential pairs on the carrier boards requires strict design constraints. See [Design Guidelines](#), page 43 for routing guidelines.

In addition, the SDVO includes an I²C bus (SDVO_CTLDATA on J1 pin A30, SDVO_CTLCLK on J1 pin B30). This bus connects to a SDVO panel DDC. The Catalyst XL does not include termination on the I²C signals. Include 3.3k Ω pull-up resistors to +2.5V on the carrier board. If your carrier board does not generate +2.5V and your design does not use the SDVO I²C signals, these signals can be pulled to V3.3S with 1M Ω resistors.

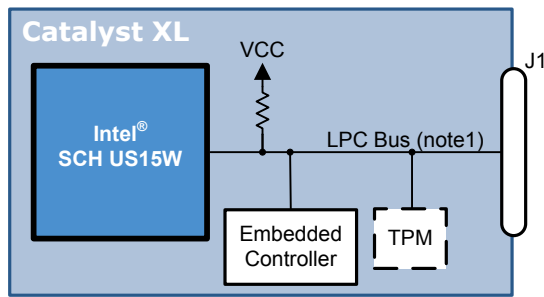
Inputs and Outputs

Several signals support a modular architecture and provide I/O expansion. The Catalyst XL includes a Low Pin Count bus supporting legacy I/O capabilities and multiple discrete I/O signals performing system reset, system management, power control, and general-purpose input and output. Connector J1 includes all I/O signals.

Low Pin Count Bus

In response to the transition from ISA-based systems, the Low Pin Count (LPC) bus provides a migration path for legacy I/O capabilities. This bus enables general-purpose I/O expansion and provides communication to low-bandwidth devices. For this purpose, the Intel SCH US15W supplies a LPC bus supporting the LPC 1.1 Specification. On the Catalyst XL, this bus connects to the Intel SCH US15W, the embedded controller, and optional TPM.

The following diagram illustrates the LPC bus architecture.



Note:

1. For details about the termination on individual signals of the LPC Bus, see [J1](#), page 49.

Externally, the LPC bus provides general-purpose expansion. Common applications on the carrier board include an external BIOS option and a Super I/O Controller that provides I/O capabilities such as serial ports, keyboard, mouse, IrDA, and general-purpose I/O.

An additional signal, LPCPD# (J1 pin B2), is driven by the embedded controller indicating an in-process system power state change to attached LPC bus devices. When this signal is active, the attached peripherals should prepare for a power down event.

Ensure that the LPC signals are routed as critical nets on the carrier board and include 10kΩ pull-up resistors to V3.3S on the LPC_ADx signals. See [Design Guidelines](#), page 43 for routing guidelines.

Reset Signals

One of two signals resets the circuitry on the module and carrier board. One signal originates from the module, while the second signal originates from the carrier board. The output signal RESET# includes several loads on the Catalyst XL. Include a buffer on the carrier board to drive additional loads.

The following table compares the reset signals.

Signal	J1 Pin	Type	Description
RESET#	B56	O	Use as a power-on reset to reset all devices on the carrier board. Output is driven by the module, forces complete system hardware reset, and is used for proper reset timing and logic synchronization.
FP_RESET#	A59	I	Do not use this signal as a power-on reset. FP_RESET# will not be detected until RESET# is de-asserted. Input initiates a hardware reset including the Intel Atom processor and Intel SCH US15W.

In addition to the hardware resets, the input signal H_INIT# (J1 pin B3) initiates a soft reset of the module. See [Reset Circuitry](#), page 60 for electrical specifications.

System Management

The signal THERM_ALERT (J1 pin A109) can be used for two system management functions as described in the next table. If your application requires specific usage of this signal, contact your local Eurotech representative for functional details.

State	Type	Description
While running	O	Can be set up to indicate detection of a thermal “over-temperature” event.
At system reset	I	Can be set up to support boot from an external device. Low for a minimum of 200ns immediately preceding de-assertion of system reset signal enables the external BIOS option.

General-Purpose Input and Output

The embedded controller supplies two general-purpose input and output (GPIO) signals as listed in the following table. See [Embedded Controller](#), page 61 for electrical specifications.

Signal	J1 Pin	Description
GPIO1	A108	Embedded controller GPIO
GPIO2	A3	Embedded controller GPIO

In addition, the signals described in the following table can be used as GPIO if their primary function is not required by your application.

Signal	J1 Pin	Primary Function	Alternate Function
FWH_WP#	A2	External BIOS option write protect	GPIO3
L_BKLTSEL	B58	Selects backlight control (PWM vs. I ² C)	GPIO4
USB_CLIENT	B53	USB2 client detection	GPIO5

These signals are software-controlled using the Catalyst System Management API. For details about this API, refer to the *Catalyst System Management Programmer Reference* (Eurotech document #110122-2021).

Intel High Definition Audio

The Intel® High Definition Audio (Intel HD Audio) Specification implements high quality audio in a PC environment. The specification defines a uniform interface between a host computer and audio codec specifying register control, physical connectivity, programming model, and codec architectural components. The Intel SCH US15W includes an Intel HD Audio interface capable of supporting up to two external audio codecs. Docking functionality is supported allowing control of an external switch for isolation of the codec within a docking station during normal docking request and acknowledge cycles.

All Intel HD Audio signals are available on connector J1. The interface supports 3.3 V or 1.5 V signaling levels. Standard modules support 3.3 V signaling levels. Contact your local Eurotech technical support if your application requires 1.5 V. For the Intel HD Audio electrical specification

Include audio codecs along with amplifiers, switches, and connectors on your carrier board. See [Intel High Definition Audio](#), page 60 for electrical specifications and [Design Guidelines](#), page 43 for routing guidelines.

Power Requirements

Power management is especially critical in high-performance systems that also require low power dissipation. Handheld and portable systems available today never really turn "off". They make use of power management techniques that cycle the electronics into power saving modes, but never fully remove power from the full system.

Embedded system designers using the Catalyst XL should have a clear understanding of how the system design allocates power usage. Create a power budget that takes into account the types of devices that are used with the Catalyst XL. This section provides information about power and power management on the Catalyst XL.

Low Power States

The Catalyst XL supports the Advanced Configuration and Power Interface (ACPI) specification. Unlike previous power standards that were BIOS-based, ACPI allows OS-directed power management. It specifies an industry-standard interface for both hardware and software that facilitates power and thermal management. This section describes how the Catalyst XL makes use of the ACPI low power modes. See [Power Consumption](#), page 58 for baseline power consumption for the module.

The ACPI specification defines the low power states for ACPI-compliant systems. The following table describes the states supported by the Catalyst XL.

State	Mode	Description
S0	Full Operation	All devices are operational with dynamic power management functions active.
S3	Standby or Sleep	The Intel Atom processor and Intel SCH US15W are powered down. Active operating system context stored in DRAM is retained using low-power self-refresh. Wake events are active and enable a transition back to full operation.
S4	Hibernation	The Intel Atom processor, Intel SCH US15W, and DRAM are powered down. Operating system context is saved to disk storage prior to powering down system voltage rails. Limited wake events are active. Resume to full operation is dependent on numerous system components including the disk storage device.
S5	Power down	The Intel Atom processor, Intel SCH US15W, and DRAM are powered down. The embedded controller is active but may be in low-power mode. No operating system context is preserved.

Wake events transition the Catalyst XL from a low-power state back to full operation. The following table lists the signals that can function as wake events. These signals are valid as wake event inputs in power state S3.

Wake Event	J1 Pin	Description
FWH_WP#	A2	Wake event when programmed as GPIO
SMB_ALERT#	A33	SMBus activity alert
USB_CLIENT	B53	Wake event when programmed as GPIO
PCIE_WAKE#	B55	Standard I/O device wake event signal
L_BKLTSEL	B58	Wake event when programmed as GPIO
PWR_BUTTON#	B59	Power button input

Power Supply Architecture

The architecture of the power supply partitions the power generation across the Catalyst XL and the carrier board. The module requires 5 V and 3.3 V input voltages supplied by the carrier board. It is the responsibility of the carrier board designers to provide input power protection as required by their application. This is especially important if the power supply wires will be subject to EMI/RFI or ESD. On-module regulators generate the core power and all other powers required by the supporting circuitry. See [Power Supply](#), page 59 for electrical specifications and details about each power rail.

Input Power Voltages

The following table describes the input power voltages required by the Catalyst XL.

Name	Power State	Description
V3.3A	S4 exit, S5 exit, S0 operation, and S3 operation	3.3 V “always” power for up/down circuitry only
V3.3S	S0 operation	3.3 V normal operating power
V3.3	S0 operation and S3 operation	3.3 V primary supply voltage for most of the on-board regulated voltages
V5A	S4 exit, S5 exit, S0 operation, and S3 operation	5 V “always” power for up/down circuitry only
V5S	S0 operation	5 V normal operating power
V_BATTERY		Backup power for the RTC

Each power rail should be routed as a power plane on your carrier board with sufficient bulk decoupling and local decoupling on each plane. See [Design Guidelines](#), page 43 for additional details about carrier board design.

Notes:

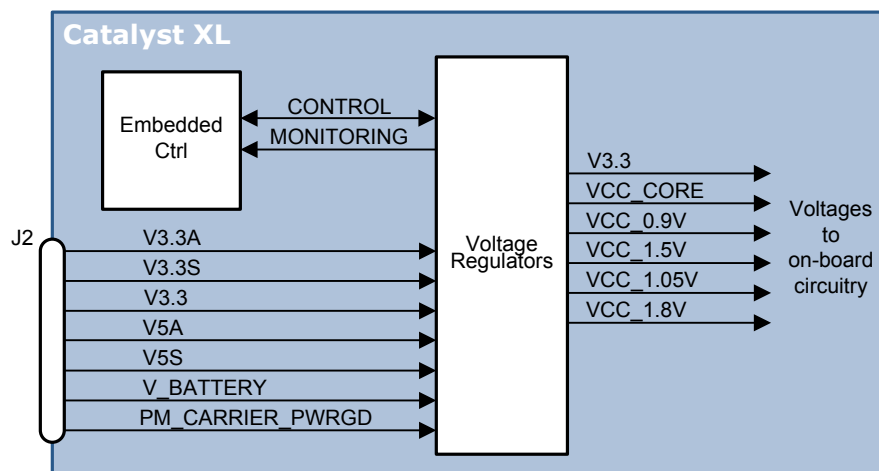
The V5A rail should lead the V3.3A rail during ramp up or not lag by more than 0.7 V.



The V5S rail should lead the V3.3S rail during ramp up or not lag by more than 0.7 V.

For an example circuit, see the Eurotech reference carrier board schematic.

The following diagram illustrates the layout of the Catalyst XL power supply.



In addition to the input power voltages, connector J2 includes the signal PM_CARRIER_PWRGD. This input from the carrier board indicates that all input power voltages are fully operational and within tolerance.



Note:

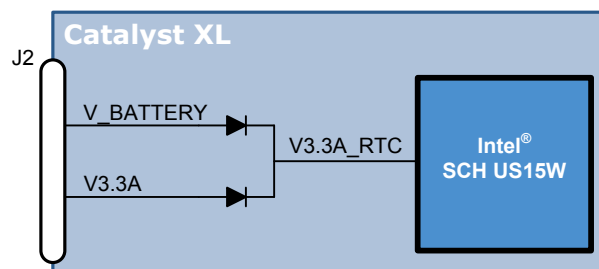
The carrier board must provide the PM_CARRIER_PWRGD signal to represent the readiness for operation.

The embedded controller functions, in conjunction with an on-module power switch, to control proper sequencing of voltages allowing for proper start-up, shutdown, and power saving transitions. In addition, it monitors input power voltages and the on-module voltage regulators. See [Embedded Controller](#), page 18 for additional details about the embedded controller.

RTC Backup Power

The Catalyst XL includes a RTC function that retains the system date and time when the system is powered down as long as the 3.3 V “always” power or backup power is provided to the module. Including a long-life 3 V battery on a carrier board is a common method to supply backup power. Use series elements, such as a diode and resistor, on the V_BATTERY output from your carrier board based on your specific requirements.

On the Catalyst XL, the V_BATTERY power input has a diode-OR with V3.3A, as shown in the following diagram.



See [Power Supply](#), page 59 for electrical specifications.

Power Switch

The input signal PWR_BUTTON# (J1 pin B59) controls a power switch included on the Catalyst XL. The function of the PWR_BUTTON# signal is dependent on the embedded controller/BIOS setup and the configuration of the operating system. The response of the system can be managed by this combination. On the standard development kit, this input is connected to a momentary button on the carrier board. Pressing this external momentary button turns the power on and off. See [Power Supply](#), page 59 for electrical specifications.

The following table details the operation of the PWR_BUTTON# signal.

PWR_BUTTON#	Operation
Momentary assertion (less than 4 seconds)	<p>On standard development kit: From shutdown, initiates a power-up sequence to full operation. From full operation, initiates an orderly shutdown sequence and turns off power.</p> <p>Options based on system configuration: From full operation, enters system sleep state. From sleep, returns to full operation.</p>
Continuous assertion (greater than 4 seconds)	Initiates a “4 second over-ride” and turns off power without notification to the operating system.



Note: Once the V5A and V3.3A rails are applied, the PWR_BUTTON# signal is not detected for up to 400 msec.

Power State Signals

The Catalyst XL provides three control signals on connector J1 indicating the power state. The embedded controller drives the two power state signals, PM_EN_S0# (J1 pin B104) and PM_EN_S3# (J1 pin B107). The on-module power switch controls the remaining signal, PM_EN_PWR (J1 pin B105). See [Power Supply](#), page 59 for electrical specifications. The next table lists these signals with the power states and input power voltages active in each state.

State	Active power rails	Power State Signals		
		PM_EN_PWR	PM_EN_S3#	PM_EN_S0#
S0	V3.3, V5S V3.3S V5A, V3.3A	High	Low	Low
S3	V3.3, V5A, V3.3A	High	Low	High
S4	V5A, V3.3A	Low	High	High
S5	V5A, V3.3A	Low	High	High



Note: Implement the exact power supply sequencing as described in this section. The module has very specific power-on sequence requirements in order to power-up and operate correctly. Power sequencing the multiple voltage rails is CRITICAL. If your design does not meet these requirements, the module will not boot.

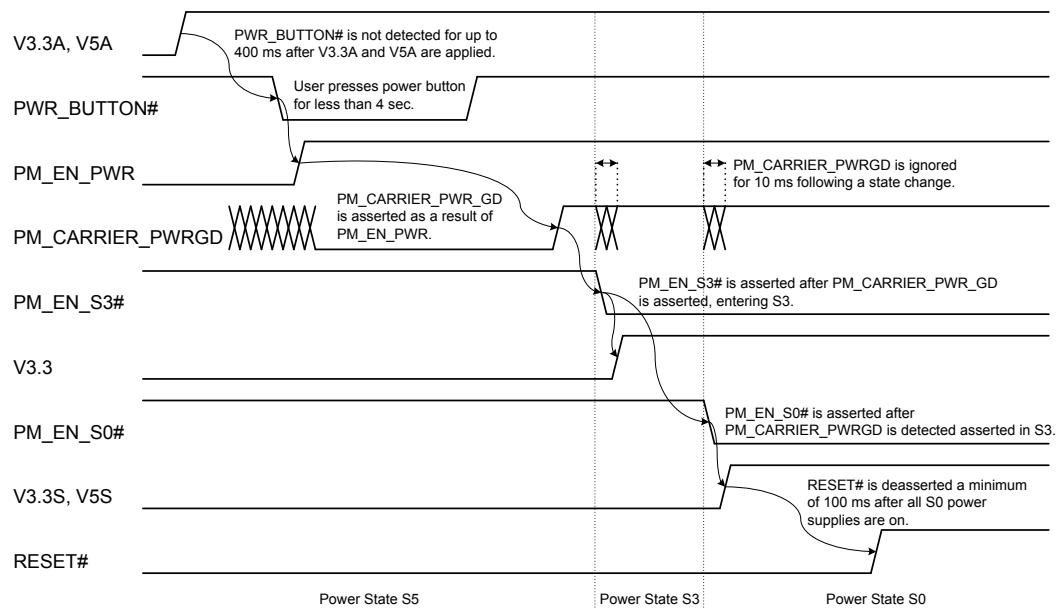
The following timing diagrams describe the relationship of the power state control signals on the Catalyst XL.

Power on initiated by power button press

During system power on, the falling edge of PWR_BUTTON# drives PM_EN_PWR high. A hardware latch on the Catalyst XL controls PM_EN_PWR. The embedded controller monitors PWR_BUTTON# until the rising edge of PWR_BUTTON#. If the power button was pressed for less than 4 seconds and the power is presently off, a power-on sequence will begin. After sampling PWR_BUTTON# high, the embedded controller waits for PM_CARRIER_PWRGD to be asserted high before driving PM_EN_S3# active (logic level low). If PM_CARRIER_PWRGD is not asserted within one second, the embedded controller will print an error message on the maintenance port and halt the power-on sequence.

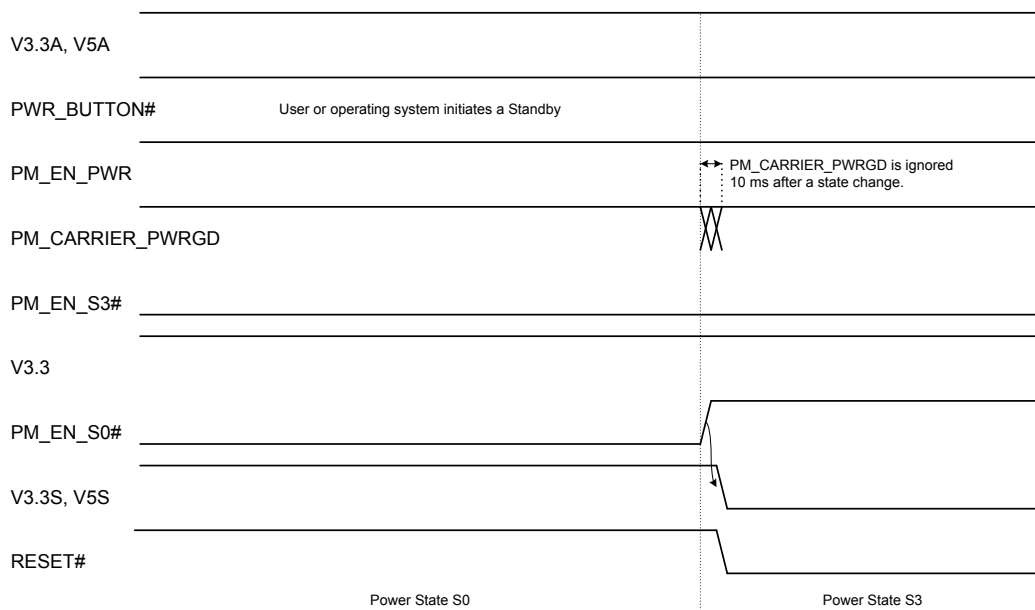
After PM_CARRIER_PWRGD is asserted, S3 power rails internal to the Catalyst XL are enabled with the assertion of PM_EN_S3# and powered by V3.3. PM_CARRIER_PWRGD is not monitored for 10 ms following the assertion of PM_EN_S3#. This provides time for the carrier board power supply to power all rails required in S3. If PM_CARRIER_PWRGD is not asserted within 100 ms, the embedded controller will print an error message on the maintenance port and halt the power-on sequence.

After the S3 power rails are within specification on the module and on the carrier board, the embedded controller asserts PM_EN_S0# (logic level low). The time from PM_EN_S3# active to PM_EN_S0# active depends on how quickly the carrier board supplies V3.3. Typically, the Catalyst XL transitions from S3 to S0 within 50msec. Once again PM_CARRIER_PWRGD is not monitored for 10 ms following the assertion of PM_EN_S0#. This allows the carrier board time to provide all power rails required in S0. On-module regulators for the processor and other devices are powered on at this time. The embedded controller monitors on-module power good signals as well as the PM_CARRIER_PWRGD signal from the carrier board to verify all S0 rails are within specification. If PM_CARRIER_PWRGD is not asserted within 1 second, the embedded controller will print an error message on the maintenance port and halt the power-on sequence. A minimum of 100 ms after all S0 power supplies are on, the RESET# signal is de-asserted.



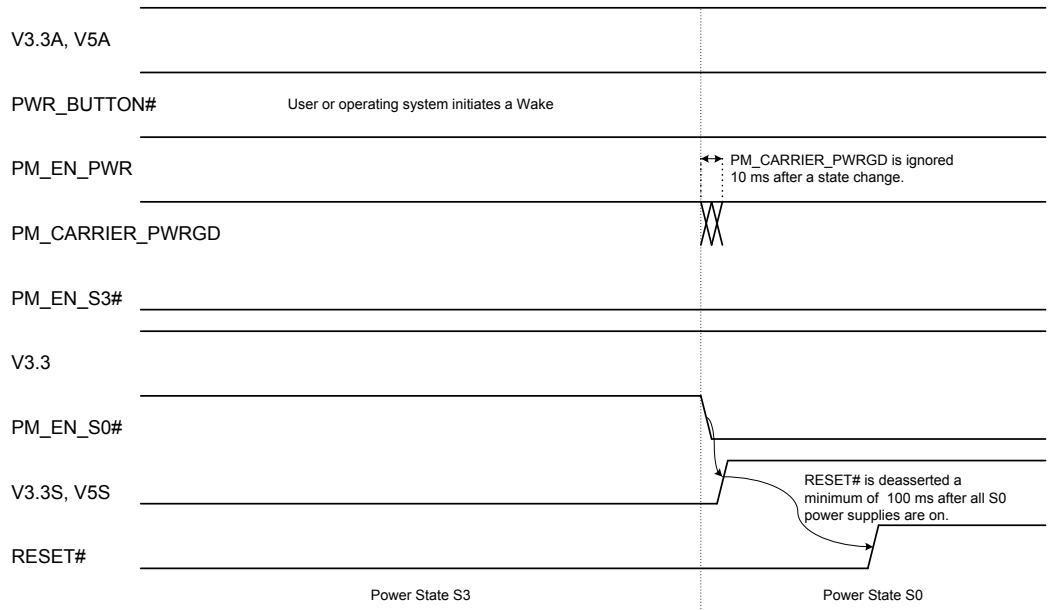
Standby (Enter S3)

The following diagram shows the Catalyst XL transitioning from S0 to S3. This transition can be initiated by the operating system or the PWR_BUTTON# input in combination with the operating system. The PM_EN_S0# signal will be de-asserted, and all S0 power rails on the Catalyst XL module will be turned off. The PM_CARRIER_PWRGD signal is not monitored for 10 ms following the de-assertion of PM_EN_S0#. This allows the carrier board S0 power rails to be turned off and PM_CARRIER_PWRGD to provide status of the power rails remaining on in S3. RESET# will be de-asserted while the system is in S3.



Standby (Exit S3)

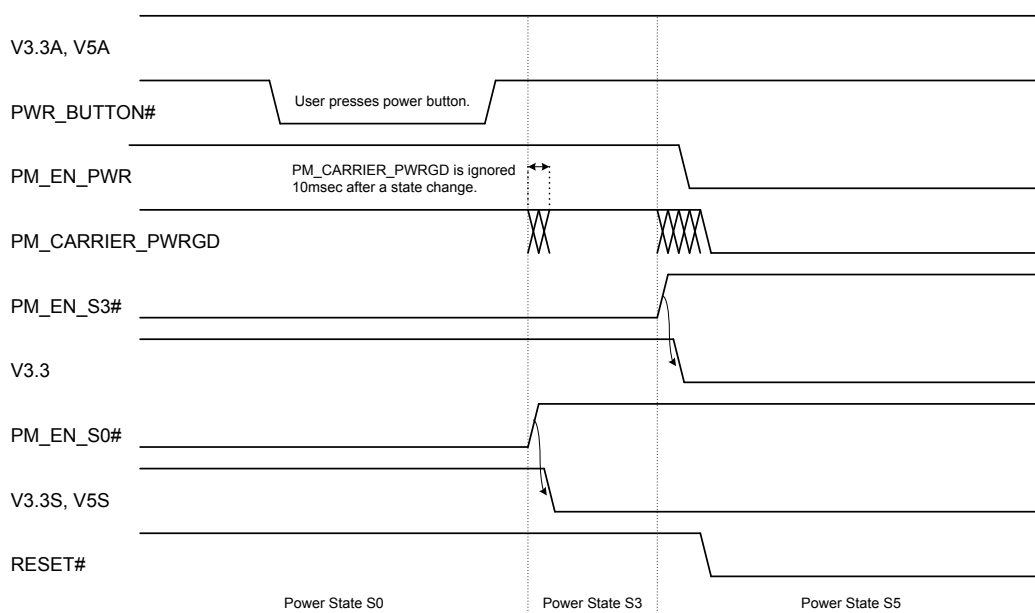
The following diagram shows the system exiting S3. The system may wake from S3 because of any wake event. PM_EN_S0# will be asserted causing all S0 power rails on the Catalyst XL to be turned on. PM_CARRIER_PWRGD will not be monitored for 10 ms after PM_EN_S0# is de-asserted. This provides time for all S0 power rails on the carrier board to be turned on and within specification. A minimum of 100 ms after all on-module supplies and carrier board S0 power supplies are within specification, RESET# will be de-asserted.



Power off initiated by power button press

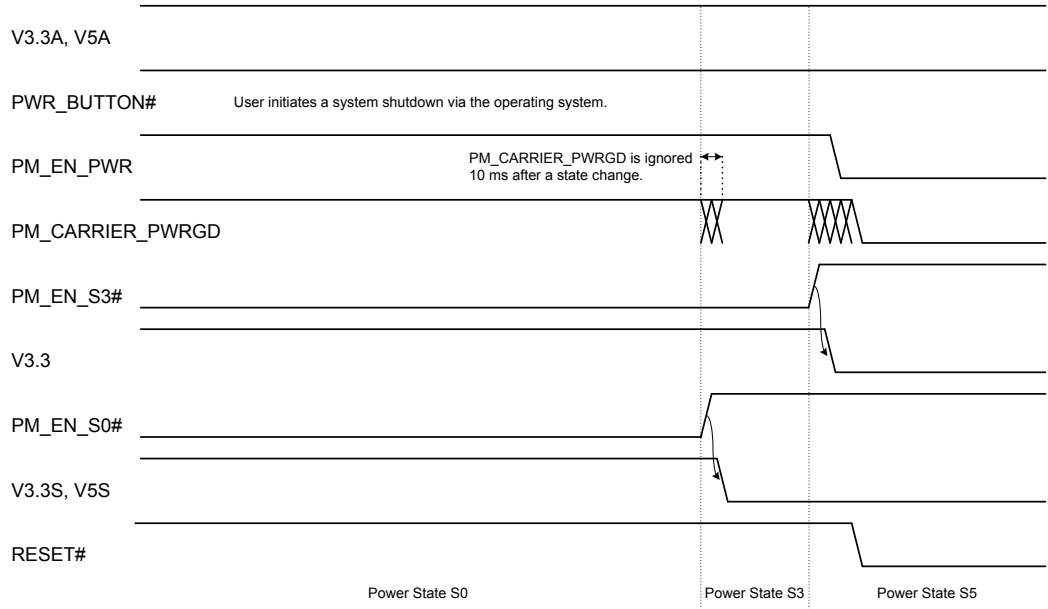
The following diagram shows a system powering off because of an assertion of the PWR_BUTTON# signal. Depending on operating system settings, a system may power off or sleep due to asserting PWR_BUTTON#. If set for a power off, the operating system will save all information needed and signal the embedded controller to perform a graceful shutdown. PM_EN_S0# will be de-asserted, followed by PM_EN_S3# and PM_EN_PWR being de-asserted. RESET# will be asserted when in S5.

If PWR_BUTTON# is asserted for more than 4 seconds, a “4 second over-ride” will be initiated and the power will be turned off without notification to the operating system.



System shutdown initiated by operating system

The following diagram shows a system powering at the request of the operating system. The user could initiate this via software control. The operating system will save all information needed and signal the embedded controller to perform a graceful shutdown. PM_EN_S0# will be de-asserted, followed by PM_EN_S3# and PM_EN_PWR being de-asserted. RESET# will be asserted when in S5.



Mechanical Specifications

This section describes mechanical and thermal design guidelines for the Catalyst XL.

Mechanical Design

Insertion and Removal

The Catalyst XL connects to the carrier board through two connectors that are in line with each other. A high-density, stacking board-to-board connector carries the data signals, while a smaller 2x7-pin 1 mm-pitch connector carries power. When fully connected, these fine pitch connectors provide reliable and durable connection. However, care is required when removing or installing the module onto the carrier board. If correct procedures for installation and removal are not followed, damage to the connectors and/or the connector pins can result.

For detailed procedures to install a module onto or remove a module from a carrier board, refer to the *Catalyst Module Installation and Removal (Eurotech document #110122-2014)*. Download this document from the Eurotech support site (<http://support.eurotech-inc.com/>, topic 2778).



Important! Observe industry-standard electronic handling procedures when handling the module. Eurotech recommends using a grounded wrist strap and heel strap. The connectors expose signals on the system bus that do not have ESD protection.

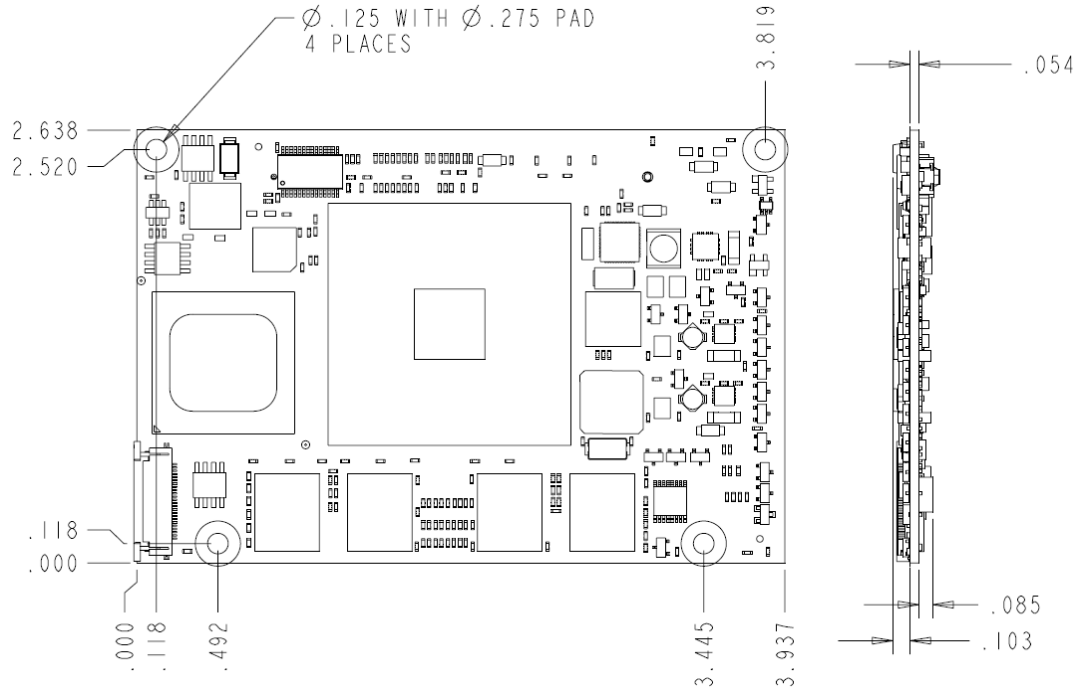
Mounting Holes

Four holes enable mounting on the carrier board. Along one side, two mounting holes are located on each corner. The mounting holes are placed off set from the corners along the opposite side of the module. The Catalyst XL ground plane connects electrically to the mounting holes through 0Ω resistors.

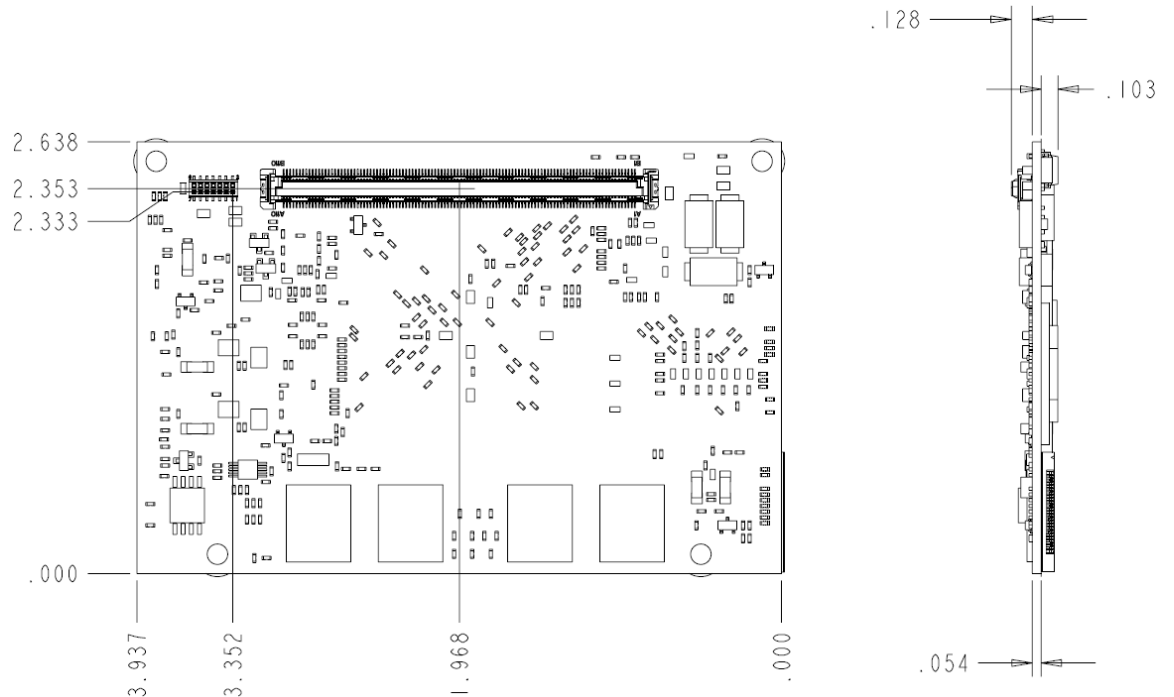
Per IPC-A-610D section 4.2.3, secure the board to standoffs using a flat washer against the board with a split washer on top between the flat washer and the screw head or nut. Do not use toothed star washers, as they cut into the plating and laminations of the board over time and will not produce an attachment that will withstand vibration and thermal cycling.


Mechanical Drawing

The following mechanical drawing specifies the dimensions of the Catalyst XL, as well as locations of key components on the board. All dimensions are in inches. The first diagram illustrates the top and side views of the module.



The next diagram illustrates the bottom and side views of the module. Notice connector J1 and J2 are located on the underside.

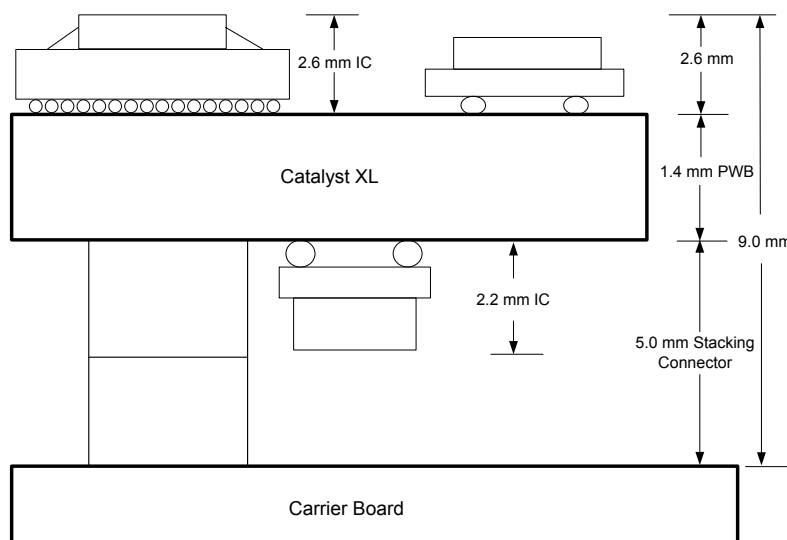


 **Note:**
 For a 2D CAD drawing and 3D CAD model, check the Eurotech support site (<http://support.eurotech-inc.com/>) or contact your local Eurotech representative.

Total Stack Height

Selection of low profile stacking connectors and components minimizes the total stack height of the Catalyst XL and carrier board. The module uses stacking board-to-board connectors to mate with a carrier board. The mating connectors on the carrier board can be either 5 mm or 8 mm stacking height. When 5 mm stacking board-to-board connectors are used, the total board height combined with the connector clearance results in a total stack height of less than 10 mm. You may place components under the module on a custom carrier board. However, the design must allow adequate heat dissipation.

The following diagram illustrates the total stack height using 5 mm stacking connectors on the carrier board.



Thermal Management

This section provides detailed data about thermal management for the Catalyst XL.

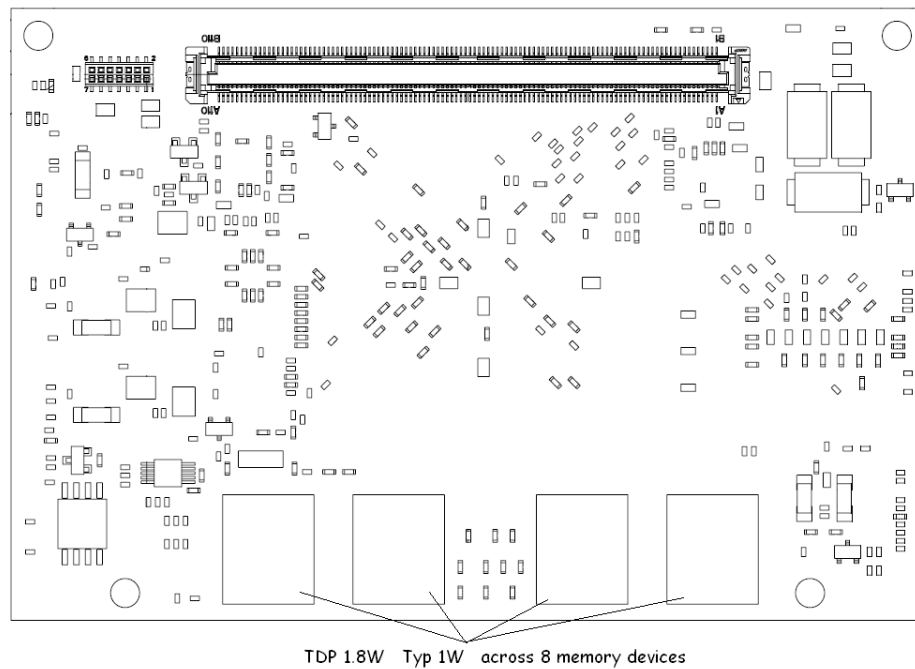
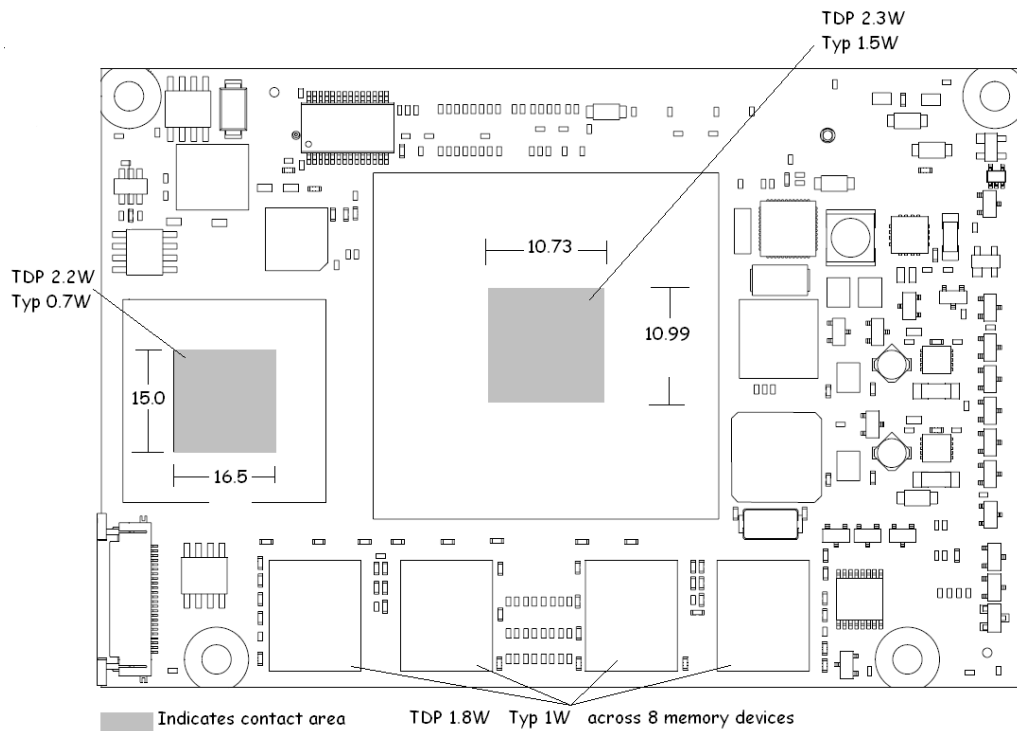
The following table summarizes the power dissipation and thermal design power for the Catalyst XL. The three key components on the Catalyst XL are the Intel Atom processor, Intel SCH US15W, and DDR-2 DRAM. The local ambient temperature of the module is defined by the temperatures at these three thermal design interface contact points.

Component	Thermal Design Power – Max Point	Typical (High End Application)	Units
Intel Atom Processor			
Interface temp - +95°C max. Copper contact, 15.0 x 16.5 mm	2.2	0.7	W
Intel SCH US15W			
Interface temp - +95°C max. Direct die contact, 10.73 x 10.99 mm	2.3	1.5	W
DDR-2 DRAM			
8 devices (4 top, 4 bottom) Combined power	1.8 (0.225 per device)	1.0 (0.125 per device)	W
System devices			
Combined power	1.2	0.9	W

Thermal Design Power – Max Point is a representation of the expected peak power dissipation of each component or component group as viewed separately. The actual power consumption in real-world applications is not expected to reach this level for any given device and never in combination. However, the thermal management solution should accommodate proper control of temperature rise so as not to exceed the maximum thermal surface interface temperatures as identified for key components (i.e. Intel Atom processor and Intel SCH US15W).

Typical (High End Application) is a realistic typical application design point for a fully active system with advanced graphics/video processing and I/O simultaneous data transfers. Some applications may utilize more CPU versus I/O processing for example, and the respective power load will shift between sub-systems based on active processing and system state. Many applications will consume considerably less power.

The following diagrams illustrate the location of the three key thermal design interface contact points on the Catalyst XL, top side and bottom side.



Carrier Board Design

An application-specific carrier board integrates with the Catalyst XL to meet various system requirements. The Catalyst XL Development Kit includes a carrier board designed to maximize the Catalyst XL functionality. This carrier board implements many industry-standard interfaces and provides a reference for custom carrier boards optimized for your requirements. This section includes many of the considerations followed in the design of the Catalyst XL Development Kit carrier board.

Design Guidelines

Design Constraints

Increasing reliability is a key consideration in the Catalyst XL design. Several constraints followed in the module design and printed wiring board (PWB) layout ensure superior product reliability and compatibility. Use similar constraints in the carrier board design.

The following are the design considerations used to improve the Catalyst XL reliability:

- Advanced high-speed signal routing techniques
 - Strict adherence to signal routing rules as collaborated with Intel design and simulation teams
 - Minimum and maximum trace lengths
 - Total, segment, and multi-segment including package length compensation
 - Bus and group length matching to tight tolerances
 - Continuous trace matching for differential pair routing
 - Impedance matching and controlled design
 - Consideration of I/O buffer characteristic variances over extended temperature ranges for improved electrical performance
 - 100% continuous ground return path for all high-speed signals
 - Routing over continuous planes for consistent transmission line impedance and clean, reliable signal transitions
- Conservative printed wiring design construction
 - Durable feature sizes and construction elements
 - Pads, fills, and holes optimized for ROHS processing and long term reliability
 - Buried power planes between ground layers to eliminate coupling with high-speed signals
 - De-rating for current loading on the power regulation circuit and interface
 - No bottom side “hot” power regulation components underneath the Intel Atom processor or the Intel SCH US15W that would reduce thermal performance

EMI/RFI Protection

Many products using Eurotech single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. The Catalyst XL incorporates the following design considerations that reduce emission and improve immunity:

- Four extra solid ground planes
- High-speed signal routing on internal ground referenced layers
- No high-speed signal return currents passed thru coupling capacitors
- Option for EMI ring on module perimeter

Routing Guidelines

Proper signal routing is critical to a successful carrier board design. The Catalyst XL supports high-speed differential and single-ended signals that require strict routing constraints.

Use the following recommendations to route high-speed signals:

- Ground references
- Continuous reference planes
- Matched lengths
- Bend minimization
- Layer-to-layer connection reduction

The following are the high-speed differential pairs that require strict routing constraints on a carrier board:

- **PCIe**
The PCIe x1 lane consists of differential signal pairs for transmit, receive, and reference clock. The module includes AC coupling capacitors on the transmit pair. Include AC coupling capacitors on the receive pair driven from the carrier board to the Catalyst XL. The recommended coupling capacitor is a 0.1 μ F surface mount 0402 discrete capacitor of type X7R/X5R. Place the 0.1 μ F capacitors near the PCIe device on the carrier board.
- **USB**
These signal pairs can be routed to USB sockets for external connections or directly to USB devices on the carrier board. Include an EMI choke between connector J1 and the USB connector when driving a USB cable. Applications with USB devices hardwired on-board do not require an EMI choke.
- **LVDS display**
The LVDS display output includes four LVDS data pairs and a LVDS pixel clock.
- **SDVO**
The SDVO consists of seven high-speed differential signal pairs.

The following are the high-speed single-ended signals that require strict routing constraints on a carrier board:

- IDE/PATA interface
- HD Audio
- SD/MMC
- LPC bus

For additional signal routing details, refer to the *Catalyst XL Carrier Board Routing Guidelines* (Eurotech document #110122-2004).

Power Planes

The following voltages are inputs to the module on [J2](#), page [56](#). These nets should be power planes on your carrier board:

- V3.3
- V3.3A
- V3.3S
- V5A
- V5S

Be sure to include sufficient bulk decoupling and local decoupling on each plane.

Requirements and Recommendations

The previous sections provided details about the various features of the Catalyst XL including design requirements and design recommendations. This section summarizes these design guidelines and provides a checklist for custom carrier board design.

Required Circuitry

The following table lists circuitry required on the carrier board.

Name	Pin	Carrier Board Design Requirement
FP_RESET#	J1 A59	Include momentary button
PWR_BUTTON#	J1 B59	Include momentary button
USB_CLIENT	J1 B53	Include 4.7k Ω pull-up resistor to 3.3 V (when USB2 is configured as a USB client)
PCIE1_PER+	J1 B95	Include 0.1 μ F AC coupling capacitors
PCIE1_PER-	J1 B94	
PCIE2_PER+	J1 A95	Include 0.1 μ F AC coupling capacitors
PCIE2_PER-	J1 A94	
SDVO_CLK+	J1 B91	Include 0.1 μ F AC coupling capacitors. Place near Catalyst XL connector J1.
SDVO_CLK-	J1 B92	
I2C_SDA	J1 B108	Include 10k Ω pull-ups to V3.3A
I2C_SCL	J1 B109	
SMC_UART_RX	J1 B57	Include access to these nets using test points or connector to aid in carrier board bring up. Include a 10k Ω pull-up to V3.3A to SMC_UART_RX.
SMC_UART_TX	J1 B106	
L_DDC_CLK	J1 A29	Include 2.2k Ω pull-ups to V3.3S
L_DDC_DATA	J1 B28	
V_BATTERY	J2 4	Include 3 V battery

Recommended Circuitry

The following table lists recommendations for circuitry on the carrier board.

Name	J1 Pin	Carrier Board Design Recommendation
TDO	A106	Include 10k Ω pull-up to V3.3S
CLK_LPC_FWH	A36	Include no more than one load
CLK_LPC_SIO	B37	Connect to legacy IO controller if required
SDVO_CTLCLK	B30	Include 3.3k Ω pull-ups to 2.5V
SDVO_CTLDATA	A30	
LPC_AD3	B38	Include 10k Ω pull-ups to V3.3S
LPC_AD2	B34	
LPC_AD1	B39	
LPC_AD0	B36	
RESET#	B56	Buffer for signal drive strength
L_BKLTEN	B32	Include a 100k Ω pull down
L_CTLA_CLK	B29	Include 4.7k Ω pull-ups to V3.3S
L_CTLB_DATA	B25	
L_VDDEN	A32	Include a 100k Ω pull down

Name	J1 Pin	Carrier Board Design Recommendation
SD0_WP	B12	Include 10k Ω pull-ups to V3.3S
SD1_WP	B16	
SD2_WP	B27	
USB0+	A71	Include an EMI choke between connector J1 and the USB connector
USB0-	A72	
USB1+	B71	Include an EMI choke between connector J1 and the USB connector
USB1-	B72	
USB2+	A68	Include an EMI choke between connector J1 and the USB connector
USB2-	A69	
USB3+	B67	Include an EMI choke between connector J1 and the USB connector
USB3-	B68	
USB4+	A65	Include an EMI choke between connector J1 and the USB connector
USB4-	A66	
USB5+	B64	Include an EMI choke between connector J1 and the USB connector
USB5-	B65	
USB6+	A62	Include an EMI choke between connector J1 and the USB connector
USB6-	A63	
USB7+	B61	Include an EMI choke between connector J1 and the USB connector
USB7-	B62	

Test and Debug

The maintenance serial port is extremely important in bring-up of a new carrier board design. Eurotech highly recommends including an external connection to SMC_UART_RX (J1 B57) and SMC_UART_TX (J1 B106) on your carrier board.

The IEEE1149.1 JTAG port, provided on connector J1, is available for programming the CPLD on the module, factory test, and software debugging. Otherwise, this port is not supported for application use. Eurotech highly recommends including an external connection to this JTAG port on your carrier board. To ensure correct operation of the JTAG interface, include a 10k Ω pull-up resistor to V3.3S on the TDO signal on the carrier board.

An additional ITP debug port, connector J3, provides full access to the XDP debugger port using a SFF style connector. Eurotech highly recommends allowing for access to this connector, in the event you are directed to use this port when working with Eurotech staff. Allow for the size of the mating connector and bend radius of the cable.

Connectors

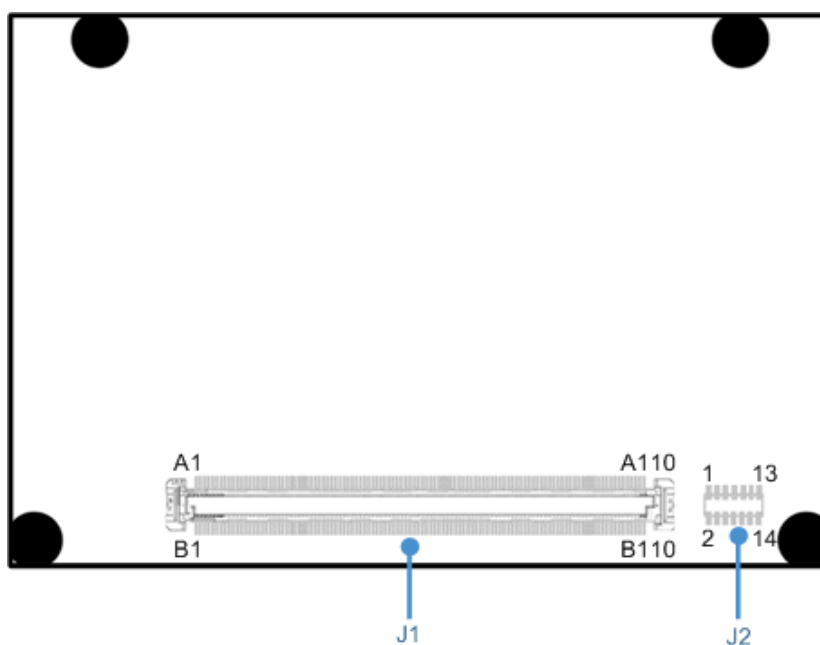
Identifying Connectors

The following diagrams illustrate the location and numbering of the connectors on the Catalyst XL. When viewing the module from the component side, connector J1 and connector J2 lie under the module.

The first diagram illustrates the top view of the module.



The second diagram illustrates the bottom view of the module.



Signal Headers

The following tables describe the electrical signals available on the connectors of the module. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions, and references to related sections.

J1: Docking Connector: Data

Board connector: 220-pin, stacking board-to-board receptacle, 0.5 mm, Tyco Electronics 3-6318490-6

Carrier board connector: Tyco Electronics 3-1827253-6, 5 mm stacking height
Tyco Electronics 3-6318491-6, 8 mm stacking height

The Catalyst XL connector J1 mates to the carrier board. Most data signals are provided on this docking connector.

Pin	Name	Type	On Module Termination	Description
A1	GND	P		Ground
A2	FWH_WP#	O-CMOS		External BIOS option write protect
A3	GPIO2	IO-CMOS		GPIO
A4	HDA_SYNC	O-HDA		Intel HD Audio
A5	HDA_RST#	O- HDA		
A6	HDA_SDI0	I- HDA		
A7	HDA_SDI1	I- HDA		
A8	reserved			
A9	SD0_DATA3	IO-LVTTL	R 48Ω	SD/MMC0
A10	SD0_DATA1	IO-LVTTL	R 48Ω	
A11	GND	P		Ground
A12	SD0_LED	O-LVTTL		SD/MMC0
A13	SD0_CLK	O-LVTTL	R 48Ω	
A14	SD1_DATA1	IO-LVTTL	R 48Ω	SD/MMC1
A15	reserved			
A16	SD0_PWR#	O-LVTTL		SD/MMC0
A17	SD1_PWR#	O-LVTTL		
A18	SD1_LED	O-LVTTL		SD/MMC1
A19	SD1_CLK	O-LVTTL	R 48Ω	
A20	SD1_CD#	I-LVTTL	PU 10kΩ V3.3S	
A21	GND	P		Ground

Pin	Name	Type	On Module Termination	Description
A22	SD2_DATA3	IO-LVTTL	R 48Ω	SD/MMC2
A23	SD2_DATA5	IO-LVTTL	R 48Ω	
A24	SD2_LED	O-LVTTL		
A25	SD2_DATA7	IO-LVTTL	R 48Ω	
A26	SD2_DATA1	IO-LVTTL	R 48Ω	
A27	SD2_DATA6	IO-LVTTL	R 48Ω	
A28	SD2_CLK	O-LVTTL	R 48Ω	
A29	L_DDC_CLK	O-LVTTL		
A30	SDVO_CTLDATA	IO		SDVO DDC I ² C
A31	GND	P		Ground
A32	L_VDDEN	O-LVTTL		LCD power enable
A33	SMB_ALERT#	I-LVTTL	PU 10kΩ V3.3S	SMBus activity alert
A34	HDA_SPKR	O-HDA		Intel HD Audio
A35	LPC_CLKRUN#	IO-LVTTL	PU 8.25kΩ V3.3S	LPC bus
A36	CLK_LPC_FWH	O-LVTTL	R 22Ω	LPC bus clock or external BIOS option clock
A37	IDE_DIOW#	O-LVTTL		IDE/PATA interface
A38	SMB_CLK	O-LVTTL	PU 2.2kΩ V3.3S	SMBus clock
A39	LPC_SERIRQ	IO-LVTTL	PU 10kΩ V3.3S	LPC bus
A40	LPC_FRAME#	O-LVTTL		
A41	GND	P		Ground
A42	IDE_A0	O-LVTTL		IDE/PATA interface
A43	IDE_DATA0	IO-IDE		
A44	IDE_DATA3	IO-IDE		
A45	IDE_DATA9	IO-IDE		
A46	IDE_A2	O-LVTTL		
A47	IDE_DATA5	IO-IDE		
A48	IDE_DATA6	IO-IDE		
A49	IDE_DATA1	IO-IDE		
A50	IDE_IOR#	O-LVTTL		
A51	GND	P		
A52	IDE_DATA2	IO-IDE		IDE/PATA interface
A53	IDE_IRQ	I-LVTTL	PU 10kΩ V3.3S	
A54	IDE_IORDY	I-LVTTL	PU 4.7kΩ V3.3S	
A55	IDE_CS1#	O-LVTTL		
A56	IDE_CS3#	O-LVTTL		

Pin	Name	Type	On Module Termination	Description
A57	HDA_DOCK_EN#	O-HDA		Intel HD Audio
A58	HDA_DOCK_RST#	O-HDA		
A59	FP_RESET#	I-3.3	PU 10k Ω V3.3S	Front panel reset
A60	GND	P		Ground
A61	USB_OC5#	I-LVTTL	PU 10k Ω V3.3	USB5 over current
A62	USB6+	IO		USB6 (high speed only)
A63	USB6-			
A64	GND	P		Ground
A65	USB4+	IO		USB4
A66	USB4-			
A67	GND	P		Ground
A68	USB2+	IO		USB2
A69	USB2-			
A70	GND	P		Ground
A71	USB0+	IO		USB0
A72	USB0-			
A73	GND	P		Ground
A74	LVDS_CLK+	O-LVDS		LVDS clock
A75	LVDS_CLK_			
A76	GND	P		Ground
A77	LVDS_DATA2+	O-LVDS		LVDS data 2
A78	LVDS_DATA2-			
A79	USB_OC2#	I-LVTTL	PU 10k Ω V3.3	USB2 over current
A80	GND	P		Ground
A81	LVDS_DATA1+	O-LVDS		LVDS data 1
A82	LVDS_DATA1-			
A83	GND	P		Ground
A84	SDVO_STALL+	I		SDVO signal allowing external device to stall the display pipeline
A85	SDVO_STALL-			
A86	GND	P		Ground
A87	SDVO_BLUE+	O	C 0.1 μ F	SDVO data
A88	SDVO_BLUE-			
A89	USB_OC3#	I-LVTTL	PU 10k Ω V3.3	USB3 over current
A90	GND	P		Ground

Pin	Name	Type	On Module Termination	Description
A91	SDVO_INT+	I		SDVO interrupt
A92	SDVO_INT-			
A93	GND	P		Ground
A94	PCIE2_PER+	I-PCIe		PCIe2 receive pair
A95	PCIE2_PER-			
A96	GND	P		Ground
A97	PCIE1_CLKREQ#	I-3.3	R 475Ω PU 10kΩ V3.3S	PCIe1 clock enable
A98	PCIE1_PET-	O-PCIe	C 0.1μF	PCIe1 transmit pair
A99	PCIE1_PET+			
A100	GND	P		Ground
A101	PCIE1_REFCLK+	O-HCSL		PCIe1 clock
A102	PCIE1_REFCLK-			
A103	GND	P		Ground
A104	TMS	O	PU 10kΩ V3.3S	JTAG
A105	TCK	I	PD 1kΩ	
A106	TDO	O		
A107	TDI	I	PU 10kΩ V3.3S	
A108	GPIO1	IO-CMOS		GPIO
A109	THERM_ALERT	IO-3.3	PU 10kΩ V3.3S	(See System Management , page 27.)
A110	GND	P		Ground
B1	GND	P		Ground
B2	LPCPD#	O-3.3		In-process system power state change indicator
B3	H_INIT#	I-LVCMOS	PU 1kΩ V1.05S	Soft reset for host processor
B4	HDA_CLK	O-HDA		Intel HD Audio
B5	HDA_SDO	O-HDA		
B6	SD0_CMD	IO-LVTTL	R 48Ω PU 40kΩ V3.3S	SD/MMC0
B7	SD0_DATA0	IO-LVTTL	R 48Ω	
B8	reserved			
B9	reserved			
B10	SD0_DATA2	IO-LVTTL	R 48Ω	SD/MMC0
B11	GND	P		Ground
B12	SD0_WP	I-LVTTL		SD/MMC0
B13	SD0_CD#	I-LVTTL	PU 10kΩ V3.3S	

Pin	Name	Type	On Module Termination	Description
B14	SD2_PWR#	O-LVTTL		SD/MMC2
B15	SD1_CMD	IO-LVTTL	R 48Ω PU 40kΩ V3.3S	SD/MMC1
B16	SD1_WP	I-LVTTL		
B17	SD1_DATA2	IO-LVTTL	R 48Ω	
B18	SD1_DATA0	IO-LVTTL	R 48Ω	
B19	SD1_DATA3	IO-LVTTL	R 48Ω	
B20	SD2_DATA0	IO-LVTTL	R 48Ω	SD/MMC2
B21	GND	P		Ground
B22	SD2_CD#	I-LVTTL	PU 10kΩ V3.3S	SD/MMC2
B23	SD2_DATA4	IO-LVTTL	R 48Ω	
B24	SD2_CMD	I-LVTTL	R 48Ω PU 40kΩ V3.3S	
B25	L_CTLB_DATA	IO-LVTTL		Backlight I ² C data
B26	SD2_DATA2	IO-LVTTL	R 48Ω	SD/MMC2
B27	SD2_WP	I-LVTTL		
B28	L_DDC_DATA	IO-LVTTL		LCD DDC I ² C
B29	L_CTLA_CLK	O-LVTTL		Backlight I ² C clock
B30	SDVO_CTLCLK	O		SDVO DDC I ² C
B31	GND	P		Ground
B32	L_BKLTEN	O		Turns power to the backlight on or off
B33	L_BKLTCTL	O-PWM		Controls intensity of the backlight
B34	LPC_AD2	IO-LVTTL	PU 10kΩ V3.3S	LPC bus
B35	SMB_DATA	IO-LVTTL	PU 2.2kΩ V3.3S	SMBus
B36	LPC_AD0	IO-LVTTL	PU 10kΩ V3.3S	LPC bus
B37	CLK_LPC_SIO	O-LVTTL	R 22Ω	
B38	LPC_AD3	IO-LVTTL	PU 10kΩ V3.3S	
B39	LPC_AD1	IO-LVTTL	PU 10kΩ V3.3S	
B40	IDE_DATA7	IO-IDE		IDE/PATA interface
B41	GND	P		Ground

Pin	Name	Type	On Module Termination	Description
B42	IDE_DATA11	IO-IDE		IDE/PATA interface
B43	IDE_DATA15	IO-IDE		
B44	IDE_DATA8	IO-IDE		
B45	IDE_DATA13	IO-IDE		
B46	IDE_DATA12	IO-IDE		
B47	IDE_DREQ	IO-LVTTL		
B48	IDE_DATA14	IO-IDE		
B49	IDE_DATA10	IO-IDE		
B50	IDE_DATA4	IO-IDE		
B51	GND	P		
B52	IDE_A1	O-LVTTL		IDE/PATA interface
B53	USB_CLIENT	I-CMOS		USB2 client detection
B54	IDE_ACK#	O-LVTTL		IDE/PATA interface
B55	PCIE_WAKE#	I-LVTTL	PU 1k Ω V3.3	Standard I/O device wake event signal
B56	RESET#	O-3.3	PU 10k Ω V3.3S	System reset
B57	SMC_UART_RX	I-3.3		Maintenance port
B58	L_BKLTSEL	O		Selects backlight control (PWM vs. I ² C)
B59	PWR_BUTTON#	I-5	PU 10k Ω V5A	Power button input
B60	GND	P		Ground
B61	USB7+	IO		USB7 (high speed only)
B62	USB7-			
B63	GND	P		Ground
B64	USB5+	IO		USB5
B65	USB5-			
B66	GND			Ground
B67	USB3+	IO		USB3
B68	USB3-			
B69	USB_OC0#	I-LVTTL	PU 10k Ω V3.3	USB0 over current
B70	GND			Ground
B71	USB1+	IO		USB1
B72	USB1-			
B73	GND			Ground
B74	LVDS_DATA3+	O-LVDS		LVDS data 3
B75	LVDS_DATA3-			

Pin	Name	Type	On Module Termination	Description
B76	GND			Ground
B77	LVDS_DATA0+	O-LVDS		LVDS data 0
B78	LVDS_DATA0-			
B79	USB_OC4#	I-LVTTL	PU 10k Ω V3.3	USB4 over current
B80	GND	P		Ground
B81	SDVO_RED+	O	C 0.1 μ F	SDVO data
B82	SDVO_RED-			
B83	GND	P		Ground
B84	SDVO_TVCLKIN+	I	C 0.1 μ F	SDVO external frequency reference
B85	SDVO_TVCLKIN-			
B86	GND	P		Ground
B87	SDVO_GREEN+	O	C 0.1 μ F	SDVO data
B88	SDVO_GREEN-			
B89	USB_OC1#	I-LVTTL	PU 10k Ω V3.3	USB1 over current
B90	GND	P		Ground
B91	SDVO_CLK+	O		SDVO clock reference
B92	SDVO_CLK-			
B93	GND	P		Ground
B94	PCIE1_PER-	I-PCle		PCle1 receive pair
B95	PCIE1_PER+			
B96	GND			Ground
B97	PCIE2_CLKREQ#	I-3.3	R 475 Ω PU 10k Ω V3.3S	PCle2 clock enable
B98	PCIE2_PET-	O-PCle	C 0.1 μ F	PCle2 transmit pair
B99	PCIE2_PET+			
B100	GND	P		Ground
B101	PCIE2_REFCLK+	O-HCSL		PCle2 clock
B102	PCIE2_REFCLK-			
B103	GND	P		Ground
B104	PM_EN_S0#	O-3.3	PU 10k Ω V3.3A	Power state indicator
B105	PM_EN_PWR	O-3.3	PD 100k Ω	
B106	SMC_UART_TX	O-3.3		Maintenance port
B107	PM_EN_S3#	O-3.3	PU 10k Ω V3.3A	Power state indicator
B108	I2C_SDA	OD		I ² C bus
B109	I2C_SCL	OD		
B110	GND	P		Ground

J2: Docking Connector: Power

Board connector: 2x7 socket, 1 mm, Samtec CLM-107-02-LM-D

Carrier board connector: Samtec MW-07-03-G-D-095-085, 5 mm stacking height
Samtec MW-07-03-G-D-226-065, 8 mm stacking height

The Catalyst XL receives the power input and controls for interfacing with an external power supply on this docking connector. See [Power Requirements](#), page 28 for a description of the Catalyst XL power supply.

Pin	Name	Type	On Module Termination	Description
1	V3.3	PI		3.3 V primary supply voltage
2	PM_CARRIER_PWRGD	I-3.3	PU 10k Ω V3.3A	Indicator for input power voltages
3	V3.3	PI		3.3 V primary supply voltage
4	V_BATTERY	PI		RTC backup power
5	V3.3	PI		3.3 V primary supply voltage
6	V5A	PI		5 V “always” power
7	V5S	PI		5 V normal operating power
8	V3.3A	PI		3.3 V “always” power
9	V5S	PI		5 V normal operating power
10	GND	P		Ground
11	V3.3S	PI		3.3 V normal operating power
12	GND	P		Ground
13	V3.3S	PI		3.3 V normal operating power
14	GND	P		Ground



Important! Disconnect the power input before removing the Catalyst XL. Removing the module from a powered carrier board may result in damage to both the carrier board and to the module.

J3: ITP Debug Port

Board connector: 24-pin FFC/FPC connector, 0.5 mm, Molex 52435-2472

Connector J3 provides an In-Target Probe (ITP) debug port for the Catalyst XL. See [Test and Debug](#), page 47 for additional details about this debug port.

Pin	Name	Type	Description
1	XDP_BPM5#	O	
2	XDP_BPM4#	O	
3	GND	P	
4	XDP_BPM3#	O	
5	XDP_BPM2#	O	
6	GND	P	
7	XDP_BPM1#	O	
8	XDP_BPM0#	O	
9	GND	P	
10	XDP_H_PWRGD	O	
11	XDP_SLPIOVR#	O	
12	CLK_XDP	O	ITP debug port
13	CLK_XDP#	O	
14	V1.05S	PO	
15	XDP_H_CPURST#	O	
16	XDP_DBRESET	I	
17	GND	P	
18	XDP_TDO	O	
19	XDP_TRST#	I	
20	XDP_TDI	I	
21	XDP_TMS	I	
22	XDP_TCK1	I	
23	GND	P	
24	XDP_TCK	I	

System Specifications

Performance

The Catalyst XL is available in various versions based on processor speed, on-module DRAM, and operating temperature. The following table specifies the processor performance.

Parameter	Min	Typ.	Max	Units
Processor operating frequency (note 2)			1.6	GHz
Processor operating frequency (note 3)	1.1		1.33	GHz
Front side bus clock	400		533	MHz
Front side bus width		64		bit

Notes:

- Specifications are for the module operating at commercial temperatures (0°C to 70°C).
- Specifications are for the module operating at industrial temperatures (-40°C to +85°C).

Power

This section includes power specifications for the Catalyst XL.

Power Consumption

Using ACPI functionality, the Catalyst XL supports multiple modes of power saving operation. Although power consumption varies based on the level of processor activity and peripheral connections, values can be estimated for typical applications.

The following table lists power consumption estimates.

Power Mode	Parameter	Min	Typ.	Max	Units
S0	Full operation		2	5	W
S3	Sleep			500	mW
S4	Hibernate			10	mW
S5	Power down			10	mW

Notes: Estimates given are expected values based upon typical applications.

Power Supply

The Catalyst XL requires the power inputs and control signals listed in the following table. See [Power Supply Architecture](#), page 29 for a description of the power supply.

Absolute Maximum Ratings

Input supply voltages 3.465 V, 5.25 V

Symbol	Parameter	Min	Typ.	Max	Units
System Power Inputs (note 4)					
V3.3	Primary supply voltage	3.135	3.3	3.465	V
I _{V3.3}			0.9	1.9	A
V3.3A	“Always” power (note 5)	3.135	3.3	3.465	V
I _{V3.3A}			0.025	0.10	A
V3.3S	Normal operating power	3.135	3.3	3.465	V
I _{V3.3S}			0.13	1.0	A
V5A	“Always” power	4.75	5.0	5.25	V
I _{V5A}			0.0008	0.20	A
V5S	Normal operating power	4.75	5.0	5.25	V
I _{V5S}			0.1	0.4	A
V_BATTERY	RTC backup power (note 6)	2.4	3.3	3.5	V
I _{V_BATTERY}				10	μA
PM_CARRIER_PWRGD (note 7)					
V _{IH}	High-level input voltage	2.0	3.3		V
V _{IL}	Low-level input voltage			0.8	V
R _{PU}	Pull-up resistance (note 8)		10		kΩ
V _{PU}				3.3	V
PWR_BUTTON#					
V _{IH}	High-level input voltage	2.5	5		V
V _{IL}	Low-level input voltage			1.0	V
R _{PU}	Pull-up resistance (note 9)		10		kΩ
V _{PU}				5	V
PM_EN_PWR					
V _{OH}	High-level output voltage	2.5	3.3		V
V _{OL}	Low-level output voltage			0.2	V

Notes:

- The maximum currents per voltage rail include peak currents and are not indicative of aggregate power consumption during normal system operation.
- If V3.3A goes below 3.08V, the embedded controller will reset and a reset header will be displayed on the maintenance port. The reset of embedded controller results in a complete restart of module circuitry including all on-module power regulation, resets, and interface power sequence signals.
- V_BATTERY has 1 μF of bulk decoupling capacitance, load side of diode.
- For detailed timing requirements, see [Power State Signals](#), page 32.
- PM_CARRIER_PWRGD includes a pull-up resistor to V3.3A.
- BTN_ONOFF# includes a pull-up resistor to V5A.

Electrical

This section provides electrical specifications for the Catalyst XL. For details about termination of individual signals, see the signal connectors in [Signal Headers](#), page 49.

Reset Circuitry

The Catalyst XL includes three reset signals. See [Reset Signals](#), page 26 for a description of these signals.

Symbol	Parameter	Min	Typ.	Max	Units
RESET# (note 10)					
V_{OH}	High-level output voltage $I_{OH} = -4 \text{ mA}$, $V_{DD}=3.3 \text{ V}$	$V_{CC}-0.4$	3.3		V
V_{OL}	Low-level output voltage $I_{OL} = 4 \text{ mA}$, $V_{DD}=3.3 \text{ V}$			0.4	V
FP_RESET# (note 11)					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
R_{PU}	Pull-up resistance		10		k Ω
V_{PU}				3.3	V
H_INIT# (note 12)					

Notes:

- Specifications per the NXP LPC2132 Product Datasheet, Rev. 04 – 16 October 2007, www.nxp.com.
- The module includes debounce circuitry and a pull-up resistor to V3.3S. FP_RESET# will not be detected until after RST# is de-asserted.
- H_INIT# is a 1.05 V CMOS signal.

Intel High Definition Audio

The Intel SCH US15W supports the Intel HD Audio specification. Standard modules operate at 3.3 V signaling levels. A 1.5 V version is available as a volume production option. See [Intel High Definition Audio](#), page 28 for a description of the audio interface.

Symbol	Parameter	Min	Typ.	Max	Units
HDA (note 13)					
V_{CC}	Supply voltage at 3.3 V signaling levels		3.3		V
V_{IH}	High-level input voltage	$0.65 V_{CC}$			V
V_{IL}	Low-level input voltage			$0.35 V_{CC}$	V
V_{OH}	High-level output voltage $I_{OH} = -500 \mu\text{A}$	$0.9 V_{CC}$			V
V_{OL}	Low-level output voltage $I_{OL} = 1500 \mu\text{A}$			$0.10 V_{CC}$	V
F_{HDA_SDIx}	Data rate		24		Mbps

Notes:

- Specifications per the Intel High Definition Audio Specification Revision 1.0.

Embedded Controller

The embedded controller provides an external I²C bus, a maintenance port, and multiple discrete I/O signals including LPCPD#, THERM_ALERT, GPIO, and PM_EN_Sx#.

Symbol	Parameter	Min	Typ.	Max	Units
LPCPD# (note 14)					
V _{OH}	High-level output voltage I _{OH} = -4 mA, V _{CC} = 3.3 V	2.4			V
V _{OL}	Low-level output voltage I _{OL} = 4 mA, V _{CC} = 3.3 V			0.45	V
THERM_ALERT (note 14)					
V _{IH}	High-level input voltage	1.7	3.3		V
V _{IL}	Low-level input voltage			0.8	V
R _{PU}	Pull-up resistance		10		kΩ
V _{PU}				3.3	V
GPIO1, GPIO2 (note 14)					
V _{IH}	High-level input voltage	1.7	3.3		V
V _{IL}	Low-level input voltage			0.8	V
V _{OH}	High-level output voltage I _{OH} = -0.1 mA, V _{CC} = 3.3 V	V _{CC} -0.2			V
V _{OL}	Low-level output voltage I _{OL} = 0.1 mA, V _{CC} = 3.3 V			0.2	V
PM_EN_S0#, PM_EN_S3# (note 15)					
V _{OH}	High-level output voltage I _{OH} = -4 mA, V _{DD} =3.3 V	V _{CC} -0.4	3.3		V
V _{OL}	Low-level output voltage I _{OL} = 4 mA, V _{DD} =3.3 V			0.4	V

Notes:

- Specifications per the Altera MAX II Device Handbook, August 2009 (MII5V1-3.3), www.altera.com.
- Specifications per the NXP LPC2132 Product Datasheet, Rev. 04 – 16 October 2007, www.nxp.com.

Clock Generator

The Catalyst XL provides two PCIe x1 buses with an on-module clock generator supplying the PCIe clock for each bus. Two additional input signals, PCIe_CLKREQ#, individually control each reference clock. See [PCI Express](#), page 21 for a description of the PCIe connectivity on the Catalyst XL.

Symbol	Parameter	Min	Typ.	Max	Units
PCIEX_REFCLK (note 16)					
F _{PCIEX_REFCLK}	Frequency		100		MHz
V _{OH}	High-level output voltage	600	700	850	mV
V _{OL}	Low-level output voltage	-150	0	27	mV
PCIEX_CLKREQ#					
V _{IH}	High-level input voltage	2.0	3.3	3.6	V
V _{IL}	Low-level input voltage	-0.3		0.8	V
R _{PU}	Pull-up resistance (note 17)		10		kΩ
V _{PU}				3.3	V
R _S	Series resistance		475		Ω

Notes:

16. PCIe1_REFCLK and PCIe2_REFCLK are HCSL outputs.
17. PCIe1_CLKREQ# and PCIe2_CLKREQ# include pull-up resistors to V3.3S

General

This section provides general specifications for the Catalyst XL.

Crystal Frequencies

Agencies certifying the Catalyst XL for compliance for radio-frequency emissions typically need to know the frequencies of on-board oscillators. The following table lists the frequencies of all crystals on the Catalyst XL.

Crystals	Device	Typ.	Units
X1	RTC	32.768	kHz
X2	Clock Generator	14.31818	MHz
X4	Embedded Controller	14.7456	MHz

Real-Time Clock

The Intel SCH US15W includes a RTC function that retains the system date and time. See [Non-Volatile Memory](#), page 19 for a description of the RTC function.

Parameter	Typ.	Units
Accuracy per month @ 25°C	+/-55	sec

Environmental

The Catalyst XL is designed to meet the environmental specifications listed in the following table. Note the local ambient temperature of the module is defined by the temperatures at three key thermal design interface contact points. Temperatures at these points must not exceed the maximum temperature specified. For additional information about the thermal interface of the Catalyst XL, see [Thermal Management](#), page 41.

Parameter	Min	Typ.	Max	Units
Commercial operating temperature	0		+70	°C
Industrial, extended operating temperature	-40		+85	°C
Storage temperature	-40		+85	°C
Relative humidity, non-condensing	5		95	%

Appendix A – Reference Information

Product Information

Product notices, updated drivers, support material:

www.eurotech.com

Intel

Information about the Intel Atom processor, Intel System Controller Hub US15W, Intel High Definition Audio specification, and LPC bus specification:

www.intel.com

Trusted Computing Group

Trusted Computer Group specification:

www.trustedcomputinggroup.org

USB

Universal Serial Bus specification:

www.usb.org

SDIO Card

SD Card Association and SDIO specification:

www.sdcard.org

MMC Card

MultimediaCard specification:

www.jedec.org

PCI SIG

PCI Express specification:

www.pcisig.com

I²C Bus

I²C bus specification:

www.nxp.com

SMBus

SMBus specification:

www.smbus.org

ACPI Specification

Information about the ACPI specification:

www.acpi.info

Appendix B – RoHS Compliance

EUROTECH

The Restriction of the use of certain Hazardous Substances (RoHS) Directive came into force on 1st July 2006. This product shall be designed using RoHS compliant components, and manufactured to comply with the RoHS Directive.

Eurotech has based its material content knowledge on a combination of information provided by third parties and auditing our suppliers and sub-contractor's operational activities and arrangements. This information is archived within the associated Technical Construction File. Eurotech has taken reasonable steps to provide representative and accurate information, though may not have conducted destructive testing or chemical analysis on incoming components and materials.

Additionally, packaging used by Eurotech for its products complies with the EU Directive 2004/12/EC in that the total concentration of the heavy metals cadmium, hexavalent chromium, lead and mercury do not exceed 100ppm.

Appendix C – Board Revision

This guide applies to the current revision of the module as given in the following section.

Identifying the Board Revision

The revision number is printed on the underside of the printed wiring board. That number is 170123-300Rx. The “x” indicates the revision level of the PWB.

Revision History

The following is an overview of the revisions to the Catalyst XL.

Revision 1

Initial release

Revision A

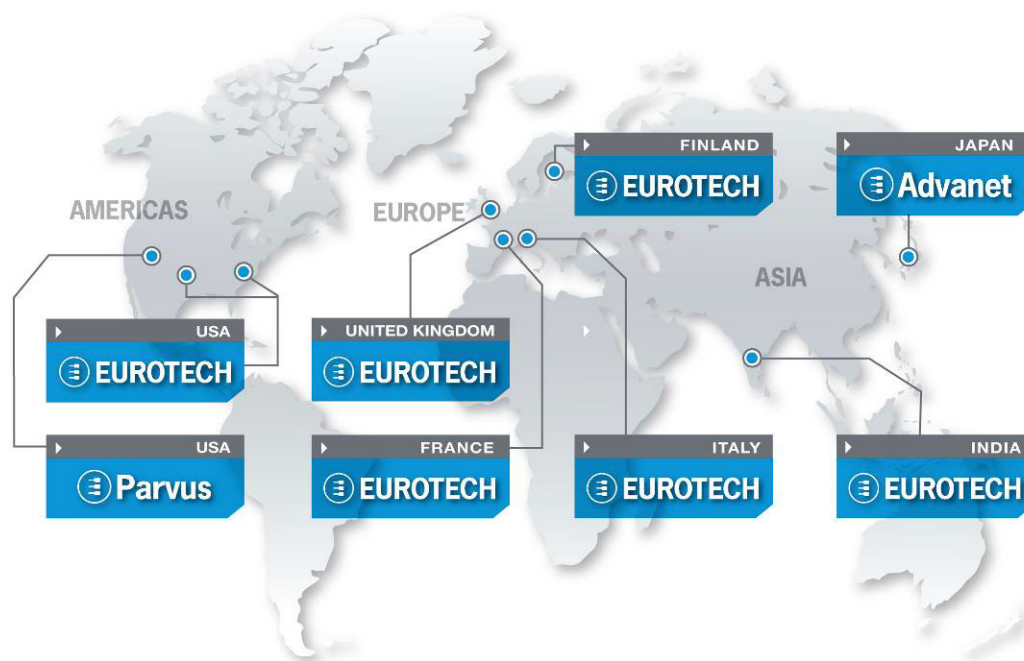
Implements routing changes to improve design margin

Adds jumper J10 for programming the embedded controller

Revision B

Removes TPM from the SMBus and adds it as an optional feature on the LPC bus

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