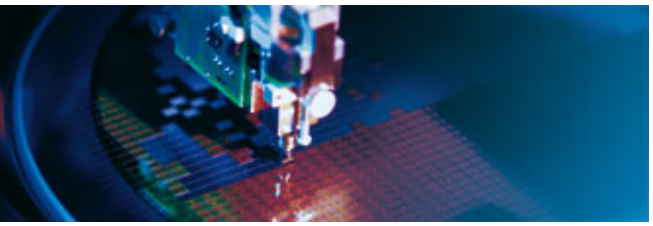
DESIGN-IN GUIDE



Catalyst LP

High Performance Module

Rev 5 – September 2011 – 110125-10005

www.eurotech.com

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Trademarks

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Document Revision History

REVISION	DESCRIPTION	DATE
3	Preliminary release	Aug 2010
4	Appendix D removed	Oct 2010
5	Initial release	Sept 2011

Table of Contents

Important User Information

In order to lower the risk of personal injury, electric shock, fire, or equipment damage, users must observe the following precautions as well as good technical judgment, whenever this product is installed or used.

All reasonable efforts have been made to ensure the accuracy of this document; however, Eurotech assumes no liability resulting from any error/omission in this document or from the use of the information contained herein.

Eurotech reserves the right to revise this document and to change its contents at any time without obligation to notify any person of such revision or changes.

Safety Notices and Warnings

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Eurotech assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Eurotech is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Installation in Enclosures

In the event that the product is placed within an enclosure, together with other heat generating equipment, ensure proper ventilation.

Do Not Operate in an Explosive Atmosphere

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Alerts that can be found throughout this manual

The following alerts are used within this manual and indicate potentially dangerous situations.

Danger, electrical shock hazard:
Information regarding potential electrical shock hazards:

- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Warning:
Information regarding potential hazards:

- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Information and/or Notes:
These will highlight important features or instructions that should be observed.

Use an Appropriate Power Supply

- Only start the product with a power supply that conforms to the voltage requirements as specified in Power Supply, page 45. In case of uncertainty about the required power supply, please contact your local Eurotech Technical Support Team.
- Use power supplies that are compliant with SELV regulation.
- Avoid overcharging power-points.

Antistatic Precautions

To avoid damage caused by ESD (Electro Static Discharge), always use appropriate antistatic precautions when handing any electronic equipment.

Life Support Policy

Eurotech products are not authorized for use as critical components in life support devices or systems without the express written approval of Eurotech.

Warranty

For Warranty terms and conditions users should contact their local Eurotech Sales Office.
See Eurotech Worldwide Presence, page 53 for full contact details.

WEEE

The information below is issued in compliance with the regulations as set out in the 2002/96/EC directive, subsequently superseded by 2003/108/EC. It refers to electrical and electronic equipment and the waste management of such products. When disposing of a device, including all of its components, subassemblies, and materials that are an integral part of the product, you should consider the WEEE directive.

This device is marketed after August 13, 2005 and you must separate all of its components when possible and dispose of them in accordance with local waste disposal legislations.

- Because of the substances present in the equipment, improper use or disposal of the refuse can cause damage to human health and to the environment.
- With reference to WEEE, it is compulsory not to dispose of the equipment with normal urban refuse and arrangements should be instigated for separate collection and disposal.
- Contact your local waste collection body for more detailed recycling information.
- In case of illicit disposal, sanctions will be levied on transgressors.

RoHS

This device, including all its components, subassemblies and the consumable materials that are an integral part of the product, has been manufactured in compliance with the European directive 2002/95/EC known as the RoHS directive (Restrictions on the use of certain Hazardous Substances). This directive targets the reduction of certain hazardous substances previously used in electrical and electronic equipment (EEE).

Technical Assistance

If you have any technical questions, cannot isolate a problem with your device, or have any enquiry about repair and returns policies, contact your local Eurotech Technical Support Team.

See Eurotech Worldwide Presence, page 53 for full contact details.

Transportation

When transporting any module or system, for any reason, it should be packed using anti-static material and placed in a sturdy box with enough packing material to adequately cushion it.

Warning:
Any product returned to Eurotech that is damaged due to inappropriate packaging will not be covered by the warranty.

Conventions

The following table describes the conventions for signal names used in this document.

Convention	Explanation
GND	Digital ground plane
#	Active low signal
+ or P	Positive signal in differential pair
- or N	Negative signal in differential pair

The following table describes the abbreviations for direction and electrical characteristics of a signal used in this document.

Type	Explanation
I	Signal is an input to the system
O	Signal is an output from the system
IO	Signal may be input or output
P	Power and ground
A	Analog signal
OD	Open-drain
CMOS	3.3 V CMOS
LVCMOS	1.05 V CMOS
LVTTL	Low Voltage TTL
3.3	3.3 V signal level
5	5 V signal level
IDE	5 V tolerant signal
HDA	High Definition Audio, 3.3 V signal
LVDS	Low Voltage Differential Signalling
PCIe	PCI Express signal
SATA	SATA differential signal
NC	No Connection
Reserved	Use is reserved to Eurotech

Some signals include termination on the Catalyst LP. The following table describes the abbreviations that specify the signal termination.

Termination	Explanation
PU	Pull-up resistor to the specified voltage
PD	Pull-down resistor
R	Series resistor
C	Series capacitor

Product Overview

The Catalyst LP is a high-performance module based on the Intel® Atom™ processor N450 (single core) or Intel® Atom™ processor D510 (dual core). It uses an integrated two-chip solution comprised of the Intel Atom processor and Intel® I/O Controller Hub (Intel® ICH8M). The Intel Atom processor contains an integrated 2D/3D graphics engine supporting hardware-accelerated graphics display and video processing capabilities, while the Intel ICH8M supports extensive I/O and data storage capabilities. The Catalyst LP maximizes the performance capabilities of the Intel Atom processor offering a feature-dense embedded solution.

An application-specific carrier board integrates with the Catalyst LP for a total production solution. This flexible, modular architecture enables easy customization and quick time-to-market. A Eurotech carrier board is available that implements several industry-standard interfaces allowing development across a broad spectrum of end-use applications.

The Catalyst LP is available with a variety of operating systems. Support is also available for the Java Virtual Machine and Eurotech's Everyware™ Software Framework, which offers an easy-to-use, Java-based development environment that minimizes time to market and allows for easy portability for future expansion.

Block Diagram

The following diagram illustrates the system organization of the Catalyst LP. Notice that the data connector has been divided into two sections for this illustration. Dotted lines indicate options.

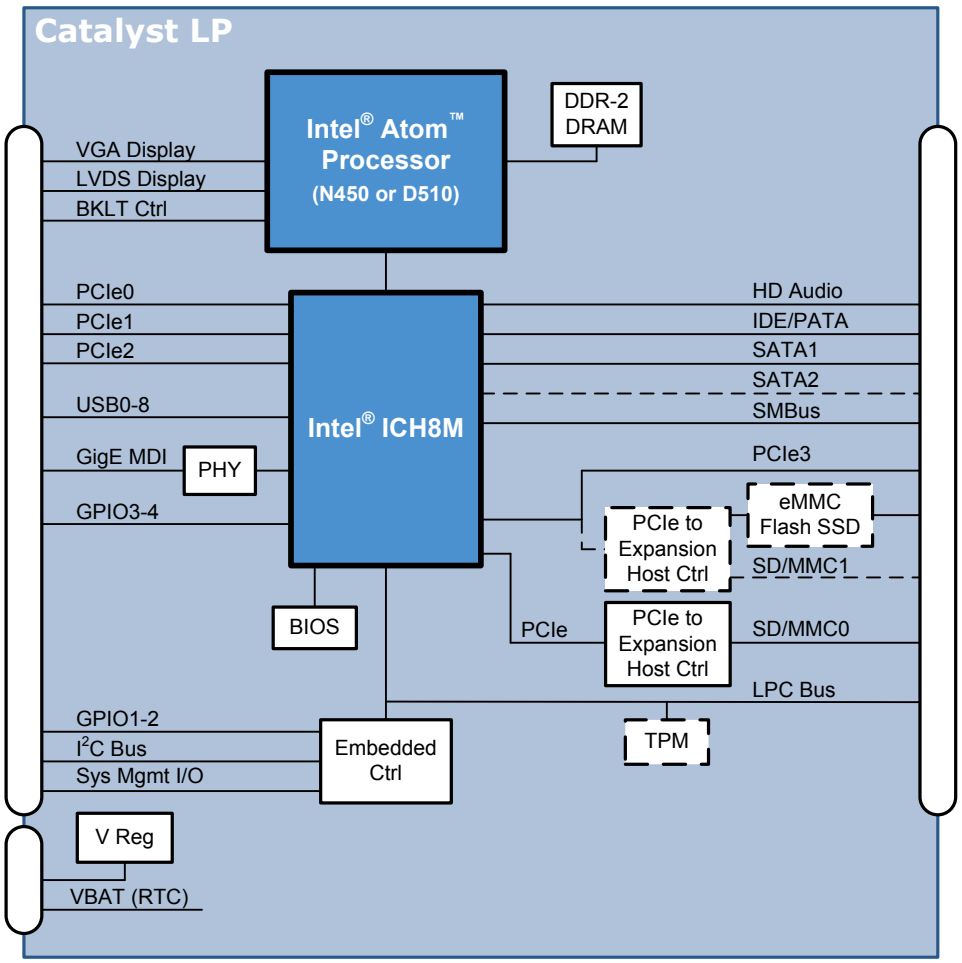


Figure 1. Catalyst LP Block Diagram

Features

Processor

- Intel® Atom™ processor N450 (single core) or Intel® Atom™ processor D510 (dual core)
- 200 MHz graphics engine (single core) or 400 MHz graphics engine (dual core)
- Intel® I/O Controller Hub (Intel® ICH8M)

Integrated System Functions

- Embedded Controller
- Optional Trusted Platform Management (Contact Eurotech for details)

Memory

- Up to 2 GB DDR-2 DRAM
- Optional on-board eMMC flash SSD (Contact Eurotech for details)
- Integrated system BIOS
- Battery-backed real-time clock
- External memory support
  - IDE/PATA disk drive
  - SATA disk drive
  - USB disk drive
  - SD/MMC card
  - PCI Express card

Communications

- Up to four PCI Express one lane slots
  - Custom configuration option for one PCI Express four lane slot
- Nine USB 2.0 ports operating at low, full, and high speeds
- Gigabit Ethernet with physical layer transceiver
- I^2C bus with I^2C master device
- System Management Bus

User Interface and Display

- Independent LVDS display output and VGA display output
- Backlight interface with control signals for intensity and power

Inputs and Outputs

- Low Pin Count bus for general-purpose I/O expansion
- Four general-purpose inputs and outputs

Audio Interface

- Intel® High Definition Audio supporting up to two external audio codecs

Power Supply

- 3.3 V and 5 V main power inputs
- ACPI power management

Mechanical

- 67 mm x 100 mm dimensions
- Less than 10 mm total stack height

Design Checklist

Eurotech provides a host of services to ensure that your product is up and running from the first prototype release. We recommend the following process for every Catalyst LP carrier board design:

Kickoff Stage

During the Kickoff Stage, you will develop your block diagram and identify any customizations your application may require.

☐ **Gather your reference materials**

Eurotech provides several documents that include key information for designing a custom carrier board. Use the following resources and ask questions:

- Catalyst LP Design-In Guide
- Catalyst LP Development Kit User Manual
- Carrier Board Routing Guidelines
- 3D CAD models
- Reference Carrier Board Schematic
- Reference Carrier Board Bill of Materials

☐ **Define your requirements**

Define your system's requirement. Be sure to include requirements such as the product features, the input power, the type of transient protection on the power supply, connectivity to the module, and all I/O to your system.

☐ **Create a block diagram**

Create a block diagram of your proposed design. This step helps to formulate the best way to connect different devices to the module.

☐ **Identify customizations**

Identify any customizations that your application requires. Examples of customizations are custom LCD panel timings and backlight control, custom module configurations, or supporting a device that is not included on Eurotech's standard carrier board. Customizations may require updates to the BIOS.

☐ **Utilize the Catalyst LP Development Kit**

Utilize the Catalyst LP Development Kit for validating your proposed design. For example, if a USB device is to be used on USB port 6, test that device by connecting it to USB port 6 on the Catalyst LP Development Kit. This testing also allows you to validate your OS image with all required drivers loaded.

☐ **Kickoff review**

Early in the development of your carrier board, meet with your Eurotech representative to review your block diagram and discuss customizations. Incorporate any changes into your design.

Preliminary Design Stage

During the Preliminary Design Stage, you will finalize your block diagram, agree on customizations, and begin your preliminary schematic.

☐ **Use the reference schematic**

Use Eurotech's reference carrier board schematic as a starting point for your design. This schematic includes many commonly used interfaces. Using the same connectivity to the module will minimize the time spent in debugging your design.

- **Select components from the reference bill of materials**

  Select the same components as those used in Eurotech's reference carrier board bill of materials. Eurotech selects components that are optimized for embedded systems based on quality, low-power consumption, availability, reliability, and industrial temperature options. Selecting the same components also allows you to use the drivers Eurotech has already integrated with the OS builds.

- **Follow the design requirements and recommendations**

  Follow the design requirements and recommendations listed in Carrier Board Design, page 35 of this design-in guide. This section provides details about circuitry to include on the carrier board.

- **Preliminary design review**

  Stay in contact with your Eurotech representative during your preliminary design. Together, finalize your block diagram and agree on customizations needed. Continue to ask questions as you move towards finalizing your design.

Critical Design Stage

During the Critical Design Stage, you will finalize your schematic making sure that you have met all the module's electrical, thermal, and mechanical design requirements.

- **Implement power supply sequencing**

  Implement the exact power supply sequencing described in Power State Signals, page 27 of this design-in guide. The module has very specific power-on sequence requirements in order to power-up and operate correctly. Power sequencing the multiple voltage rails, as described in this section, is CRITICAL. If your design does not meet these requirements, the module will not boot.

- **Provide a system-level reset**

  Buffer and use the system reset signal RST# (J1 B56), described in Reset Signals, page 23, to reset all devices on the carrier board. The embedded controller controls the de-assertion of this signal with appropriate timings relative to power being stable. Timing requirements for power stable to reset de-asserted and reset de-asserted to device available are critical.

- **Create a power budget**

  Create a power budget that takes into account the current requirement of the module, as specified in Power Supply, page 45, and of the devices that are used with the module. Design your power supply to handle the maximum current requirement.

- **Determine thermal management**

  Determine what type of thermal management is required for your design. Use your power budget and the information provided in Thermal Management, page 33 of this design-in guide to design a heat spreader, if necessary.

- **Follow the module's mechanical requirements**

  Follow the exact mechanical requirements given in Mechanical Design, page 31 for mounting holes placement, position of the board-to-board connectors, and stack height on your carrier board design.

- **Use advanced layout and high-speed routing techniques**

  Follow the design constraints and routing guidelines described in Carrier Board Design, page 35 of this design-in guide. Adhering to good design practices for high-speed PCB design is essential. You should have your schematic 95% complete, especially the high-speed signals and buses of the module, power sequencing, and system reset, before you start board layout. Meet with your Eurotech representative to review your schematic before you begin layout. After your layout is complete, meet again to review your complete design.

- **Have a strategy to debug your design**

  Review your strategy to bring-up and to debug your design. Ensure that you have included the necessary support in your design. The maintenance serial port is extremely important in bring-up of a new design. Eurotech highly recommends including an external connection to SMC_UART_RX (J1 B57) and SMC_UART_TX (J1 B106) on your carrier board.

- **Critical design review**

  Do an in-depth review of your finished design, including final schematic and board layout, to ensure that you have met all the requirements described in this checklist and throughout this design-in guide. Again, ask your Eurotech representative questions.

Prototype Bring-up Stage

Eurotech provides assistance in bringing-up your prototype at your site or ours. We have several tools that can assist the process including "stand-alone" BIOS releases, BIOS modifications to meet specific platform or test requirements, and power monitoring applications for the module. The "stand-alone" BIOS sets up the internal functions of the module and basic I/O functions. It is not dependent on any specific carrier board, devices, or circuits. This BIOS provides "basic" level functionality and can be used as a tool in the bring-up or debug of your unique carrier board.

- **Begin with the basics**

  Begin by checking basic functionality such as power, reset, and clocks. Verify that the power sequencing is as it should be and that the voltage regulator outputs are at nominal levels. Check that the system reset signal is asserted and deasserted according to the power sequencing requirements. Ensure all clocks necessary for bring-up are running properly.

- **Start with minimal devices**

  Minimize the number of devices required for bring-up. Using Eurotech's "debug" set of firmware is a good start. This firmware can be used (on case-by-case) basis as a debug and bring-up tool for your specific design prototyping or in the debugging phases of your development. It disables all NON-Critical-to-BOOT functions to simplify the system functionality to base level. After you have verified this base level, enable each subsystem as needed. Adding one device at a time will help determine which subsystem, if any, is having problems.

- **Utilize the maintenance port**

  Utilize the maintenance port output to identify problems during bring-up. This port provides important debug information including BIOS POST codes and error messages that enable you to monitor the operation of the module.

- **Use your Catalyst LP Development Kit**

  Use your Catalyst LP Development Kit to isolate problems. If a problem occurs during bring-up of your carrier board, try to duplicate the problem on the development kit.

- **Prototype bring-up review**

  Review your bring-up process and share lessons learned with your Eurotech representative.

Acceptance of Customizations

Eurotech is committed to your design success. Using our support services throughout the development cycle ensures a complete and robust solution with which to move forward.

- **Customization Acceptance**

  Meet with your Eurotech representative to discuss acceptance of any customizations and to plan the steps toward production of your Catalyst LP design.

Development Kit

The Catalyst LP Development Kit is designed to get the developer up and running quickly. The development kit includes the Catalyst LP, a standard development kit carrier board, and supporting peripheral devices. To provide flexibility and allow development across a broad spectrum of end-use applications, the carrier board maximizes the Catalyst LP functionality and implements many industry-standard interfaces. This configuration allows you to become familiar with the Catalyst LP functionality prior to customization for your specific application. In addition, the standard development kit carrier board provides a reference for custom carrier board design.

For a complete description of the Catalyst LP Development Kit, refer to the *Catalyst LP Development Kit User Manual (Eurotech document 110125-4000)*.

Related Documents

This guide provides details about the various features of the Catalyst LP and about how it creates a system that meets your application needs. It extends the information provided in the *Catalyst LP Development Kit User Manual* and is intended for hardware design engineers. Design details are provided as guidelines for custom carrier board design.

The following documents are also important resources for the Catalyst LP.

Document	
Catalyst XL - Catalyst LP Compatibility Technical Bulletin	110125-1001
Catalyst LP Development Kit User Manual	110125-4000
Catalyst LP Development Kit Quick Start	110125-4001
Catalyst Module Display Adapter User Manual	110122-4000
Catalyst Module Installation and Removal	110122-2014
Catalyst System Management Programmer Reference	110122-2021
Catalyst SMBus Programmer Reference	110122-2022
Catalyst I2C Bus Programmer Reference	110122-2023

Table 1. Related Documents

Check the Eurotech support site (http://support.eurotech-inc.com/) for errata reports and for the latest releases of these documents.

Software Specifications

Eurotech provides an application-ready platform including BIOS, operating system, and development environment. This section gives a brief description of the software support available for the Catalyst LP. For additional details, contact your local Eurotech representative.

Operating System Support

The Catalyst LP is compatible with the following operating systems:

- Windows® Embedded Standard
- Wind River Linux 3.0 (future option)
- Select real-time operating systems

For details about available support of each operating system, contact your local Eurotech representative.

BIOS

The Catalyst LP incorporates a custom system BIOS developed by Eurotech.

Software Development Kit

Eurotech has developed a Software Development Kit (SDK) and its Application Programming Interface (API) for the following functions:

- System Management
- SMBus
- I^2C bus

For details about the availability of these SDKs, contact your local Eurotech representative.

Everyware™ Software Framework

Everyware Software Framework (ESF) is an inclusive software framework that puts a middleware layer between the operating system and the OEM application. It provides industry-standard interfaces that shorten development time, simplify coding, and allow software to be ported from one Eurotech hardware platform to another. ESF is a future option for the Catalyst LP. If your application requires ESF, contact your local Eurotech representative.

Information about ESF is available at http://esf.eurotech.com.

Hardware Specifications

Core Processor

The Catalyst LP bases its architecture on an integrated two-chip solution comprised of the Intel Atom processor and Intel ICH8M. In addition, the Catalyst LP fully integrates system functions that include system management and control implemented by an advanced chip level solution, tightly integrated power management controls, system BIOS firmware memory, and optional Trusted Platform Management (TPM) for industry-standard secure data encryption. This fully integrated and flexible feature set increases product readiness and compliance. The following sections describe the functionality and feature set of this processor technology as it relates to the Catalyst LP architecture.

Intel Atom Processor

At the core of the Catalyst LP is the Intel Atom processor N450 (single core) or the Intel Atom processor D510 (dual core). This high-performance architecture offers dual or single core processing with hardware-accelerated 2D/3D graphics display and video processing capabilities.

External Interrupts

The Catalyst LP provides several sources for external interrupts capable of generating a processor interrupt when the system is in power state S0. The following table lists these interrupt signals.

Signal	J1 Pin	Description
GPIO1	A108	Embedded controller GPIO
GPIO2	A3	Embedded controller GPIO
SMB_ALERT#	A33	SMBus activity alert

Table 2. External Interrupts

For additional information about these signals, see General-Purpose Input and Output, page 23 and System Management Bus, page 20.

Intel I/O Controller Hub

The Intel Atom processor operates in conjunction with the Intel ICH8M. This companion device provides a wide range of capabilities that include PCIe, USB, SATA, Intel HD Audio support, IDE/PATA, SMBus, LPC bus, Ethernet, and a RTC function. Subsequent sections describe each capability.

Embedded Controller

An embedded controller included on the Catalyst LP performs two main functions: ACPI power management and hardware monitoring. It connects to the Intel ICH8M using the LPC bus.

Combined with the ICH8M and on-module power switch, the embedded controller supports ACPI power management. It functions, in conjunction with these devices, to control proper sequencing of voltages ensuring proper start-up, shutdown, and power saving transitions. For further details about power management, see Power Supply Architecture, page 25.

As a second function, the embedded controller provides hardware monitoring for voltage and temperature. Voltage monitoring measures the input power and on-module voltage regulators. Temperature monitoring measures temperatures on the Intel Atom processor die and near the memory chips. You can also monitor temperatures on your carrier board by connecting an external temperature sensor to the embedded controller I^2C bus provided on connector J1. For further details about the I^2C bus, see I^2C Bus, page 20.

In addition to the two main functions, the embedded controller performs extended functionality that includes optional battery management, device initialization, GPIO functions, wake event control, and customization for private SPI bus. For further details about the embedded controller's extended functionality, contact your local Eurotech representative.

Trusted Platform Management (option)

The optional on-module TPM function is compliant with the Trusted Computer Group specification version 1.2. This function provides public key generation, public key storage encryption/decryption, storage of hashes, key endorsement, and TPM initialization. As an option, the TPM is included on the LPC bus.

Memory

The Catalyst LP combined with a carrier board provides a variety of storage capabilities. The following sections describe the different types of memory supported and provide details about implementation.

Synchronous DRAM

Double Data Rate Synchronous DRAM (DDR-2) is used on the Catalyst LP for system main memory and frame buffer memory. Options up to 2 GB are available. The Intel Atom processor supports unified memory architecture in which the integrated 2D/3D graphics controller memory is "unified" with the system main memory. The default frame buffer is 4 MB with options in the BIOS Setup for selecting an 8 MB option. Extended graphics memory space is available up to 256 MB. The graphics driver controls this size based on usage.

Non-Volatile Memory

The Catalyst LP includes non-volatile memory for system BIOS storage and a real-time clock (RTC) functionality.

BIOS and Configuration Data

A serial interface flash memory device stores the BIOS boot firmware, BIOS Setup settings, and module configuration data on the Catalyst LP. Standard configuration is 2 MB. The flash device connects to the Intel ICH8M using a serial peripheral interface (SPI). This system BIOS memory supports pre-programmability at the device level, in-circuit programming on module, and updates using a run-time flash utility. In addition, programmable write protection is available using multiple flash sectors.

Real-Time Clock

The Intel ICH8M includes a RTC function. It retains the system date and time when the system is powered down as long as the 3.3 V "always" power or backup power is provided to the chip. For further details, see Real-Time Clock, page 50.

Flash SSD (option)

The Catalyst LP supports an optional on-module eMMC flash SSD. An 8 GB option is available in the standard module configuration. Options of 16 GB and 32 GB are available as custom module configurations. In addition to providing mass storage, this memory is a system boot option.

Notes:
The eMMC flash SSD option and PCIe slot 3 are mutually exclusive. If the flash SSD is populated, PCIe slot 3 is no longer available on connector J1. This option is set at time of production.

External Memory Interfaces

Five types of external memory interfaces provide mass storage options on a carrier board. The Catalyst LP supplies the signals for an IDE/PATA interface, two SATA ports, nine USB ports, an SD/MMC interface, and up to four PCIe slots that can connect external memory to the module. Connector J1 provides the signals for each option. Include support circuitry and connectors on your carrier board.

The high-speed differential and single-ended signals associated with these external memory interfaces require strict routing constraints on the carrier board. For routing guidelines, see Design Guidelines, page 35.

IDE/PATA Disk Drive

The Catalyst LP provides an IDE/Parallel ATA (PATA) interface for mass storage supporting up to two devices: one master and one slave. A common application is to connect this interface to a 2.5-inch IDE/PATA disk drive.

The following table lists supported IDE/PATA Standards and Modes.

IDE/PATA Standard	Transfer Modes Supported	Transfer Rate (Mbps)
ATA-1 **(ATA, IDE)**	PIO modes 0, 1, 2 Single-word DMA modes 0, 1, 2 Multi-word DMA mode 0	3.3, 5.2, 8.3 2.1, 4.2, 8.3 4.2
ATA-2, ATA-3 **(EIDE, Fast ATA)**	PIO modes 3, 4 Multi-word DMA modes 1, 2	11.1, 16.6 13.3, 16.6
ATA/ATAPI-4 **(Ultra DMA, Ultra ATA)**	Ultra DMA modes 0, 1, 2 (a.k.a. Ultra DMA/33)	16.7, 25.0, 33.3
ATA/ATAPI-5 **(Ultra-DMA, Ultra ATA)**	Ultra DMA modes 3, 4 (a.k.a. Ultra DMA/66)	44.4, 66.7
ATA/ATAPI-6 **(Ultra-DMA, Ultra ATA)**	Ultra-DMA mode 5 (a.k.a. Ultra DMA/100)	100 (reads), 89 (writes)

Table 3. Supported IDE/PATA Standards and Modes

See the following section for limitations of the IDE/PATA and SATA interfaces.

SATA Disk Drive

The Catalyst LP supports two serial ATA (SATA) buses providing the option for high-capacity, removable storage SATA disk drives. These interfaces support the Serial ATA Specification, Revision 2.5 with data transfer rates of up to 3.0 Gbps.

Notes:
Revision A modules support up to two SATA ports. SATA 2 and the IDE/PATA interface are mutually exclusive. If IDE/PATA is used, only SATA 1 is available.

Revision B modules support SATA 1, SATA 2, and IDE/PATA.

USB Mass Storage Device

A USB mass storage device can connect to one of nine USB ports on the Catalyst LP. Any USB device that has USB drivers installed on the Catalyst LP can connect to the USB host ports. For a description of these ports, see USB, page 19.

SD Cards

The Catalyst LP includes one Secure Digital and MultiMediaCard (SD/MMC) interface for memory and I/O expansion. You can use this interface to implement a SD/MMC socket on a carrier board providing mass storage or to develop custom unique add-in cards.

This SD/MMC interface is compliant with the following specifications:

- SD Spec. Part 1 Physical Layer Spec. Version 3.00
- SD Spec. Part A2 SD Host Controller Standard Spec. Version 2.00
- Compliant with SD Spec. Part E1 SDIO Spec. Version 2.00
- Compliant with SD Spec. Part 2 File System Spec. Version 2.00
- Compliant with MultiMediaCard System Spec. Version 4.2

In addition to the SD/MMC signals, connector J1 includes signals to control SD/MMC support circuitry on the carrier board. The interface includes signals to control a power FET and to drive a LED. For routing guidelines, see Design Guidelines, page 35.

PCIe Memory Card

A PCIe x1 memory card can connect to one of four PCIe x1 slots available on the Catalyst LP. For a description of the PCI Express capability, see PCI Express, page 18.

Communications

The Catalyst LP supports several industry-standard channels for communication with peripheral and peer devices on the carrier board. These include PCI Express, USB, Gigabit Ethernet, I^2C bus, and SMBus. The Catalyst LP does not limit flexibility by integrating fixed function I/O components. All communication signals are available on connector J1 providing flexibility and ease of implementation on the carrier board. This allows development of a unique carrier board optimized for your requirements.

PCI Express

A key capability of the Catalyst LP is its PCI Express (PCIe) support. In the standard configuration, the Intel ICH8M provides up to four PCIe one lane (PCIe x1) slots on connector J1. As a custom configuration, these PCIe slots can be configured as one PCIe four lane (PCIe x4) slot. Each slot is compliant with the PCI Express Base Specification, Revision 1.1 supporting 2.5 Gbps bandwidth in each direction. These high-speed differential pairs require strict routing constraints on the carrier board and AC coupling. For routing guidelines, see Design Guidelines, page 35.

Notes:
The eMMC flash SSD option and PCIe slot 3 are mutually exclusive. If the flash SSD is populated, PCIe slot 3 is no longer available on connector J1. This option is set at time of production.

The following table shows the mapping of connector J1 to the Intel ICH8M's PCIe ports.

Connector J1 Pin	Connector J1 Signal Name	Intel ICH8M PCIe Port
A99, A98 **B95, B94**	PCIE_TXP2_SLOT0, PCIE_TXN2_SLOT0 PCIE_RXP2_SLOT0, PCIE_RXN2_SLOT0	1
B99, B98 **A95, A94**	PCIE_TXP2_SLOT1, PCIE_TXN2_SLOT1 PCIE_RXP2_SLOT1, PCIE_RXN2_SLOT1	2
A84, A85 **A87, A88**	PCIE_TXP2_SLOT2, PCIE_TXN2_SLOT2 PCIE_RXP2_SLOT2, PCIE_RXN2_SLOT2	3
B16, B17 **B18, B19**	PCIE_TXP2_SLOT3, PCIE_TXN2_SLOT3 PCIE_RXP2_SLOT3, PCIE_RXN2_SLOT3	4

Table 4. PCIe Slot Mapping

An on-module clock generator supplies the PCIe clocks for two of the four ports: PCIe slot 0 and PCIe slot 1. To provide a reference clock for PCIe slot 2 and PCIe slot 3, include a differential buffer on your carrier board. Buffer the reference clock for PCIe slot 0 or PCIe slot 1 to drive multiple clocks. Use a buffer similar to the type of IDT ICS9DBL411.

Additional input signals to the module, CLK_SLOT0_OE# and CLK_SLOT1_OE#, control each reference clock. On a carrier board, these signals connect to the PCIe sockets indicating the presence of a PCIe device. When activated, this signal enables the PCIe clock for the device. For electrical specifications, see PCIe Clock Generator, page 47.

USB

The Intel ICH8M provides nine Universal Serial Bus (USB) ports. All ports function as general-purpose USB host ports supporting the USB 1.1 specification operating at low (1.5 Mbps) and full (12 Mbps) speeds and the USB 2.0 specification operating at high speed (480 Mbps).

The following table describes the USB connectivity on the Catalyst LP.

Connector J1 Pin	Connector J1 Signal Name	Intel ICH8M USB Port
A71, A72	**USB_PP0, USB_PN0**	0
B71, B72	**USB_PP1, USB_PN1**	1
A68, A69	**USB_PP2, USB_PN2**	2
B67, B68	**USB_PP3, USB_PN3**	3
A65, A66	**USB_PP4, USB_PN4**	4
B64, B65	**USB_PP5, USB_PN5**	5
A62, A63	**USB_PP6, USB_PN6**	6
B61, B62	**USB_PP7, USB_PN7**	7
B74, B75	**USB_PP8, USB_PN8**	9

Table 5. USB Port Connectivity

USB0-5 also include over-current detection inputs. Use these USB host ports to connect to devices external to the carrier board. USB mouse and keyboard are the most common client devices, but you can connect any USB device that has USB drivers installed on the Catalyst LP. USB6, USB7, and USB8 do not include the associated over-current detection signals. When possible, connect these ports to devices on the carrier board. For electrical specifications, see USB, page 47.

In order to create a fully functioning USB host port, include the host power supply, current limiter circuits, EMI chokes, and over-voltage protection on your carrier board. The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The carrier board must supply the 5 V power required by client devices. Use a power switch with the corresponding over-current detection for each port. For routing guidelines, see Design Guidelines, page 35.

Gigabit Ethernet

The Intel ICH8M includes a Gigabit Ethernet Controller that conforms to the IEEE 802.3 standard. This device connects to an Intel® 82567 Gigabit Ethernet Physical Layer Transceiver located on the module, supporting a Media Dependent Interface (MDI) for 10Base-T, 100Base-TX, and 1000Base-T applications. For information about this device, refer to www.intel.com. In addition, the transceiver drives three programmable LED control signals which are available on connector J1.

Depending on your application, this MDI interface may be used directly or magnetics and an RJ-socket may be required on your carrier board to complete the connection to your network. Contact your local Eurotech representative for additional information about the magnetics recommended for use on the carrier board. For routing guidelines, see Design Guidelines, page 35.

Carrier I²C Bus

I²C (Inter-IC) bus is a multi-master, "two-wire" synchronous serial bus for communications between integrated circuits (ICs) and for addressing peripherals in a system. The Catalyst LP provides an external connection to its I²C bus with the embedded controller acting as the bus master.

The following diagram illustrates the I²C architecture on the Catalyst LP.

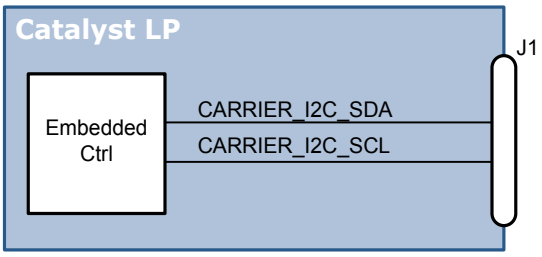


Figure 2. I²C Bus Architecture

When possible, use the SMBus to communicate with devices on the carrier board instead of the carrier I²C bus. When this bus is used on your carrier board, power all devices connected to it using the 3.3 V "Always" power (V3.3A) or isolate the devices from the bus when powered off. Notice that the module does not include termination on the I²C bus. Include 10kΩ pull-up resistors to V3.3A on the carrier board. For electrical specifications, see Carrier I²C Bus, page 47.

System Management Bus

System Management Bus (SMBus) follows the same operating principles as I²C. Similar to I²C, SMBus is a "two-wire" interface allowing multiple devices to communicate with each other. Devices function as bus masters and bus slaves. SMBus enables communication between devices and allows connection of devices that require legacy software accessibility thru standard SMB addressing.

The Catalyst LP provides an external connection on connector J1 to its SMBus with the Intel ICH8M acting as bus master. This bus supports the SMBus 2.0 Specification. In addition, the module supports hardware alerting on the SMBus using the I/O signal SMB_ALERT#.

Notes:
SMBus is not compatible with all I²C devices. Review the device data sheet carefully before connecting an I²C device to the SMBus.

The following diagram illustrates the SMBus architecture.

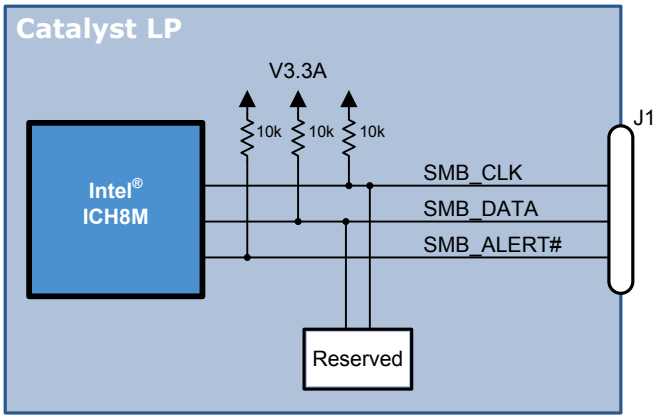


Figure 3. SMBus Architecture

Notice that the module includes pull-up resistors to V3.3A on the SMBus. On your carrier board, power all devices connected to this bus using the V3.3A power or isolate the devices from the bus when powered off. For electrical specifications, see SMBus, page 47.

The following table lists the addresses of the SMBus devices on the Catalyst LP.

Module Device	Address	Function
Reserved	1101 0010 1101 0011	Write Read

Table 6. SMBus Addresses

Display and User Interface

The Intel Atom processor includes an integrated 2D/3D graphics engine supporting hardware-accelerated graphics display and video processing capabilities. The processor provides two independent display outputs. A LVDS output drives the primary display, while a VGA output drives a secondary display. In addition, the processor provides discrete backlight control signals.

This section summarizes the Catalyst LP graphics display and video processing capabilities. Display resolutions are specified at the maximum refresh rate and color depth. Higher resolutions may be possible at lower refresh rates and color depths. This relationship is due primarily to the increased processing bandwidth required at higher output resolutions.

LVDS Display and Backlight Control

The growing demand for higher resolution displays has been meet with design limitations on the interface between the LCD and graphics controller. Increased resolution LCDs require an increased clock speed, a larger number of data lines, and a higher power consumption. LVDS serial data transmission addresses these issues by providing a high-speed, low-power interface on a single pair of wires per channel. The Catalyst LP supplies a LVDS output to drive a primary display.

The following table summarizes the LVDS display output capabilities.

Feature	LVDS Display
Resolution	Up to 1366 x 768, 18-bit color

Table 7. LVDS Display Capabilities

The LVDS display output consists of three LVDS data pairs, as well as a LVDS pixel clock, supporting 18-bit color. If your application requires transmission over a display cable greater than 7 inches, include an LVDS buffer/repeater on your carrier board to boost the data and pixel clock signals. Use controlled impedance cables that target 97 Ω. ± 20%. Cables should not introduce major impedance discontinuities that cause signal reflections. The differential pairs also require strict routing constraints on the carrier board. For routing guidelines, see Design Guidelines, page 35.

Additional capabilities include the discrete signal L_VDDEN (J1 pin A32) that controls power to the display and an I^2C interface (L_DDC_DATA on J1 pin B28, L_DDC_CLK on J1 pin A29) for communication with the LCD Display Data Channel (DDC). For electrical specifications, see LVDS Display and Backlight, page 48.

Backlight

Most LCDs include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Backlight inverters drive the panel backlights. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. To reduce power consumption, most backlight inverters include control signals to dim and turn off the backlight.

To support these features, the Catalyst LP supplies three backlight control signals and an I^2C bus (L_CTLB_DATA on J1 pin B25, L_CTLA_CLK on J1 pin B29) for communication with the backlight. For electrical specifications, see LVDS Display and Backlight, page 48.

The following table describes the backlight control signals.

Signal	J1 Pin	Type	Description
L_BKLTCTL	B33	O	Controls the intensity of the backlight
L_BKLTEN	B32	O	Turns power to the backlight on or off
L_BKLTSEL0_GPIO#	B58	O	Selects backlight control (PWM vs. I^2C)

Table 8. Backlight Control Signals

VGA Display

As a secondary display option, the Catalyst LP drives an analog RGB output. This output provides red, green, and blue data, as well as horizontal sync and vertical sync signals. To connect to a VGA display, add termination, output filters, and buffers on your carrier board. For routing guidelines, see Design Guidelines, page 35.

The following table summarizes the VGA display output capabilities.

Feature		VGA Display
Resolution	D510	Up to 2048 x 1536 x 32 bpp at 60 Hz
	N450	Up to 1400 x 1050 x 32 bpp at 60 Hz

Table 9. VGA Display Capabilities

In addition, the module provides a Display Data Channel (DDC) serial bus (VGA_DDC_SDA on J1 pin A30, VGA_DDC_CLK on J1 pin B30) for monitor Plug and Play capability with various computer displays. For electrical specifications, see VGA Display, page 48.

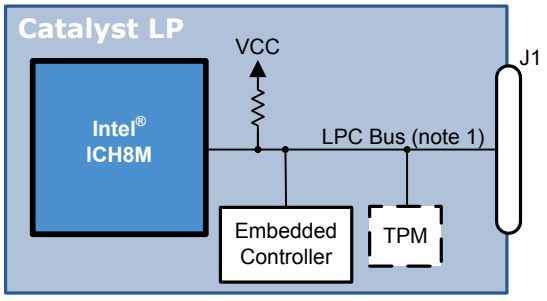
Inputs and Outputs

Several signals on the Catalyst LP support I/O expansion and system management. The module includes a Low Pin Count bus supporting legacy I/O capabilities and multiple discrete I/O signals performing system reset, power control, and general-purpose input and output. Connector J1 includes all I/O signals.

Low Pin Count Bus

In response to the transition from ISA-based systems, the Low Pin Count (LPC) bus provides a migration path for legacy I/O capabilities. This bus enables general-purpose I/O expansion and provides communication to low-bandwidth devices. For this purpose, the Intel ICH8M supplies a LPC bus supporting the supporting the Low Pin Count Interface Specification, Revision 1.1. On the Catalyst LP, the LPC bus connects to the Intel ICH8M, the embedded controller, and an optional TPM.

The following diagram illustrates the LPC bus architecture.



Note:
1. For details about the termination on individual signals on the LPC bus, see J1, page 40.

Figure 4. LPC Bus Architecture

Externally, the LPC bus provides general-purpose expansion. A common application on the carrier board includes a Super I/O Controller that provides I/O capabilities such as serial ports, keyboard, mouse, IrDA, and general-purpose I/O. Ensure that the LPC signals are routed as critical nets on your carrier board and include 10kΩ pull-up resistors to V3.3S on the LPC_ADx signals. For routing guidelines, see Design Guidelines, page 35.

Reset Signals

One of two signals resets the circuitry on the module and carrier board. One signal originates from the module, while the second signal originates from the carrier board. The output signal RST# includes several loads on the Catalyst LP. Include a buffer on the carrier board to drive additional loads.

The following table compares the reset signals.

Signal	J1 Pin	Type	Description
RST#	B56	O	Use as a power-on reset to reset all devices on the carrier board. Output is driven by the module, forces complete system hardware reset, and is used for proper reset timing and logic synchronization.
FP_RESET#	A59	I	Do not use this signal as a power-on reset. FP_RESET# will not be detected until RST# is de-asserted. Input initiates a hardware reset including the Intel Atom processor and Intel ICH8M.

Table 10. Reset Signals

In addition to the hardware resets, the input signal H_INIT# (J1 pin B3) initiates a soft reset of the module. For electrical specifications, see Reset Signals, page 46.

General-Purpose Input and Output

The Catalyst LP provides four general-purpose input and output (GPIO) signals, as described in the following table. For electrical specifications, see General-purpose Inputs and Outputs, page 49.

Signal	J1 Pin	Description
GPIO1	A108	Embedded controller GPIO
GPIO2	A3	Embedded controller GPIO
GPIO3	A2	Intel ICH8M GPIO1
GPIO4	B53	Intel ICH8M GPIO8

Table 11. GPIO Signals

GPIO1 and GPIO2 are software-controlled using the Catalyst System Management API. For details about this API, refer to the *Catalyst System Management Programmer Reference (Eurotech document #110122-2021)*. Future revisions of the API will support the Intel ICH8M GPIO.

Intel High Definition Audio

The Intel High Definition Audio (Intel HD Audio) Specification implements high quality audio in a PC environment. The specification defines a uniform interface between a host computer and audio codec specifying register control, physical connectivity, programming model, and codec architectural components. The Intel ICH8M provides an Intel HD Audio interface capable of supporting up to two external audio codecs. Docking functionality is supported allowing control of an external switch for isolation of the codec within a docking station during normal docking request and acknowledge cycles.

All Intel HD Audio signals are available on connector J1. The Catalyst LP supports only 3.3 V signalling levels. For electrical specifications, see Intel High Definition Audio, page 49. Include audio codecs along with amplifiers, switches, and connectors on your carrier board. For routing guidelines, see Design Guidelines, page 35.

Power Requirements

Power management is especially critical in high-performance systems that also require low power dissipation. Handheld and portable systems available today never really turn "off". They make use of power management techniques that cycle the electronics into power saving modes, but never fully remove power from the full system.

Embedded system designers using the Catalyst LP should have a clear understanding of how the system design allocates power usage. Create a power budget that takes into account the types of devices that are used with the Catalyst LP. For baseline power consumption for the module, see Power Consumption, page 46. This section provides information about power and power management on the Catalyst LP.

Low Power States

The Catalyst LP supports the Advanced Configuration and Power Interface (ACPI), version 2.0. Unlike previous power standards that were BIOS-based, ACPI allows OS-directed power management. It specifies an industry-standard interface for both hardware and software that facilitates power and thermal management. This section describes how the Catalyst LP makes use of the ACPI low power modes.

The ACPI specification defines the low power states for ACPI-compliant systems. The following table describes the states supported by the Catalyst LP.

State	Mode	Description
S0	Full Operation	All devices are operational with dynamic power management functions active.
S3	Standby or Sleep	The Intel Atom processor and Intel ICH8M are powered down. Active operating system context stored in DRAM is retained using low-power self-refresh. Wake events are active and enable a transition back to full operation.
S4	Hibernation	The Intel Atom processor, Intel ICH8M, and DRAM are powered down. Operating system context is saved to disk storage prior to powering down system voltage rails. Limited wake events are active. Resume to full operation is dependent on numerous system components including the disk storage device.
S5	Power down	The Intel Atom processor, Intel ICH8M, and DRAM are powered down. The embedded controller is active but may be in low-power mode. No operating system context is preserved.

Table 12. ACPI Power States

Wake events transition the Catalyst LP from a low-power state back to full operation. The following table lists the signals that can function as wake events. These signals are valid as wake event inputs in power state S3.

Wake Event	J1 Pin	ICH8M Pin	Description
GPIO4	B53	AE16	Intel ICH8M GPIO8
GPIO3	A2	AJ8	Intel ICH8M GPIO1
SMB_ALERT#	A33	AG22	SMBus activity alert
PCIE_WAKE#	B55	AE17	Standard I/O device wake event signal
BTN_ONOFF#	B59	-	Power button input

Table 13. Wake Events

Power Supply Architecture

The architecture of the power supply partitions the power generation across the Catalyst LP and the carrier board. The module requires 5 V and 3.3 V input voltages supplied by the carrier board. It is the responsibility of the carrier board designers to provide input power protection as required by their application. This is especially important if the power supply wires will be subject to EMI/RFI or ESD. On-module regulators generate the core power and all other powers required by the supporting circuitry. For electrical specifications and details about each power rail, see Power Supply, page 45.

Input Power Voltages

The following table describes the input power voltages required by the Catalyst LP.

Name	Power State	Description
V3.3A	S4 exit, S5 exit, S0 operation, and S3 operation	3.3 V “always” power for up/down circuitry only
V3.3S	S0 operation	3.3 V normal operating power
V3.3	S0 operation and S3 operation	3.3 V primary supply voltage for most of the on-board regulated voltages
V5A	S4 exit, S5 exit, S0 operation, and S3 operation	5 V “always” power for up/down circuitry only
V5S	S0 operation	5 V normal operating power
V_BATTERY		Backup power for the RTC

Table 14. Input Power Voltages

Each power rail should be routed as a power plane on your carrier board with sufficient bulk decoupling and local decoupling on each plane. For additional details about carrier board design, see Design Guidelines, page 35.

Notes:
The V5A rail should lead the V3.3A rail during ramp up.

The V5S rail should lead the V3.3S rail during ramp up or not lag by more than 0.7 V. It is acceptable for these two voltage rails to ramp up at the same time.

For an example circuit, see the Eurotech reference carrier board schematic.

The following diagram illustrates the layout of the Catalyst LP power supply.

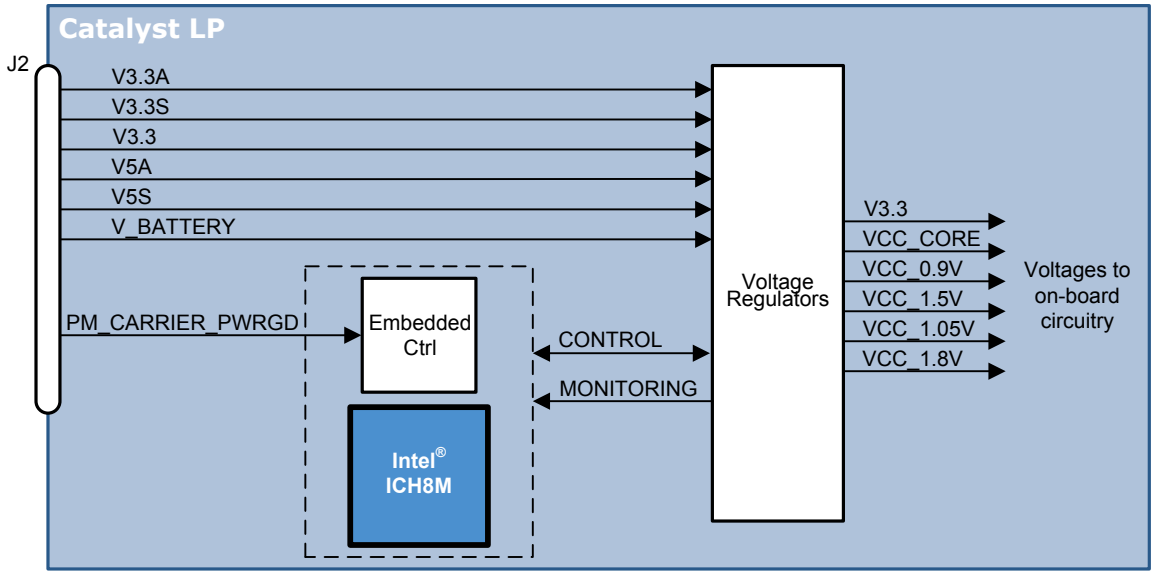


Figure 5. Power Supply Architecture

In addition to the input power voltages, connector J2, page 44 includes the signal PM_CARRIER_PWRGD. This input from the carrier board indicates that all input power voltages are fully operational and within tolerance.

Notes:
The carrier board must provide the PM_CARRIER_PWRGD signal to represent the readiness for operation.

The embedded controller functions, in conjunction with the Intel ICH8M and on-module power switch, to control proper sequencing of voltages allowing for proper start-up, shutdown, and power saving transitions. In addition, it monitors input power voltages and the on-module voltage regulators. For additional details about the embedded controller, see Embedded Controller, page 15.

RTC Backup Power

The Catalyst LP includes a RTC function that retains the system date and time when the system is powered down as long as the 3.3 V “always” power or backup power is provided to the module. Including a long-life 3 V battery on a carrier board is a common method to supply backup power. Use series elements, such as a diode and resistor, on the V_BATTERY output from your carrier board based on your specific requirements.

On the Catalyst LP, the V_BATTERY power input has a diode-OR with V3.3A, as shown in the following diagram.

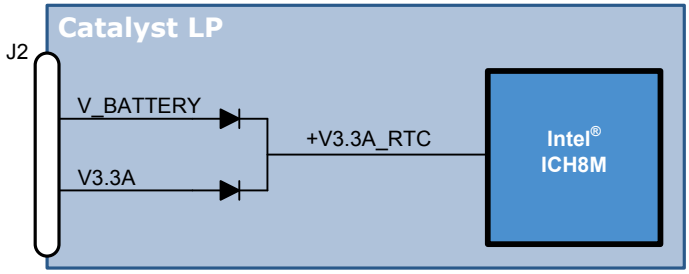


Figure 6. RTC Backup Power Architecture

For specifications, see Power Supply, page 45 and Real-Time Clock, page 50.

Power Switch

The input signal BTN_ONOFF# (J1 pin B59) controls a power switch included on the Catalyst LP. The function of the BTN_ONOFF# signal is dependent on the embedded controller/BIOS setup and the configuration of the operating system. The response of the system can be managed by this combination. On the standard development kit, this input is connected to a momentary button on the carrier board. Pressing this external momentary button turns the power on and off. For electrical specifications, see Power Supply, page 45.

The following table details the operation of the BTN_ONOFF#.

BTN_ONOFF#	Operation
Momentary assertion (less than 4 seconds)	On standard development kit: From shutdown, initiates a power-up sequence to full operation. From full operation, initiates an orderly shutdown sequence and turns off power. Options based on system configuration: From full operation, enters system sleep state. From sleep, returns to full operation.
Continuous assertion (greater than 4 seconds)	Initiates a “4 second over-ride” and turns off power without notification to the operating system.

Table 15. BTN_ONOFF#

Notes:
Once the V5A and V3.3A rails are applied, the BTN_ONOFF# signal is not detected for 400 msec.

Power State Signals

The Catalyst LP provides three control signals on connector J1 indicating the power state. The Intel ICH8M controls the two power state signals, PM_EN_S0# (J1 pin B104) and PM_EN_S3# (J1 pin B107). The on-module power switch controls the remaining signal, PM_EN_PWR (J1 pin B105). For electrical specifications, see Power Supply, page 45.

The following table lists these signals with the power states and input power voltages active in each state.

State	Active power rails	PM_EN_PWR	PM_EN_S3#	PM_EN_S0#
S0	V3.3, V5S V3.3S V5A, V3.3A	High	Low	Low
S3	V3.3, V5A, V3.3A	High	Low	High
S4	V5A, V3.3A	Low	High	High
S5	V5A, V3.3A	Low	High	High

Table 16. Low Power States

Notes:
Implement the exact power supply sequencing as described in this section. The module has very specific power-on sequence requirements in order to power-up and operate correctly. Power sequencing the multiple voltage rails is CRITICAL. If your design does not meet these requirements, the module will not boot.

For additional details about best practices for power sequencing, contact your local Eurotech representative.

The following timing diagrams describe the relationship of the power state control signals on the Catalyst LP.

Power-on initiated by power button press

In a typical system power on, the falling edge of BTN_ONOFF# drives PM_EN_PWR high. A hardware latch on the Catalyst LP controls PM_EN_PWR. The embedded controller monitors BTN_ONOFF# until the rising edge of BTN_ONOFF#.

After sampling BTN_ONOFF# high, the embedded controller waits for PM_CARRIER_PWRGD to be asserted high before driving PM_EN_S3# active (logic level low). After PM_CARRIER_PWRGD is asserted, S3 power rails internal to the Catalyst LP are enabled with the assertion of PM_EN_S3# and powered by V3.3. After the S3 power rails are within specification on the module and on the carrier board, the ICH8M asserts PM_EN_S0# (logic level low). The time from PM_EN_S3# active to PM_EN_S0# active depends on how quickly the carrier supplies V3.3.

(This diagram will be provided in future revisions.)

Figure 7. Power-on initiated by power button press

Standby (Enter S3)

The following diagram shows the Catalyst LP transitioning from S0 to S3. This transition can be initiated by the operating system or the BTN_ONOFF# input in combination with the operating system. The PM_EN_S0# signal will be de-asserted, and all S0 power rails on the Catalyst LP module will be turned off. The PM_CARRIER_PWRGD signal is not monitored for 10 ms following the de-assertion of PM_EN_S0#. This allows the carrier board S0 power rails to be turned off and PM_CARRIER_PWRGD to provide status of the power rails remaining on in S3.

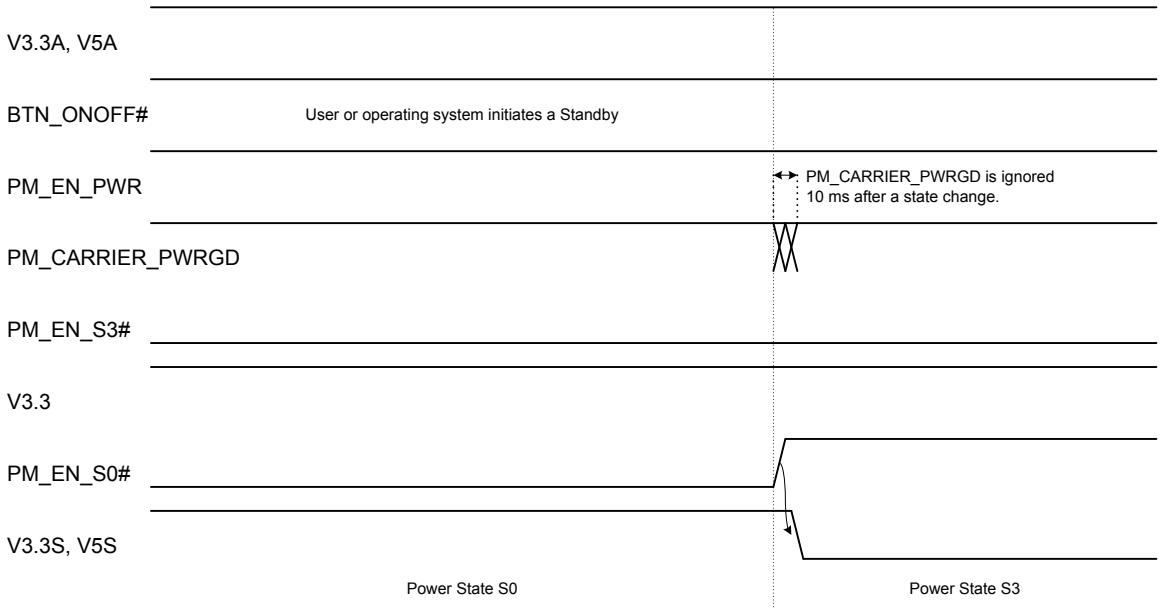


Figure 8. Standby (Enter S3)

Standby (Exit S3)

The following diagram shows the system exiting S3. The system may wake from S3 because of any event shown in Table 13, page 24. PM_EN_S0# will be asserted causing all S0 power rails on the Catalyst LP to be turned on. PM_CARRIER_PWRGD will not be monitored for 10 ms after PM_EN_S0# is de-asserted. This provides time for all S0 power rails on the carrier board to be turned on and within specification.

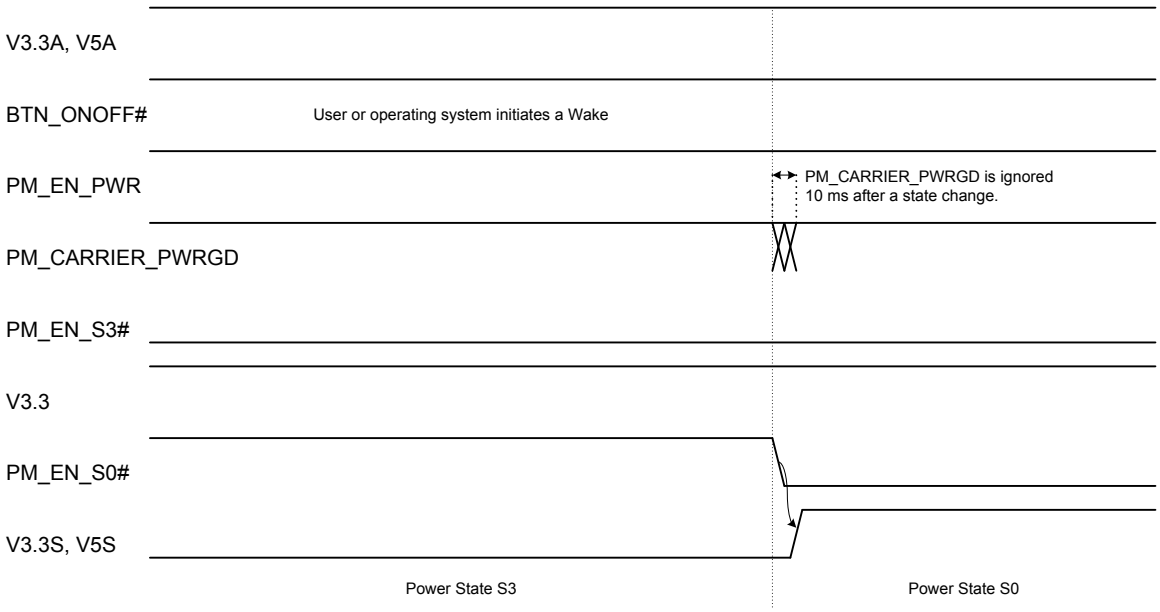


Figure 9. Standby (Exit S3)

Power off initiated by power button press

The following diagram shows a system powering off because of an assertion of the BTN_ONOFF# signal. Depending on operating system settings, a system may power off or sleep due to asserting BTN_ONOFF#. If set for a power off, the operating system will save all information needed and the system will perform a graceful shutdown. PM_EN_S0# will be de-asserted, followed by PM_EN_S3# and PM_EN_PWR being de-asserted.

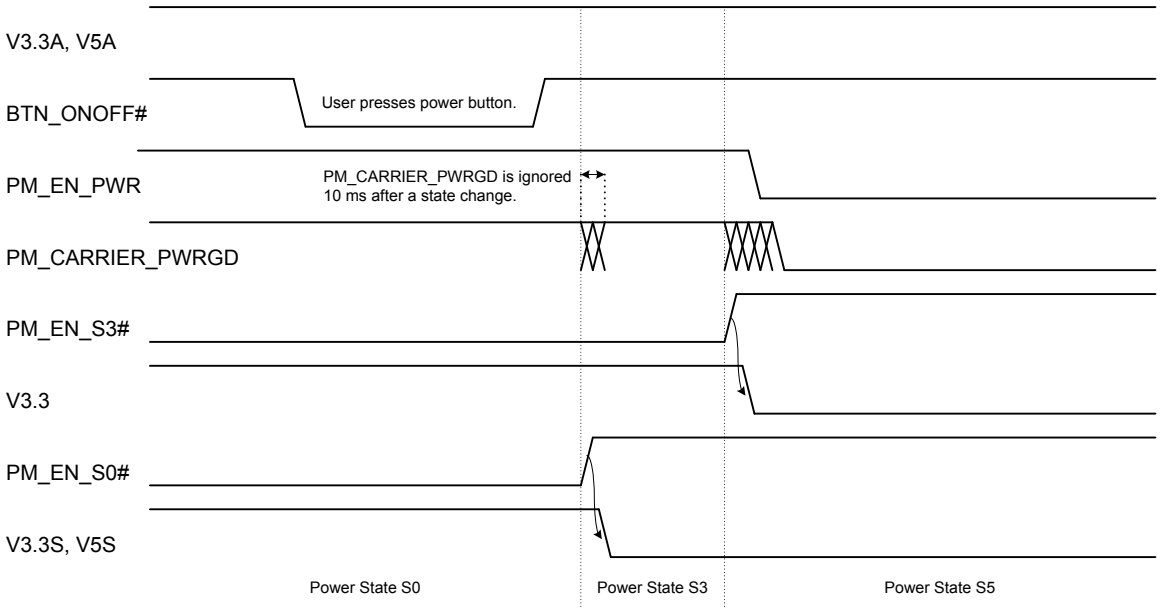


Figure 10. Power off initiated by power button press

System shutdown initiated by operating system

The following diagram shows a system powering at the request of the operating system. The user could initiate this via software control. The operating system will save all information needed and teh system will perform a graceful shutdown. PM_EN_S0# will be de-asserted, followed by PM_EN_S3# and PM_EN_PWR being de-asserted.

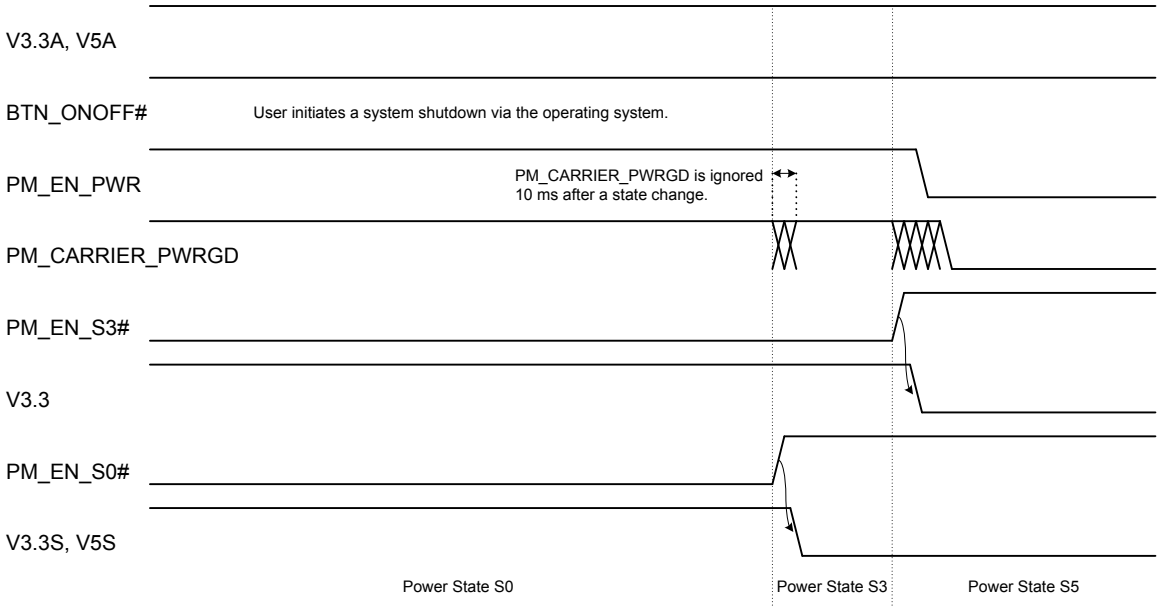


Figure 11. System shutdown initiated by operating system

Mechanical Specifications

This section describes mechanical and thermal design guidelines for the Catalyst LP.

Mechanical Design

Mechanical Drawing

The following mechanical drawing specifies the dimensions of the Catalyst LP, as well as locations of key components on the board. All dimensions are in inches.

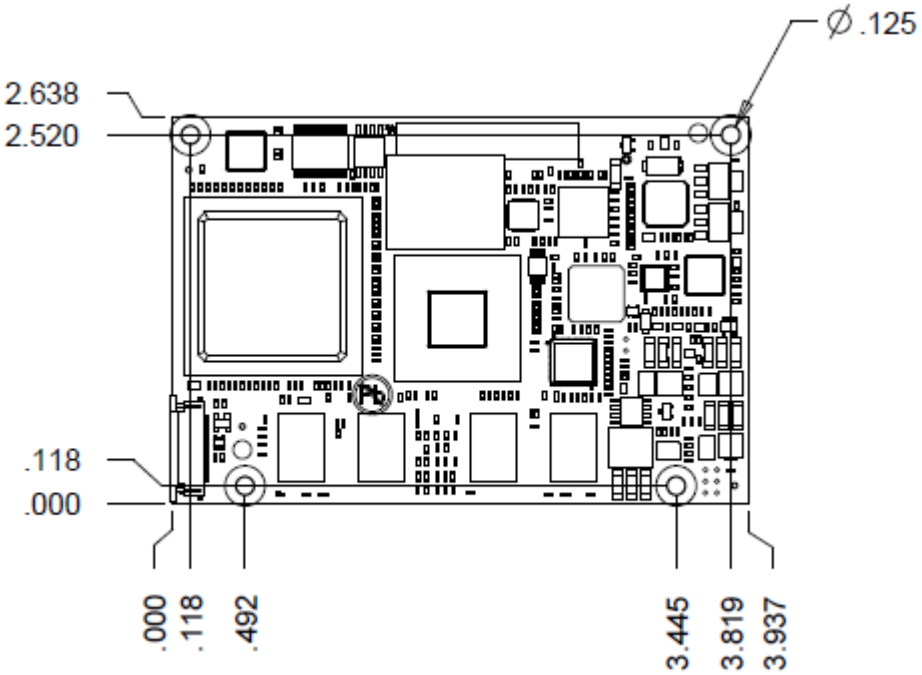


Figure 12. Catalyst LP, Top View

Figure 13. Catalyst LP, Side View

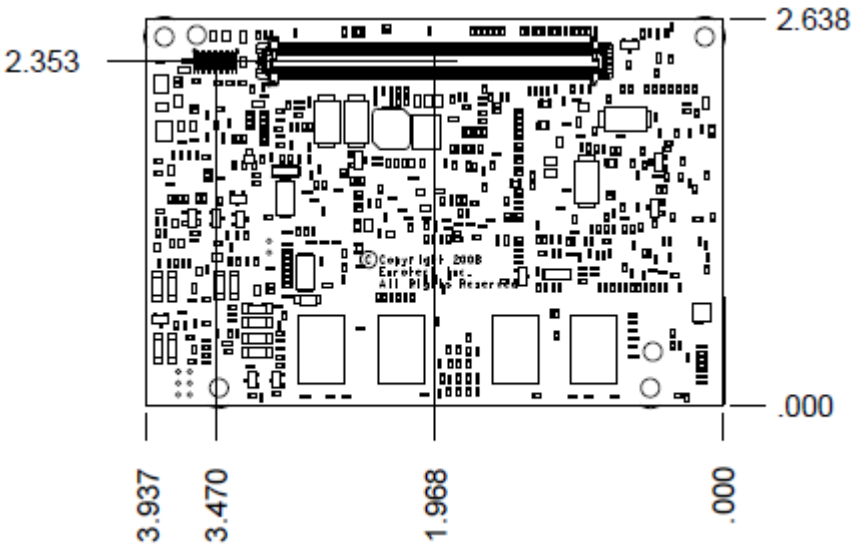


Figure 14. Catalyst LP, Bottom View

Notes:
For a 2D CAD drawing and 3D CAD model, check the Eurotech support site (http://support.eurotech-inc.com/) or contact your local Eurotech representative.

Total Stack Height

Selection of low profile stacking connectors and components minimizes the total stack height of the Catalyst LP and carrier board. The module uses stacking board-to-board connectors to mate with a carrier board. The mating connectors on the carrier board can be either 5 mm or 8 mm stacking height. When 5 mm stacking board-to-board connectors are used, the total board height combined with the connector clearance results in a total stack height of 8.7 mm. You may place components under the module on a custom carrier board. However, the design must allow adequate heat dissipation.

The following diagram illustrates the total stack height using 5 mm stacking connectors on the carrier board.

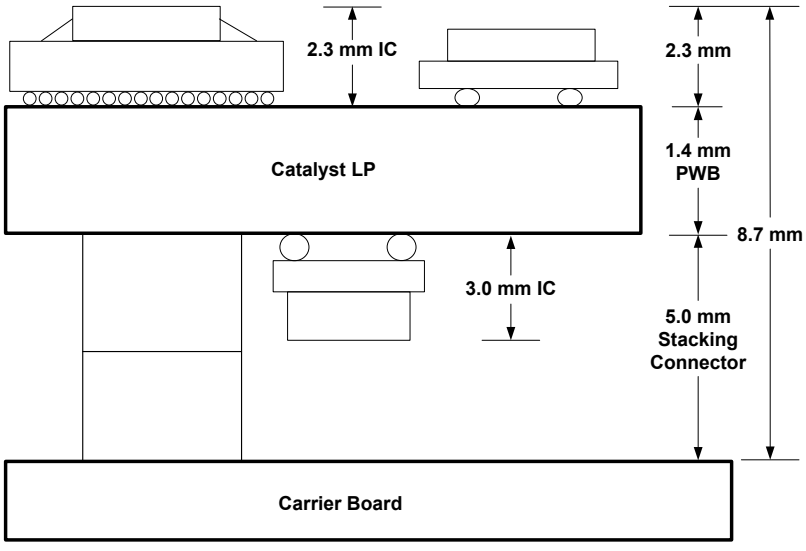


Figure 15. Total Stack Height

Mounting Holes

Four holes enable mounting on the carrier board. Along one side, two mounting holes are located on each corner. The mounting holes are placed off set from the corners along the opposite side of the module. The Catalyst LP ground plane connects electrically to the mounting holes.

Per IPC-A-610D section 4.2.3, secure the board to standoffs using a flat washer against the board with a split washer on top between the flat washer and the screw head or nut. Do not use toothed star washers, as they cut into the plating and laminations of the board over time and will not produce an attachment that will withstand vibration and thermal cycling.

Insertion and Removal

The Catalyst LP connects to the carrier board through two connectors that are in line with each other. A high-density, stacking board-to-board connector carries the data signals, while a smaller 2x7-pin 1 mm-pitch connector carries power. When fully connected, these fine pitch connectors provide reliable and durable connection. However, care is required when removing or installing the module onto the carrier board. If correct procedures for installation and removal are not followed, damage to the connectors and/or the connector pins can result.

For detailed procedures to install a module onto or remove a module from a carrier board, refer to the *Catalyst Module Installation and Removal (Eurotech document #110122-2014)*. Download this document from the Eurotech support site (http://support.eurotech-inc.com/, topic 2778).

Warning:
Observe industry-standard electronic handling procedures when handling the module. Eurotech recommends using a grounded wrist strap and heel strap. The connectors expose signals on the system bus that do not have ESD protection.

Thermal Management

The Catalyst LP requires convective cooling or heat spreading to dissipate the heat generated by the module. The following section provides details about thermal management for the Catalyst LP.

The Thermal Design Power (TDP) is a representation of the expected peak power dissipation of each component or component group as viewed separately. The actual power consumption in real-world applications is not expected to reach this level for any given device and never in combination. However, the thermal management solution should accommodate proper control of temperature rise so as not to exceed the maximum thermal design interface temperatures as identified for key components.

The following table summarizes the thermal design power for three key components on the Catalyst LP. The local ambient temperature of the module is defined by the temperatures at these three thermal design interface contact points.

Component		Thermal Design Power – Max Point	Units
Intel Atom processor (note 2)	Dual core	5.5	W
	Single core	13	W
Intel ICH8M		2.4	W
DDR-2 DRAM **8 devices (4 top, 4 bottom), Combined power**		2.25	W

Notes:
2. TDP per the Intel Atom Processor N450, D410 and D510 for Embedded Applications Thermal Design Guide, Revision 1.0, February 2010 (#323439-001 EN).

Table 17. Thermal Design Power

The following diagrams illustrate the location of the three key thermal design interface contact points.

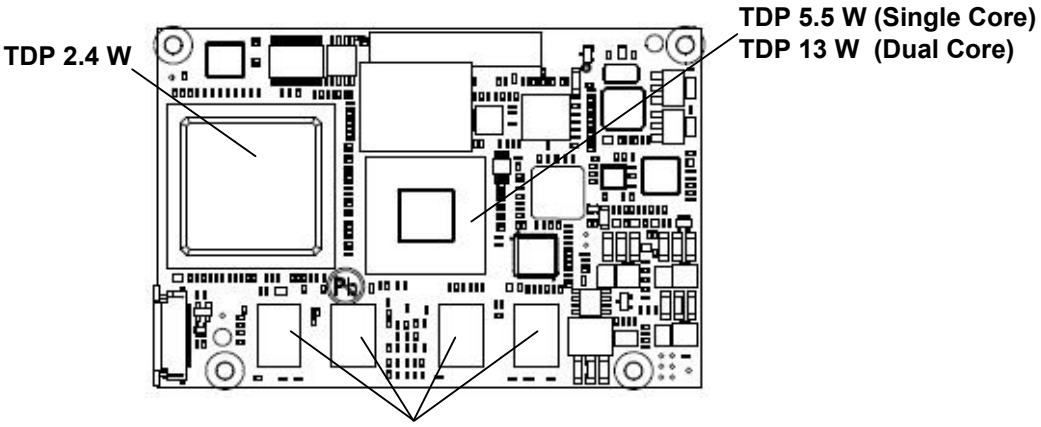


Figure 16. Thermal Interface, Top Side

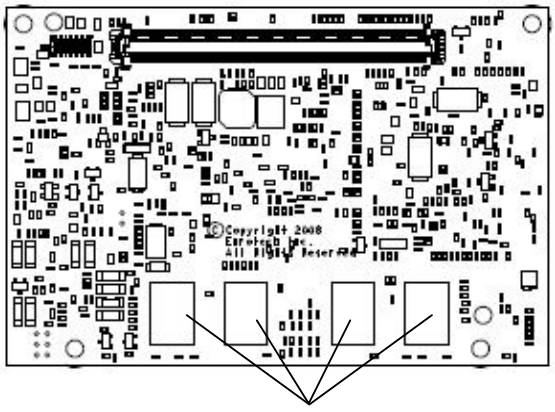


Figure 17. Thermal Interface, Bottom Side

Carrier Board Design

An application-specific carrier board integrates with the Catalyst LP to meet various system requirements. The Catalyst LP Development Kit includes a carrier board designed to maximize the Catalyst LP functionality. This carrier board implements many industry-standard interfaces and provides a reference for custom carrier boards optimized for your requirements. This section includes many of the considerations followed in the design of the Catalyst LP Development Kit carrier board.

Design Guidelines

Design Constraints

Increasing reliability is a key consideration in the Catalyst LP design. Several constraints followed in the module design and printed wiring board (PWB) layout ensure superior product reliability and compatibility. Use similar constraints in the carrier board design.

The following are the design considerations used to improve the Catalyst LP reliability:

- Advanced high-speed signal routing techniques
  - Strict adherence to signal routing rules as collaborated with Intel design and simulation teams
    - Minimum and maximum trace lengths
    - Total, segment, and multi-segment including package length compensation
    - Bus and group length matching to tight tolerances
    - Continuous trace matching for differential pair routing
  - Impedance matching and controlled design
    - Consideration of I/O buffer characteristic variances over extended temperature ranges for improved electrical performance
    - 100% continuous ground return path for all high-speed signals
    - Routing over continuous planes for consistent transmission line impedance and clean, reliable signal transitions
- Conservative printed wiring design construction
  - Durable feature sizes and construction elements
    - Pads, fills, and holes optimized for ROHS processing and long term reliability
  - Buried power planes between ground layers to eliminate coupling with high-speed signals
  - De-rating for current loading on the power regulation circuit and interface
  - No bottom side “hot” power regulation components underneath the Intel Atom processor or the Intel ICH8M that would reduce thermal performance

EMI/RFI Protection

Many products using Eurotech single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. The Catalyst LP incorporates the following design considerations that reduce emission and improve immunity:

- Four extra solid ground planes
- High-speed signal routing on internal ground referenced layers
- No high-speed signal return currents passed thru coupling capacitors
- Option for EMI ring on module perimeter

Routing Guidelines

High-Speed Differential and Single-ended Signals

Proper signal routing is critical to a successful carrier board design. The Catalyst LP supports high-speed differential and single-ended signals that require strict routing constraints. Use the following recommendations to route high-speed signals:

- Ground references
- Continuous reference planes
- Matched lengths
- Bend minimization
- Layer-to-layer connection reduction

The following are the high-speed differential pairs that require strict routing constraints on a carrier board:

- PCIe
  The PCIe x1 slot consists of differential signal pairs for transmit, receive, and reference clock. The module includes AC coupling capacitors on the transmit pair. Include AC coupling capacitors on the receive pair driven from the carrier board to the Catalyst LP. The recommended coupling capacitor is a 0.1µF surface mount 0402 discrete capacitor of type X7R/X5R. Place the 0.1µF capacitors near the PCIe device on the carrier board.
- USB
  These signal pairs can be routed to USB sockets for external connections or directly to USB devices on the carrier board. Include an EMI choke between connector J1 and the USB connector when driving a USB cable. Applications with USB devices hardwired on-board do not require an EMI choke.
- LVDS display
  The LVDS display output includes three LVDS data pairs and a LVDS pixel clock.
- SATA
  Each SATA interface includes two high-speed differential pairs.
- Ethernet
  The Gigabit Ethernet signals include four high-speed differential pairs.

The following are the high-speed single-ended signals that require strict routing constraints on a carrier board:

- IDE/PATA interface
- SD/MMC
- LPC bus
- HD Audio

Analog Video Signals

The VGA display output includes analog video signals that require strict routing constraints on a carrier board. Use the following recommendations to route these signals:

- Separate analog section with no digital signals routed through the section
- Continuous analog reference plane
- Adequate spacing between signals
- Bend minimization
- Layer-to-layer connection reduction

Contact your local Eurotech technical support for additional signal routing details.

Power Planes

The following voltages are inputs to the module on J2, page 44. These nets should be power planes on your carrier board:

- V3.3
- V3.3A
- V3.3S
- V5A
- V5S

Be sure to include sufficient bulk decoupling and local decoupling on each plane.

Requirements and Recommendations

The previous sections provided details about the various features of the Catalyst LP including design requirements and design recommendations. This section summarizes these design guidelines and provides a checklist for custom carrier board design.

Required Circuitry

The following table lists circuitry required on the carrier board.

Name	Pin	Carrier Board Design Requirement
Cat_LP_Detect	J1 B103	See Carrier Board Configuration, page 37.
FP_RESET#	J1 A59	Include momentary button
BTN_ONOFF#	J1 B59	Include momentary button
PCIE_RXP2_SLOT0 **PCIE_RXN2_SLOT0**	J1 B95 J1 B94	Include 0.1µF AC coupling capacitors
PCIE_RXP2_SLOT1 **PCIE_RXN2_SLOT1**	J1 A95 J1 A94	Include 0.1µF AC coupling capacitors
PCIE_RXP2_SLOT2 **PCIE_RXN2_SLOT2**	J1 A87 J1 A88	Include 0.1µF AC coupling capacitors
PCIE_RXP2_SLOT3 **PCIE_RXN2_SLOT3**	J1 B18 J1 B19	Include 0.1µF AC coupling capacitors
CARRIER_I2C_SDA **CARRIER_I2C_SCL**	J1 B108 J1 B109	Include 10kΩ pull-up to V3.3A
SMC_UART_RX **SMC_UART_TX**	J1 B57 J1 B106	Include access to these nets using test points or connector to aid in carrier board bring up Include a 10kΩ pull-up to V3.3A to SMC_UART_RX
L_DDC_CLK **L_DDC_DATA**	J1 A29 J1 B28	Include a 2.2kΩ pull up to V3.3S
V_BATTERY	J2 4	Include 3 V battery

Table 18. Circuitry Required on the Carrier Board

Carrier Board Configuration

The Catalyst LP conforms to the same footprint as other Eurotech modules. However, the modules are not pin-compatible. Each module has a unique pinout on connector J1 providing different feature sets. When installed in a carrier board, the Catalyst LP reads the input signal Cat_LP_Detect (J1 B103) to determine the configuration of the carrier board. This pin must be left open on your carrier board. If the Cat_LP_Detect input is connected incorrectly on the carrier board, the Catalyst LP will not boot.

Recommended Circuitry

The following table lists recommendations for circuitry on the carrier board.

Name	J1 Pin	Carrier Board Design Recommendation
JTAG_TDO	A106	Include 10kΩ pull-up to V3.3S
CLK_LPC_FWH	A36	Include no more than one load
CLK_LPC_SIO	B37	Connect to legacy IO controller if required
LPC_AD3 **LPC_AD2** **LPC_AD1** **LPC_AD0**	B38 B34 B39 B36	Include 10kΩ pull-ups to V3.3S
RST#	B56	Buffer for signal drive strength
L_CTLA_CLK **L_CTLB_DATA**	B29 B25	Include 4.7kΩ pull up to V3.3S
SLOT0_WP	B12	Include a 10kΩ pull up to V3.3S
USB_PP0 **USB_PN0**	A71 A72	Include an EMI choke between connector J1 and the USB connector
USB_PP1 **USB_PN1**	B71 B72	Include an EMI choke between connector J1 and the USB connector
USB_PP2 **USB_PN2**	A68 A69	Include an EMI choke between connector J1 and the USB connector
USB_PP3 **USB_PN3**	B67 B68	Include an EMI choke between connector J1 and the USB connector
USB_PP4 **USB_PN4**	A65 A66	Include an EMI choke between connector J1 and the USB connector
USB_PP5 **USB_PN5**	B64 B65	Include an EMI choke between connector J1 and the USB connector
USB_PP6 **USB_PN6**	A62 A63	Include an EMI choke between connector J1 and the USB connector
USB_PP7 **USB_PN7**	B61 B62	Include an EMI choke between connector J1 and the USB connector
USB_PP8 **USB_PN8**	B74 B75	Include an EMI choke between connector J1 and the USB connector
SATA1_T+ **SATA1_T-**	A17 A18	Include 0.01µF AC coupling capacitors. Place near SATA connector.
SATA1_R+ **SATA1_R-**	A19 A20	Include 0.01µF AC coupling capacitors. Place near SATA connector.
SATA2_T+ **SATA2_T-**	B81 B82	Include 0.01µF AC coupling capacitors. Place near SATA connector.
SATA2_R+ **SATA2_R-**	B84 B85	Include 0.01µF AC coupling capacitors. Place near SATA connector.
VGA_R **VGA_G** **VGA_B**	A91 A92 B91	Include termination and filter

Table 19. Circuitry Recommended on the Carrier Board

Test and Debug

The maintenance serial port is extremely important in bring-up of a new carrier board design. Eurotech highly recommends including an external connection to SMC_UART_RX (J1 B57) and SMC_UART_TX (J1 B106) on your carrier board.

The IEEE1149.1 JTAG port, provided on connector J1, is available for programming the CPLD on the module, factory test, and software debugging. Otherwise, this port is not supported for application use. Eurotech highly recommends including an external connection to this JTAG port on your carrier board. To ensure correct operation of the JTAG interface, include a 10kΩ pull-up resistor to V3.3S on the TDO signal on the carrier board.

An additional ITP debug port, connector J3, provides full access to the XDP debugger port using a SFF style connector. Eurotech highly recommends allowing for access to this connector, in the event you are directed to use this port when working with Eurotech staff. Allow for the size of the mating connector and bend radius of the cable.

Connectors

Identifying Connectors

The following diagrams illustrate the location and numbering of the connectors on the Catalyst LP. When viewing the module from the component side, connector J1 and connector J2 lie under the module.

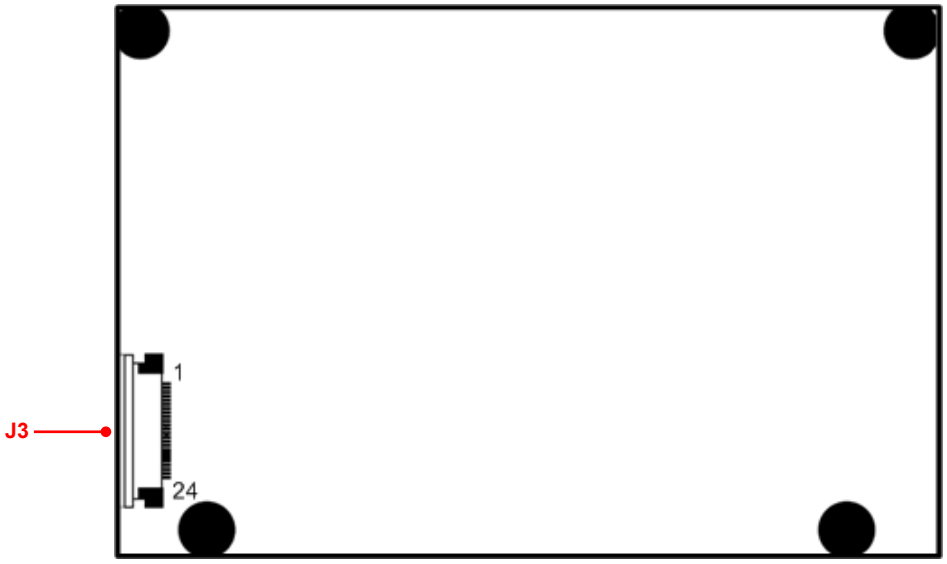


Figure 18. Connector Location, Top View

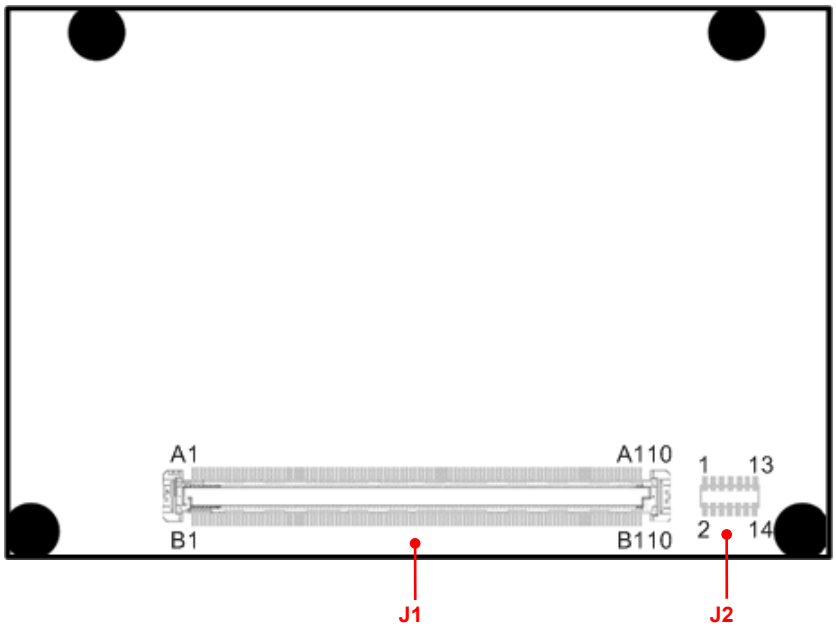


Figure 19. Connector Location, Bottom View

Signal Headers

The following tables describe the electrical signals available on the connectors of the module. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions, and references to related sections.

J1: Docking Connector: Data

Board connector: 220-pin, stacking board-to-board receptacle, 0.5 mm, Tyco Electronics 3-6318490-6
Carrier board connector: Tyco Electronics 3-1827253-6, 5 mm stacking height
Tyco Electronics 3-6318491-6, 8 mm stacking height

The Catalyst LP connector J1 mates to the carrier board. Most data signals are provided on this docking connector.

Pin	Name	Type	On Module Termination	Description
A1	GND	P		Ground
A2	GPIO3	IO-3.3		Intel ICH8M GPIO1
A3	GPIO2	IO-CMOS		Embedded controller GPIO
A4	HDA_SYNC	O-HDA		Intel HD Audio frame sync
A5	HDA_RST#	O-HDA		Intel HD Audio reset
A6	HDA_SDATAIN0	I-HDA		Intel HD Audio serial data input 0
A7	HDA_SDATAIN1	I-HDA		Intel HD Audio serial data input 1
A8	SLOT0_DATA4	IO-3.3		SD/MMC 0 data 4
A9	SLOT0_DATA3	IO-3.3		SD/MMC 0 data 3
A10	SLOT0_DATA1	IO-3.3		SD/MMC 0 data 1
A11	GND	P		Ground
A12	SLOT0_LED	O-3.3		SD/MMC 0 LED
A13	SLOT0_CLK	O-3.3		SD/MMC 0 clock
A14	LDRQ0#	IO-LVTTL		LPC bus encoded DMA request (Contact Eurotech for details)
A15	SLOT0_DATA7	IO-3.3		SD/MMC 0 data 7
A16	SLOT0_PWR#	O-3.3		SD/MMC 0 power control
A17	SATA1_T+	O-SATA		SATA1 transmit, positive signal
A18	SATA1_T-	O-SATA		SATA1 transmit, negative signal
A19	SATA1_R+	I-SATA		SATA1 receive, positive signal
A20	SATA1_R-	I-SATA		SATA1 receive, negative signal
A21	GND	P		Ground
A22	MDI_P_0	IO-A		Gigabit Ethernet, positive signal
A23	MDI_N_0	IO-A		Gigabit Ethernet, negative signal
A24	LAN_LED0	O-3.3		Ethernet LED 0
A25	MDI_P_2	IO-A		Gigabit Ethernet, positive signal
A26	MDI_N_2	IO-A		Gigabit Ethernet, negative signal
A27	MDI_P_3	IO-A		Gigabit Ethernet, positive signal
A28	MDI_N_3	IO-A		Gigabit Ethernet, negative signal
A29	L_DDC_CLK	O-OD		LCD DDC I^2C clock
A30	VGA_DDC_SDA	IO-OD	PU 6.81kΩ V3.3S	VGA DDC I^2C data
A31	GND	P		Ground
A32	L_VDDEN	O-CMOS		LCD power enable
A33	SMB_ALERT#	IO-LVTTL	PU 10kΩ V3.3A	SMBus activity alert
A34	SPKR	O-LVTTL		Intel HD Audio speaker
A35	PM_CLKRUN#	IO-LVTTL	PU 8.25kΩ V3.3S	Initiates active clock output from LPC bus master
A36	CLK_LPC_FWH	O-LVTTL	R 33.2Ω PU 10kΩ V3.3S	LPC bus clock
A37	IDE_PDIOW#	O-LVTTL		IDE/PATA write
A38	SMB_CLK	O-LVTTL	PU 10kΩ V3.3A	SMBus clock
A39	INT_SERIRQ	IO-LVTTL	PU 10kΩ V3.3S	LPC bus interrupt
A40	LPC_FRAME#	O-LVTTL		LPC bus frame sync
A41	GND	P		Ground
A42	IDE_PDA0	O-LVTTL		IDE/PATA address 0
A43	IDE_PDD0	IO-IDE		IDE/PATA data 0
A44	IDE_PDD3	IO-IDE		IDE/PATA data 3
A45	IDE_PDD9	IO-IDE		IDE/PATA data 9

Pin	Name	Type	On Module Termination	Description
A46	IDE_PDA2	O-LVTTL		IDE/PATA address 2
A47	IDE_PDD5	IO-IDE		IDE/PATA data 5
A48	IDE_PDD6	IO-IDE		IDE/PATA data 6
A49	IDE_PDD1	IO-IDE		IDE/PATA data 1
A50	IDE_PDIOR#	O-LVTTL		IDE/PATA read
A51	GND	P		Ground
A52	IDE_PDD2	IO-IDE		IDE/PATA data 2
A53	INT_IRQ14	I-LVTTL	PU 10kΩ V3.3S	IDE/PATA interrupt
A54	IDE_PDIORDY	I-LVTTL	PU 4.7kΩ V3.3S	IDE/PATA ready
A55	IDE_PDCS1#	O-LVTTL		IDE-PATA chip select 1
A56	IDE_PDCS3#	O-LVTTL		IDE-PATA chip select 3
A57	HDA_DOCK_EN#	O-LVTTL		Intel HD Audio enable
A58	HDA_DOCK_RST#	O-HDA		Intel HD Audio reset
A59	FP_RESET#	I-3.3	PU 10kΩ V3.3S	Front panel reset
A60	GND	P		Ground
A61	USB_OC5#	I-LVTTL	PU 10kΩ V3.3A	USB5 over current
A62	USB_PP6	IO-USB		USB 6, positive signal
A63	USB_PN6	IO-USB		USB 6, negative signal
A64	GND	P		Ground
A65	USB_PP4	IO-USB		USB 4, positive signal
A66	USB_PN4	IO-USB		USB 4, negative signal
A67	GND	P		Ground
A68	USB_PP2	IO-USB		USB 2, positive signal
A69	USB_PN2	IO-USB		USB 2, negative signal
A70	GND	P		Ground
A71	USB_PP0	IO-USB		USB 0, positive signal
A72	USB_PN0	IO-USB		USB 0, negative signal
A73	GND	P		Ground
A74	LA_CLKP	O-LVDS		LVDS clock, positive signal
A75	LA_CLKN	O-LVDS		LVDS clock, negative signal
A76	GND	P		Ground
A77	LA_DATAP2	O-LVDS		LVDS data 2, positive signal
A78	LA_DATAN2	O-LVDS		LVDS data 2, negative signal
A79	USB_OC2#	I-LVTTL	PU 10kΩ V3.3A	USB 2 over current
A80	GND	P		Ground
A81	LA_DATAP1	O-LVDS		LVDS data 1, positive signal
A82	LA_DATAN1	O-LVDS		LVDS data 1, negative signal
A83	GND	P		Ground
A84	PCIE_TXP2_SLOT2	O-PCIe	C 0.1µF	PCIe 2 transmit , positive signal
A85	PCIE_TXN2_SLOT2	O-PCIe	C 0.1µF	PCIe 2 transmit, negative signal
A86	GND	P		Ground
A87	PCIE_RXP2_SLOT2	I-PCIe		PCIe 2 receive, positive signal
A88	PCIE_RXN2_SLOT2	I-PCIe		PCIe 2 receive, negative signal
A89	USB_OC3#	I-LVTTL	PU 10kΩ V3.3A	USB 3 over current
A90	GND	P		Ground
A91	VGA_R	O-A	PD 150Ω	Red data
A92	VGA_G	O-A	PD 150Ω	Green data
A93	GND	P		Ground
A94	PCIE_RXN2_SLOT1	I-PCIe		PCIe 1 Receive , negative signal
A95	PCIE_RXP2_SLOT1	I-PCIe		PCIe 1 Receive, positive signal
A96	GND	P		Ground
A97	CLK_SLOT0_OE#	I-LVTTL	R 475Ω PU 10kΩ V3.3S	PCIe 0 clock enable
A98	PCIE_TXN2_SLOT0	O-PCIe	C 0.1µF	PCIe 0 Transmit, negative signal
A99	PCIE_TXP2_SLOT0	O-PCIe	C 0.1µF	PCIe 0 Transmit, positive signal
A100	GND	P		Ground
A101	CLK_PCIE_SLOT0	O		PCIe 0 Clock, positive signal
A102	CLK_PCIE_SLOT0#	O		PCIe 0 Clock, negative signal
A103	GND	P		Ground
A104	JTAG_TMS	O	PU 10kΩ V3.3S	JTAG
A105	JTAG_TCK	I	PD 1kΩ	JTAG
A106	JTAG_TDO	O		JTAG
A107	JTAG_TDI	I	PU 10kΩ V3.3S	JTAG
A108	GPIO1	IO-CMOS		Embedded controller GPIO

Pin	Name	Type	On Module Termination	Description
A109	Reserved			
A110	GND	P		Ground
B1	GND	P		Ground
B2	LPCPD#	O-LVTTL		(Contact Eurotech for details)
B3	H_INIT#	I-LVCMOS		Soft reset for host processor
B4	HDA_BITCLK	O-HDA		Intel HD Audio bit clock
B5	HDA_SDATAOUT	O-HDA		Intel HD Audio data out
B6	SLOT0_CMD	IO-3.3	PU 40.2kΩ V3.3S	SD/MMC 0 command
B7	SLOT0_DATA0	IO-3.3		SD/MMC 0 data 0
B8	SLOT0_DATA6	IO-3.3		SD/MMC 0 data 6
B9	SLOT0_DATA5	IO-3.3		SD/MMC 0 data 5
B10	SLOT0_DATA2	IO-3.3		SD/MMC 0 data 2
B11	GND	P		Ground
B12	SLOT0_WP	I-3.3		SD/MMC 0 write protect
B13	SLOT0_CD#	I-3.3	PU 10kΩ V3.3S	SD/MMC 0 card detection
B14	Reserved			
B15	Reserved			
B16	PCIE_TXP2_SLOT3	O-PCIe	C 0.1µF	PCIE 3 transmit, positive signal
B17	PCIE_TXN2_SLOT3	O-PCIe	C 0.1µF	PCIE 3 transmit, negative signal
B18	PCIE_RXP2_SLOT3	I-PCIe		PCIE 3 receive, positive signal
B19	PCIE_RXN2_SLOT3	I-PCIe		PCIE 3 receive, negative signal
B20	Reserved			
B21	GND	P		Ground
B22	MDI_P_1	IO-A		Gigabit Ethernet, positive signal
B23	MDI_N_1	IO-A		Gigabit Ethernet, negative signal
B24	LAN_LED2	O-3.3		Ethernet LED 2
B25	L_CTLB_DATA	IO-OD		Backlight I^2C data
B26	Reserved			
B27	LAN_LED1	O-3.3		Ethernet LED 1
B28	L_DDC_DATA	IO-OD		LCD DDC I^2C data
B29	L_CTLA_CLK	O-OD		Backlight I^2C clock
B30	VGA_DDC_CLK	O-OD	PU 6.81kΩ V3.3S	VGA DDC I^2C clock
B31	GND	P		Ground
B32	L_BKLTEN	O-CMOS		Turns power to the backlight on/off
B33	L_BKLTCTL	O-CMOS		Controls intensity of the backlight
B34	LPC_AD2	IO-LVTTL	PU 10kΩ V3.3S	LPC Bus address/data 2
B35	SMB_DATA	IO-LVTTL	PU 10kΩ V3.3A	SMBus data
B36	LPC_AD0	IO-LVTTL	PU 10kΩ V3.3S	LPC Bus address/data 0
B37	CLK_LPC_SIO	O-LVTTL	R 33.2Ω PD 10kΩ	LPC Bus clock
B38	LPC_AD3	IO-LVTTL	PU 10kΩ V3.3S	LPC Bus address/data 3
B39	LPC_AD1	IO-LVTTL	PU 10kΩ V3.3S	LPC Bus address/data 1
B40	IDE_PDD7	IO-IDE		IDE/PATA data 7
B41	GND	P		Ground
B42	IDE_PDD11	IO-IDE		IDE/PATA data 11
B43	IDE_PDD15	IO-IDE		IDE/PATA data 15
B44	IDE_PDD8	IO-IDE		IDE/PATA data8
B45	IDE_PDD13	IO-IDE		IDE/PATA data 13
B46	IDE_PDD12	IO-IDE		IDE/PATA data 12
B47	IDE_PDDREQ	IO-IDE		IDE/PATA request
B48	IDE_PDD14	IO-IDE		IDE/PATA data 14
B49	IDE_PDD10	IO-IDE		IDE/PATA data 10
B50	IDE_PDD4	IO-IDE		IDE/PATA data 4
B51	GND	P		Ground
B52	IDE_PDA1	O-LVTTL		IDE/PATA address 1
B53	GPIO4	IO-3.3		Intel ICH8M GPIO8
B54	IDE_PDDACK#	O-LVTTL		IDE/PATA acknowledge
B55	PCIE_WAKE#	I-LVTTL	PU 1kΩ V3.3A	Standard I/O device wake event
B56	RST#	O-3.3	PU 10kΩ V3.3A	System reset
B57	SMC_UART_RX	I-3.3		Maintenance port Receive
B58	L_BKLTSEL0_GPIO#	O-3.3		Selects backlight control (PWM vs. I^2C)
B59	BTN_ONOFF#	I-5	PU 10kΩ V5A	Power button input
B60	GND	P		Ground
B61	USB_PP7	IO-USB		USB 7, positive signal

Pin	Name	Type	On Module Termination	Description
B62	USB_PN7	IO-USB		USB 7, negative signal
B63	GND	P		Ground
B64	USB_PP5	IO-USB		USB 5, positive signal
B65	USB_PN5	IO-USB		USB 5, negative signal
B66	GND	P		Ground
B67	USB_PP3	IO-USB		USB 3, positive signal
B68	USB_PN3	IO-USB		USB 3, negative signal
B69	USB_OC0#	I-LVTTL	PU 10kΩ V3.3A	USB 0 over current
B70	GND	P		Ground
B71	USB_PP1	IO-USB		USB 1, positive signal
B72	USB_PN1	IO-USB		USB 1, negative signal
B73	GND	P		Ground
B74	USB_PP8	IO-USB		USB 8, positive signal
B75	USB_PN8	IO-USB		USB 8, negative signal
B76	GND	P		Ground
B77	LA_DATAP0	O-LVDS		LVDS data 0, positive signal
B78	LA_DATAN0	O-LVDS		LVDS data 0, negative signal
B79	USB_OC4#	I-LVTTL	PU 10kΩ V3.3A	USB 4 over current
B80	GND	P		Ground
B81	SATA2_T+	O-LVDS		SATA 2 transmit, positive signal
B82	SATA2_T-	O-LVDS		SATA 2 transmit, negative signal
B83	GND	P		Ground
B84	SATA2_R+	I-LVDS		SATA 2 receive, positive signal
B85	SATA2_R-	I-LVDS		SATA 2 receive, negative signal
B86	GND	P		Ground
B87	VGA_HS	O-CMOS		VGA horizontal sync
B88	VGA_VS	O-CMOS		VGA vertical sync
B89	USB_OC1#	I-LVTTL	PU 10kΩ V3.3A	USB 1 over current
B90	GND	P		Ground
B91	VGA_B	O-A		Blue data
B92	Reserved			Reserved
B93	GND	P		Ground
B94	PCIE_RXN2_SLOT0	I-PCIe		PCIe0 receive , negative signal
B95	PCIE_RXP2_SLOT0	I-PCIe		PCIe0 receive, positive signal
B96	GND	P		Ground
B97	CLK_SLOT1_OE#	I-LVTTL	R 475Ω PU 10kΩ V3.3S	PCIe 1 clock enable
B98	PCIE_TXN2_SLOT1	O-PCIe	C 0.1µF	PCIe 1 transmit, negative signal
B99	PCIE_TXP2_SLOT1	O-PCIe	C 0.1µF	PCIe 1 transmit , positive signal
B100	GND	P		Ground
B101	CLK_PCIE_SLOT1	O	R 33Ω	PCIe 1 clock, positive signal
B102	CLK_PCIE_SLOT1#	O	R 33Ω	PCIe 1 clock, negative signal
B103	Cat_LP_Detect	I-3.3	PU 10kΩ V3.3A	Indicates Catalyst LP mode (See Carrier Board Configuration)
B104	PM_EN_S0#	O-3.3	PU 10kΩ V3.3A	Power state indicator
B105	PM_EN_PWR	O-3.3	PD 15kΩ	Power state indicator
B106	SMC_UART_TX	O-3.3		Maintenance port Transmit
B107	PM_EN_S3#	O-3.3	PU 10kΩ V3.3A	Power state indicator
B108	CARRIER_I2C_SDA	IO-OD		I^2C bus data
B109	CARRIER_I2C_SCL	O-OD		I^2C bus clock
B110	GND	P		Ground

J2: Docking Connector: Power

Board connector: 2x7 socket, 1 mm, Samtec CLM-107-02-LM-D
Carrier board connector: Samtec MW-07-03-G-D-095-085, 5 mm stacking height
Samtec MW-07-03-G-D-226-065, 8 mm stacking height

The Catalyst LP receives the power input and controls for interfacing with an external power supply on this docking connector. For a description of the Catalyst LP power supply, see Power Requirements, page 24.

Pin	Name	Type	Description
1	V3.3	PI	3.3 V primary supply voltage
2	PM_CARRIER_PWRGD	I-3.3	Indicator for input power voltages
3	V3.3	PI	3.3 V primary supply voltage
4	V_BATTERY	PI	RTC backup power
5	V3.3	PI	3.3 V primary supply voltage
6	V5A	PI	5 V “always” power
7	V5S	PI	5 V normal operating power
8	V3.3A	PI	3.3 V “always” power
9	V5S	PI	5 V normal operating power
10	GND	P	Ground
11	V3.3S	PI	3.3 V normal operating power
12	GND	P	Ground
13	V3.3S	PI	3.3 V normal operating power
14	GND	P	Ground

Warning:
Disconnect the power input before removing the Catalyst LP. Removing the module from a powered carrier board may result in damage to both the carrier board and to the module.

J3: ITP Debug Port

Board connector: 24-pin FFC/FPC connector, 0.5 mm, Molex 52435-2472

Connector J3 provides an In-Target Probe (ITP) debug port for the Catalyst TC. For additional details, see Test and Debug, page 38.

System Specifications

Power

This section includes power specifications for the Catalyst LP.

Power Supply

The Catalyst LP requires the power inputs and control signals listed in the following table. For a description of the power supply, see Power Supply Architecture, page 25.

Symbol	Parameter	Min	Typ.	Max	Units
System Power Inputs (note 3)					
V3.3	Primary supply voltage	3.135	3.3	3.465	V
$I_{V3.3}$	Dual core		1.84	3.0	A
	Single core		1.67	2.5	A
V3.3A	"Always" power (note 4)	3.135	3.3	3.465	V
$I_{V3.3A}$	Dual core		0.5	0.75	A
	Single core		0.5	0.75	A
V3.3S	Normal operating power	3.135	3.3	3.465	V
$I_{V3.3S}$	Dual core		0.48	1.0	A
	Single core		0.46	1.0	A
V5A	"Always" power	4.75	5.0	5.25	V
I_{V5A}	Dual core		0	0.003	A
	Single core		0	0.003	A
V5S	Normal operating power	4.75	5.0	5.25	V
I_{V5S}	Dual core		0.84	1.7	A
	Single core		0.35	0.75	A
V_BATTERY	RTC backup power (note 5)	2.4	3.3	3.5	V
$I_{V\_BATTERY}$				10	µA
PM_CARRIER_PWRGD (note 6)					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
R_{PU}	Pull-up resistance (note 7)		10		kΩ
V_{PU}				3.3	V
PM_EN_PWR					
V_{OH}	High-level output voltage I_{OH} = -0.5 mA	2.0	3.3		V
V_{OL}	Low-level output voltage I_{OL} = 50 µA (note 8)			0.8	V
PM_EN_S0#, PM_EN_S3# (note 9)					
V_{OH}	High-level output voltage I_{OH} = -16 mA, V_{DD}=3 V	2.4	3.3		V
V_{OL}	Low-level output voltage I_{OL} = 16 mA, V_{DD}=3 V			0.4	V
BTN_ONOFF#					
V_{IH}	High-level input voltage	2.5	5		V
V_{IL}	Low-level input voltage			1.0	V
R_{PU}	Pull-up resistance (note 10)		10		kΩ
V_{PU}				5	V

Notes:

3. The maximum currents per voltage rail include peak currents and are not indicative of aggregate power consumption during normal system operation.
4. If V3.3A goes below 3.08V, the embedded controller will reset and a reset header will be displayed on the maintenance port. The reset of embedded controller results in a complete restart of module circuitry including all on-module power regulation, resets, and interface power sequence signals.
5. V_BATTERY has 1 µF of bulk decoupling capacitance, load side of diode.
6. For detailed timing requirements, see Power State Signals, page 27.
7. PM_CARRIER_PWRGD includes a pull-up resistor to V3.3A.
8. PM_EN_PWR is not actively driven low but is pulled low by a 15kΩ resistor.
9. Specifications per the SN74LVC1G00 Product Datasheet, SCES212W – March 2011, www.ti.com.
10. BTN_ONOFF# includes a pull-up resistor to V5A.

Power Consumption

Using ACPI functionality, the Catalyst LP supports multiple modes of power saving operation. Although power consumption varies based on the level of processor activity and peripheral connections, values can be estimated for typical applications. The following table lists typical power consumption estimates.

Power Mode	Parameter		V3.3	V3.3A	V3.3S	V5A	V5S	Units
S0	Full operation	Dual core	6.1	1.6	1.6	0	4.2	W
		Single core	5.5	1.6	1.5	0	1.8	W
S3	Sleep		250	500	-	15	-	mW
S5	Power down		-	500	-	15	-	mW

Performance

The Catalyst LP meets the performance specifications listed in the following table. For additional details about the processor, see Core Processor, page 15.

Parameter		Min	Typ.	Max	Units
Processor operating frequency	Dual Core			1.6	GHz
	Single Core			1.6	GHz

Electrical

This section provides electrical specifications for the Catalyst LP. For additional details about termination of individual signals, see the signal connectors in Signal Headers, page 40.

Reset Signals

The Catalyst LP includes three reset signals. For a description of these signals, see Reset Signals, page 23.

Symbol	Parameter	Min	Typ.	Max	Units
RST# (note 11)					
V_{OH}	High-level output voltage I_{OH} = -0.5 mA, V_{CC} = 3.3 V	0.9*V_{CC}	3.3		V
V_{OL}	Low-level output voltage I_{OL} = 1.5 mA, V_{CC} = 3.3 V			0.1*V_{CC}	V
R_{PU}	Pull-up resistance (note 12)		10		kΩ
V_{PU}				3.3	V
FP_RESET# (note 13)					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
R_{PU}	Pull-up resistance		10		kΩ
V_{PU}				3.3	V
H_INIT# (note 14)					
V_{IH}	High-level input voltage V_{CC} = 1.05 V	0.7*V_{CC}	1.05	V_{CC}+0.1	V
V_{IL}	Low-level input voltage V_{CC} = 1.05 V	-0.1	0	0.3*V_{CC}	V

Notes:

11. Specifications per the Intel I/O Controller Hub 8 (ICH8) Family Datasheet, May 2007 (#313056-003).
12. RST# includes a pull-up resistor to V3.3A.
13. The module includes debounce circuitry and a pull-up resistor to V3.3S. FP_RESET# will not be detected until after RST# is de-asserted.
14. Specifications per the Intel Atom Processor N400 Series Datasheet – Volume 1, Revision 002, April 2010 (#322847-002) and Intel Atom Processor D400 and D500 Series Datasheet- Volume 1, June 2010 (#322844-002).

PCIe Clock Generator

An on-module clock generator provides a PCIe clock for PCIe slot 0 and PCIe slot 1. Two additional input signals, CLK_SLOTx_OE#, individually control each reference clock. For a description of the PCIe slots, see PCI Express Bus, page 18.

Symbol	Parameter	Min	Typ.	Max	Units
CLK_PCIE_SLOT0, CLK_PCIE_SLOT1(note 15)					
F_{PCIEx_REFCLK}	Frequency		100		MHz
V_{HIGH}	Maximum output voltage			1150	mV
V_{LOW}	Minimum output voltage	-300			mV
CLK_SLOT0_OE#, CLK_SLOT1_OE#					
V_{IH}	High-level input voltage	2	3.3		V
V_{IL}	Low-level input voltage			0.8	V
R_{PU}	Pull-up resistance (note 16)		10		kΩ
V_{PU}				3.3	V

Notes:

15. The CLK_PCIE_SLOT0 and CLK_PCIE_SLOT1 signal pairs are low power differential outputs. Specifications per the IDT ICS9DBL411A Datasheet, 02/21/08 (#1250B) and IDT ICS9LPRS502 Datasheet, 02/26/09 (#1125E).
16. CLK_SLOT0_OE# and CLK_SLOT1_OE# include pull-up resistors to V3.3S.

USB

Six of the nine USB host ports, USB0-5, include over-current detection inputs. For a description of these ports, see USB, page 19.

Symbol	Parameter	Min	Typ.	Max	Units
USB_OCx#					
R_{PU}	Pull-up resistance (note 17)		10		kΩ
V_{PU}				3.3	V

Notes:

17. USB_OC0#, USB_OC1#, USB_OC2#, USB_OC3#, USB_OC4#, and USB_OC5# include pull-up resistors to V3.3A.

Carrier I^2C Bus

The Catalyst LP includes an external connection to the embedded controller I^2C bus on connector J1. For a description of this bus, see Carrier I^2C Bus, page 20.

Symbol	Parameter	Min	Typ.	Max	Units
CARRIER_I2C_SDA, CARRIER_I2C_SCL (note 18)					
$F_{CARRIER\_I2C\_CLK}$	Bus clock	100		400	kHz

Notes:

18. CARRIER_I2C_SDA and CARRIER_I2C_SCL do not include termination on the module. Include 10kΩ pull-up resistors to V3.3A on the carrier board.

SMBus

The Catalyst LP includes an external connection to the SMBus on connector J1. For a description of this bus, see System Management Bus, page 20.

Symbol	Parameter	Min	Typ.	Max	Units
SMB_CLK, SMB_DATA, SMB_ALERT#					
F_{SMB_CLK}	Bus clock	10		100	kHz
R_{PU}	Pull-up resistance (note 19)		10		kΩ
V_{PU}				3.3	V

Notes:

19. SMB_CLK, SMB_DATA, and SMB_ALERT# include pull-up resistors to V3.3A.

LVDS Display and Backlight

The Catalyst LP provides discrete signals and two serial buses to control an LCD and backlight. For a description of these signals, see LVDS Display and Backlight Control, page 21.

Symbol	Parameter	Min	Typ.	Max	Units
L_VDDEN, L_BKLTEN, L_BKLTCTL, L_BKLTSEL0_GPIO# (note 20)					
V_{OH}	High-level output voltage I_{OH} = -2 mA, V_{CC} = 3.3 V	V_{CC}-0.5		V_{CC}	V
V_{OL}	Low-level output voltage I_{OL} = 6 mA, V_{CC} = 3.3 V	0		0.4	V
L_DDC_CLK, L_DDC_DATA, L_CTLB_DATA, L_CTLA_CLK (note 20, 21)					
F_{CLK}	Bus clock			100	kHz
V_{IH}	High-level input voltage	0.7*V_{PU}		0.5+V_{PU}	V
V_{IL}	Low-level input voltage	-0.5		0.3*V_{PU}	V
V_{OL}	Low-level output voltage I_{OL} = 3 mA	0		0.4	V

Notes:

20. Specifications per the Intel Atom Processor N400 Series Datasheet – Volume 1, Revision 002, April 2010 (#322847-002), Intel Atom Processor D400 and D500 Series Datasheet- Volume 1, June 2010 (#322844-002), and Intel I/O Controller Hub 8 (ICH8) Family Datasheet, May 2007 (#313056-003).
21. L_DDC_CLK and L_DDC_DATA do not include termination on the module. Include 2.2kΩ pull-up resistors to V3.3S on the carrier board.
    L_CTLB_DATA and L_CTLA_CLK do not include termination on the module. Include 4.7kΩ pull-up resistors to V3.3S on the carrier board.

VGA Display

The Catalyst LP provides an analog RGB output to drive a VGA display and DDC serial interface for monitor Plug and Play capability. For a description of the VGA display output, see VGA Display, page 22.

Symbol	Parameter	Min	Typ.	Max	Units
VGA_R, VGA_G, VGA_B (note 22)					
R_{PD}	Pull-down resistance		150		Ω
VGA_HS, VGA_VS (note 23)					
V_{OH}	High-level output voltage I_{OH} = -8 mA	2.4		3.3	V
V_{OL}	Low-level output voltage I_{OL} = 8 mA	0		0.5	V
VGA_DDC_SDA, VGA_DDC_CLK (note 23)					
$F_{VGA\_DDC\_CLK}$	Bus clock			100	kHz
R_{PU}	Pull-up resistance (note 24)		6.81		kΩ
V_{PU}				3.3	V
V_{IH}	High-level input voltage	0.7*V_{PU}		0.5+V_{PU}	V
V_{IL}	Low-level input voltage	-0.5		0.3*V_{PU}	V
V_{OL}	Low-level output voltage I_{OL} = 3 mA	0		0.4	V

Notes:

22. The analog video signal specifications conform to the VESA Video Signal Standard Version 1, Revision 2.
23. Specifications per the Intel Atom Processor N400 Series Datasheet – Volume 1, Revision 002, April 2010 (#322847-002) and Intel Atom Processor D400 and D500 Series Datasheet- Volume 1, June 2010 (#322844-002).
24. VGA_DDC_SDA and VGA_DDC_CLK include pull-up resistors to V3.3S.

General-purpose Inputs and Outputs

The Catalyst LP provides four GPIOs. For a description of these signals, see General-Purpose Input and Output, page 23.

Symbol	Parameter	Min	Typ.	Max	Units
GPIO1, GPIO2 (note 25)					
V_{IH}	High-level input voltage	1.7	3.3		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage I_{OH} = -0.1 mA, V_{CC} = 3.3 V	V_{CC}-0.2			V
V_{OL}	Low-level output voltage I_{OL} = 0.1 mA, V_{CC} = 3.3 V			0.2	V
GPIO3 (note 26)					
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage I_{OH} = -0.5 mA, V_{CC} = 3.3 V	0.9*V_{CC}			V
V_{OL}	Low-level output voltage I_{OL} = 1.5 mA, V_{CC} = 3.3 V			0.1*V_{CC}	V
GPIO4 (note 26)					
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage I_{OH} = -0.5 mA, V_{CC} = 3.3 V	V_{CC}-0.5			V
V_{OL}	Low-level output voltage I_{OL} = 6 mA, V_{CC} = 3.3 V			0.4	V

Notes:
25. Specifications per the Altera MAX II Device Handbook, August 2009 (MII5V1-3.3).
26. Specifications per the Intel I/O Controller Hub 8 (ICH8) Family Datasheet, May 2007 (#313056-003).

Intel High Definition Audio

The Intel ICH8M supports the Intel HD Audio specification. For a description of the audio interface, see Intel High Definition Audio, page 23.

Symbol	Parameter	Min	Typ.	Max	Units
HDA (note 27)					
V_{CC}	Supply voltage		3.3		V
V_{IH}	High-level input voltage	0.65*V_{CC}			V
V_{IL}	Low-level input voltage			0.35*V_{CC}	V
V_{OH}	High-level output voltage I_{OH} = -500 µA	0.9*V_{CC}			V
V_{OL}	Low-level output voltage I_{OL} = 1500 µA			0.10*V_{CC}	V
F_{HDA_SDIx}	Data rate		24		Mbps

Note:
27. Specifications per the Intel High Definition Audio Specification Revision 1.0.

General

This section provides general specifications for the Catalyst LP.

Crystal Frequencies

Agencies certifying the Catalyst LP for compliance for radio-frequency emissions typically need to know the frequencies of on-board oscillators. The following table lists the frequencies of all crystals on the Catalyst LP.

Crystals	Device	Typ.	Units
X3	RTC	32.768	kHz
X4	Clock Generator	14.31818	MHz
X5	Embedded Controller	14.7456	MHz
X8	Ethernet Controller	25.000	MHz

Real-Time Clock

The Intel ICH8M includes a RTC function that retains the system date and time. For a description of this function, see Real-Time Clock, page 16.

Parameter	Typ.	Units
Accuracy per month @ 25°C	+/-55	sec

Environmental

The Catalyst LP is designed to meet the environmental specifications listed in the following table. Note the local ambient temperature of the module is defined by the temperatures at three key thermal design interface contact points. Temperatures at these points must not exceed the maximum temperature specified. For additional information about the thermal interface of the Catalyst LP, see Thermal Management, page 33.

Parameter	Min	Typ.	Max	Units
Commercial operating temperature	0		+70	°C
Storage temperature	-40		+85	°C
Relative humidity, non-condensing	5		95	%

Appendix A – Reference Information

Product Information

Product notices, updated drivers, support material:
www.eurotech.com

Intel

Information about the Intel products, High Definition Audio specification, and LPC bus specification:
www.intel.com

Trusted Computing Group

Trusted Computer Group specification:
www.trustedcomputinggroup.org

SATA

Serial ATA specification:
www.sata-io.org

USB

Universal Serial Bus specification:
www.usb.org

SDIO Card

SD Card Association and SDIO specification:
www.sdcard.org

MMC Card

JEDEC MMC 4.0 specification:
www.jedec.org

PCI SIG

PCI Express specification:
www.pcisig.com

I^2C Bus

I^2C bus specification and information about the general-purpose I/O ports:
www.nxp.com

SMBus

SMBus specification:
www.smbus.org

ACPI Specification

ACPI specification:
www.acpi.info

Appendix B – Board Revision

This guide applies to the current revision of the module as given in the following section.

Identifying the Board Revision

The revision number is printed on the underside of the printed wiring board. That number is 170125-100Rx. The “x” indicates the revision level of the PWB.

Board Revision History

The following is an overview of the revisions to the Catalyst LP.

Revision A

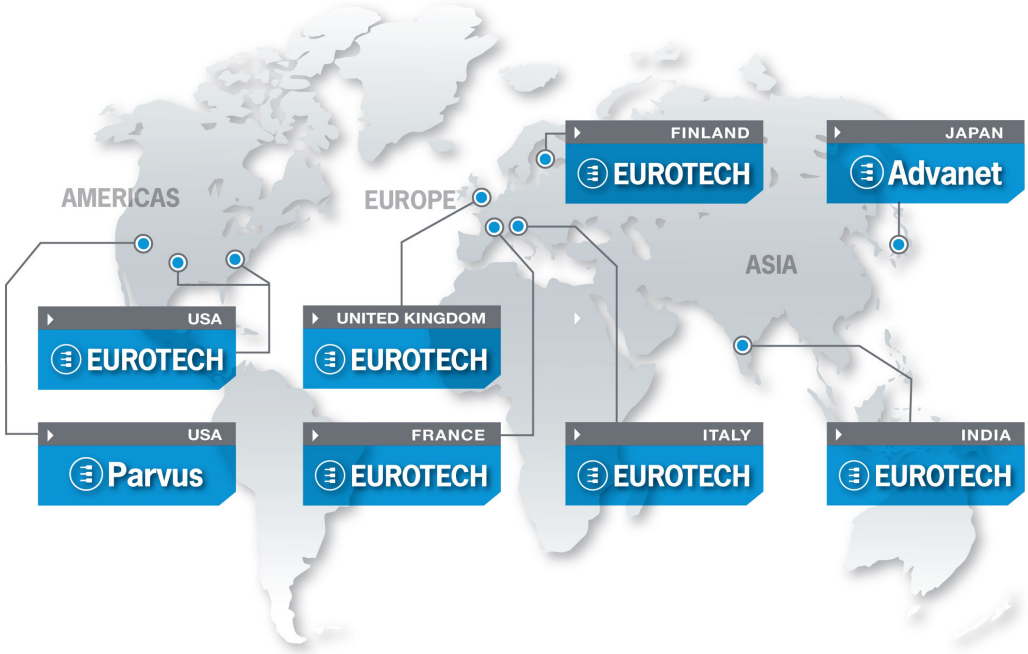
Initial release

Revision B

SATA 2 and IDE/PATA are no longer mutually exclusive. Supports SATA 1, SATA 2, and IDE/PATA.

Improved testability

Eurotech Worldwide Presence



AMERICAS

USA

EUROTECH
Toll free +1 888.941.2224
Tel. +1 301.490.4007
Fax +1 301.490.4582
E-mail: sales.us@eurotech.com
E-mail: support.us@eurotech.com
Web: www.eurotech-inc.com

PARVUS
Tel. +1 800.483.3152
Fax +1 801.483.1523
E-mail: sales@parvus.com
E-mail: tsupport@parvus.com
Web: www.parvus.com

EUROPE

Italy

EUROTECH
Tel. +39 0433.485.411
Fax +39 0433.485.499
E-mail: sales.it@eurotech.com
E-mail: support.it@eurotech.com
Web: www.eurotech.com

United Kingdom

EUROTECH
Tel. +44 (0) 1223.403410
Fax +44 (0) 1223.410457
E-mail: sales.uk@eurotech.com
E-mail: support.uk@eurotech.com
Web: www.eurotech.com

France

EUROTECH
Tel. +33 04.72.89.00.90
Fax +33 04.78.70.08.24
E-mail: sales.fr@eurotech.com
E-mail: support.fr@eurotech.com
Web: www.eurotech.com

Finland

EUROTECH
Tel. +358 9.477.888.0
Fax +358 9.477.888.99
E-mail: sales.fi@eurotech.com
E-mail: support.fi@eurotech.com
Web: www.eurotech.com

ASIA

Japan

ADVANET
Tel. +81 86.245.2861
Fax +81 86.245.2860
E-mail: sales@advanet.co.jp
E-mail: tsupport@advanet.co.jp
Web: www.advanet.co.jp

India

EUROTECH
Tel. +91 80.43.35.71.17
E-mail: sales.in@eurotech.com
E-mail: support.in@eurotech.com
Web: www.eurotech.com

To find your nearest contact refer to: www.eurotech.com/contacts

EUROTECH

www.eurotech.com

EUROTECH HEADQUARTERS
Via Fratelli Solari 3/a
33020 Amaro (Udine) – ITALY
Phone: +39 0433.485.411
Fax: +39 0433.485.499

For full contact details go to: www.eurotech.com/contacts