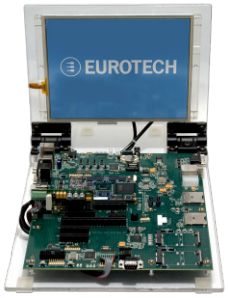
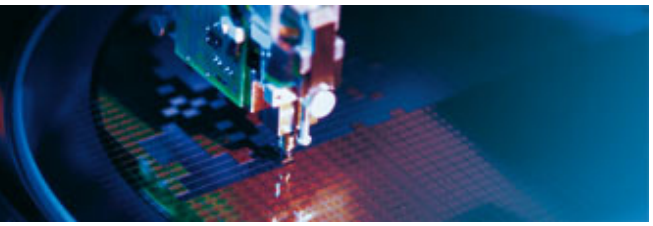
USER MANUAL





Catalyst LP

Development Kit

Rev 4 – Sept 2011 – 110125-40004

www.eurotech.com

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Trademarks

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Document Revision History

REVISION	DESCRIPTION	DATE
2	Preliminary release	Aug 2010
3	Appendix D removed	Oct 2010
4	Initial release	Sept 2011

Table of Contents

Important User Information

In order to lower the risk of personal injury, electric shock, fire, or equipment damage, users must observe the following precautions as well as good technical judgment, whenever this product is installed or used.

All reasonable efforts have been made to ensure the accuracy of this document; however, Eurotech assumes no liability resulting from any error/omission in this document or from the use of the information contained herein.

Eurotech reserves the right to revise this document and to change its contents at any time without obligation to notify any person of such revision or changes.

Safety Notices and Warnings

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Eurotech assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Eurotech is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Installation in Enclosures

In the event that the product is placed within an enclosure, together with other heat generating equipment, ensure proper ventilation.

Do Not Operate in an Explosive Atmosphere

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Alerts that can be found throughout this manual

The following alerts are used within this manual and indicate potentially dangerous situations.

Danger, electrical shock hazard:
Information regarding potential electrical shock hazards:

- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Warning:
Information regarding potential hazards:

- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Information and/or Notes:
These will highlight important features or instructions that should be observed.

Use an Appropriate Power Supply

- Only start the product with a power supply that conforms to the voltage requirements as specified in Power Supply, page 52. In case of uncertainty about the required power supply, please contact your local Eurotech Technical Support Team.
- Use power supplies that are compliant with SELV regulation.
- Use certified power cables. The power cable must fit the product, the voltage, and the required current. Position cable with care. Avoid positioning cables in places where they may be trampled on or compressed by objects placed on it. Take particular care of the plug, power-point, and outlet of power cable.
- Avoid overcharging power-points.

Antistatic Precautions

To avoid damage caused by ESD (Electro Static Discharge), always use appropriate antistatic precautions when handing any electronic equipment.

Life Support Policy

Eurotech products are not authorized for use as critical components in life support devices or systems without the express written approval of Eurotech.

Warranty

For Warranty terms and conditions users should contact their local Eurotech Sales Office.

See Eurotech Worldwide Presence, page 61 for full contact details.

WEEE

The information below is issued in compliance with the regulations as set out in the 2002/96/EC directive, subsequently superseded by 2003/108/EC. It refers to electrical and electronic equipment and the waste management of such products. When disposing of a device, including all of its components, subassemblies, and materials that are an integral part of the product, you should consider the WEEE directive.

This device is marketed after August 13, 2005 and you must separate all of its components when possible and dispose of them in accordance with local waste disposal legislations.

- Because of the substances present in the equipment, improper use or disposal of the refuse can cause damage to human health and to the environment.
- With reference to WEEE, it is compulsory not to dispose of the equipment with normal urban refuse and arrangements should be instigated for separate collection and disposal.
- Contact your local waste collection body for more detailed recycling information.
- In case of illicit disposal, sanctions will be levied on transgressors.

RoHS

This device, including all it components, subassemblies and the consumable materials that are an integral part of the product, has been manufactured in compliance with the European directive 2002/95/EC known as the RoHS directive (Restrictions on the use of certain Hazardous Substances). This directive targets the reduction of certain hazardous substances previously used in electrical and electronic equipment (EEE).

Technical Assistance

If you have any technical questions, cannot isolate a problem with your device, or have any enquiry about repair and returns policies, contact your local Eurotech Technical Support Team.

See Eurotech Worldwide Presence, page 61 for full contact details.

Transportation

When transporting any module or system, for any reason, it should be packed using anti-static material and placed in a sturdy box with enough packing material to adequately cushion it.

Warning:
Any product returned to Eurotech that is damaged due to inappropriate packaging will not be covered by the warranty.

Conventions

The following table describes the conventions for signal names used in this document.

Convention	Explanation
GND	Digital ground plane
#	Active low signal
+ or P	Positive signal in differential pair
- or N	Negative signal in differential pair

The following table describes the abbreviations for direction and electrical characteristics of a signal used in this document.

Type	Explanation
I	Signal is an input to the system
O	Signal is an output from the system
IO	Signal may be input or output
P	Power and ground
A	Analog signal
OD	Open-drain
CMOS	3.3 V CMOS
LVCMOS	1.05 V CMOS
LVTTL	Low Voltage TTL
3.3	3.3 V signal level
5	5 V signal level
IDE	5 V tolerant signal
HDA	High Definition Audio, 3.3 V (default) or 1.5 V signal
LVDS	Low Voltage Differential Signalling
PCIe	PCI Express signal
NC	No Connection
Reserved	Use is reserved to Eurotech

Some signals include termination on the Catalyst LP or carrier board. The following table describes the abbreviations that specify the signal termination.

Termination	Explanation
PU	Pull-up resistor to the specified voltage
PD	Pull-down resistor
R	Series resistor
C	Series capacitor

Product Overview

The Catalyst LP Development Kit provides a development platform for the Catalyst LP and a reference for custom carrier board design. The kit consists of the following components:

- Catalyst LP with Intel® Atom™ processor D510, dual core (finned heat sink, CTLP1007) or Catalyst LP with Intel® Atom™ processor N450, single core (x-shaped heat sink, CTLP1008)
- Catalyst LP Development Kit carrier board
- 10.4-inch TFT LCD with SVGA resolution (800 x 600, 6-bit color) and cable
- CCFL backlight inverter and cable
- 4-wire resistive touch panel and cable
- Catalyst Module Display Adapter
- CompactFlash card loaded with Windows® Embedded Standard or Wind River Linux (future option)
- FreeDOS USB flash drive for BIOS updates
- 12 VDC adapter and AC cord
- DB9FF cable (for maintenance port P2 only)
- Plexiglas mounting
- Stylus and screen cleaning cloth

Please make sure you have received all the components before you begin your development. For details about getting started, refer to the *Catalyst LP Development Kit Quick Start (Eurotech document #110125-4001)*.

As a development platform, this kit allows you to become familiar with the Catalyst LP functionality prior to customization for your specific application. Utilize the development kit to validate your proposed design for both software and hardware. For example, if a USB device is to be used on USB port 0, test that device by connecting it to USB port 0 on the development kit running your application. This type of testing also allows you to validate your operating system image with all required drivers loaded.

To provide flexibility and allow development across a broad spectrum of end-use applications, the Catalyst LP Development Kit carrier board maximizes the Catalyst LP functionality and implements many industry-standard interfaces. This configuration provides a valuable reference for your application-specific carrier board. Use Eurotech's carrier board as a starting point for your design. Using the same connectivity to the module and the same components will minimize the time spent in debugging your new design.

In addition to the Catalyst LP Development Kit, Eurotech provides a variety of services to ensure that your Catalyst LP-based product is up and running from the first prototype release. Stay in contact with your sales and support representatives throughout your development cycle to ensure a complete and robust solution with which to move forward.

Block Diagram

The following diagram illustrates the system organization of the Catalyst LP Development Kit. Notice that the data connector has been divided into two sections for this illustration. Functionality provided by the Catalyst LP is included in the dark blue section, while functionality provided by the carrier board is included in the light blue-gray section. Dotted lines indicate options.

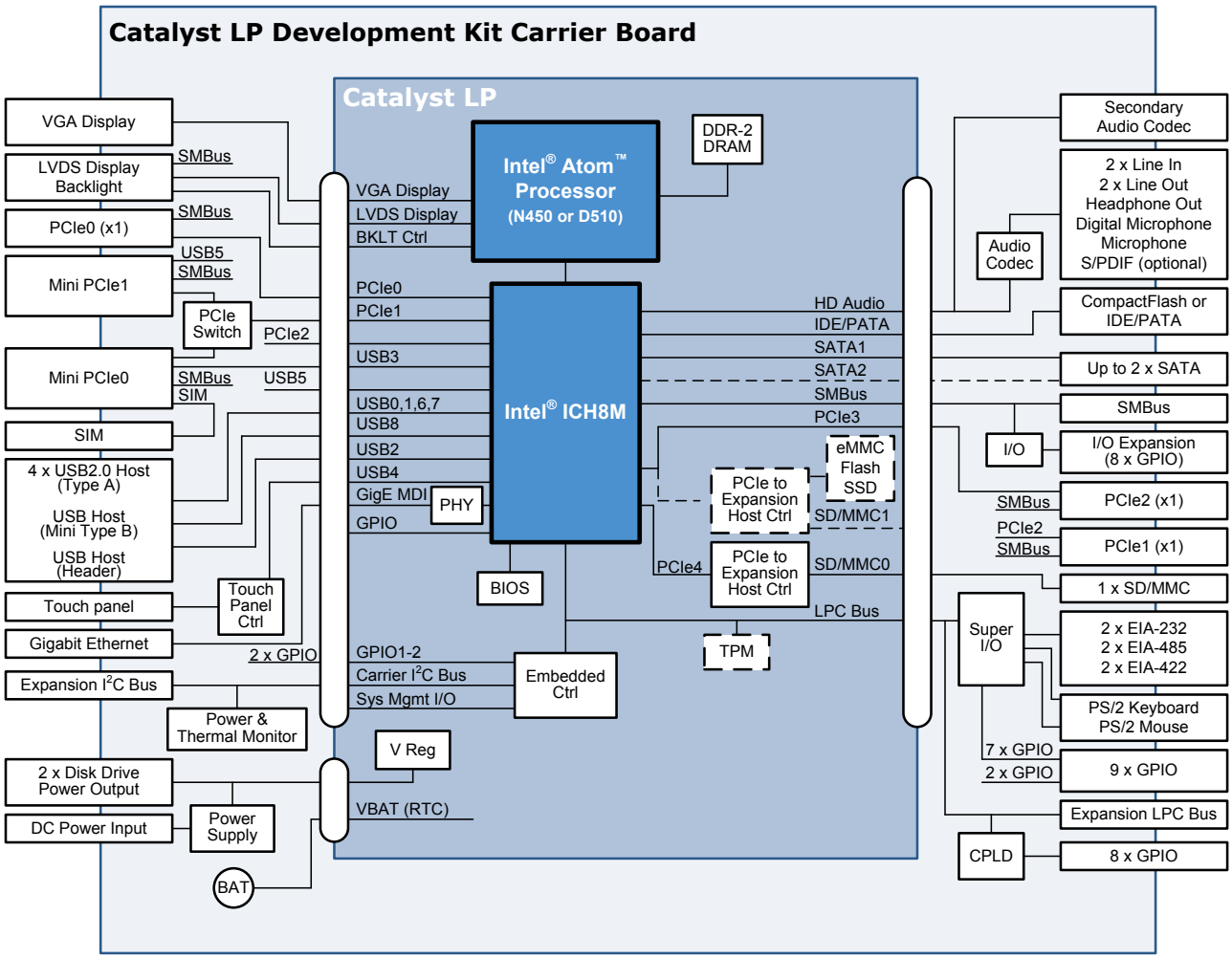


Figure 1. Catalyst LP Development Kit Block Diagram

Features

Processor

- Intel® Atom™ processor N450 (single core) or Intel® Atom™ processor D510 (dual core)
- 200 MHz graphics engine (single core) or 400 MHz graphics engine (dual core)
- Intel® I/O Controller Hub (Intel® ICH8M)

Integrated System Functions

- Embedded Controller
- Optional Trusted Platform Management (Contact Eurotech for details)

Memory

- Up to 2 GB DDR-2 DRAM
- Optional on-board eMMC flash SSD (Contact Eurotech for details)
- Integrated system BIOS
- Battery-backed real-time clock
- External memory support
  - IDE/PATA disk drive or CompactFlash card
  - SATA disk drive
  - USB disk drive
  - SD/MMC card
  - PCI Express or Mini PCI Express card

Communications

- Up to three PCI Express one lane (PCIe x 1) slots
  - Custom configuration option for one PCI Express four lane and two PCI Express one lane slots
- Two Mini PCI Express slots (PCIe, SMBus, USB)
- Six USB 2.0 ports operating at low, full, and high speeds
  - Four host ports (USB Type A)
  - One host port (Mini USB Type B)
  - One host port (Header)
- Six serial ports
  - Two EIA-232, 9-wire
  - Two EIA-422
  - Two EIA-485
- Gigabit Ethernet
- I^2C bus with I^2C master device
- System Management Bus

User Interface and Display

- Two independent display outputs
  - LVDS display
  - VGA display
- Catalyst Module Display Adapter
- 10.4-inch TFT LCD with SVGA resolution (800 x 600, 6-bit color)
- CCFL backlight inverter with control signals for intensity and on/off
- Resistive touch panel (4-, 5-, or 8-wire options)
- PS/2 keyboard and mouse support

Inputs and Outputs

- Low Pin Count bus for general-purpose I/O expansion
- Twenty five general-purpose inputs and outputs

Audio Interface

- Intel® High Definition Audio compatible codec
  - Two stereo line inputs
  - Two stereo line outputs
  - Stereo headphone output
  - Stereo microphone input
  - Digital microphone input
  - S/PDIF output (optional)
- Secondary audio codec expansion support

Power Supply

- 100-240 VAC power adapter supplying 12 V main power input
- Two auxiliary power output for external peripheral devices
- ACPI power management
- Real-time power monitoring

Carrier Board Detection

The Catalyst LP conforms to the same footprint as other Eurotech Catalyst modules. However, the modules are not pin-compatible. Each module has a unique pinout on connector J1 providing different feature sets. When installed in a carrier board, the Catalyst LP reads the input signal Cat_LP_Detect (J1 pin B103) to determine the configuration of the carrier board. Do not connect this input on the carrier board.

Warning:

Install Catalyst LP modules or other compatible modules only in carrier boards designed for the Catalyst LP. Installing incompatible modules may result in damage to the carrier board and module.

If the Cat_LP_Detect input is connected incorrectly on the carrier board, the Catalyst LP will not boot.

For full details about compatibility between modules, see the technical bulletin for your module.

Related Documents

This manual describes how the Catalyst LP integrates with Eurotech's carrier board to provide a development platform and reference design for your specific application. It complements the information provided in the *Catalyst LP Design-In Guide* and is intended for software application developers, system integrators, and hardware design engineers.

The following documents are also important resources for developing applications for the Catalyst LP.

Document	
Catalyst LP Design-In Guide	110125-1000
Catalyst XL - Catalyst LP Compatibility Technical Bulletin	110125-1001
Catalyst LP Development Kit Quick Start	110125-4001
Catalyst Module Display Adapter User Manual	110122-4000
Catalyst Module Installation and Removal	110122-2014
Catalyst System Management Programmer Reference	110122-2021
Catalyst SMBus Programmer Reference	110122-2022
Catalyst I2C Bus Programmer Reference	110122-2023

Table 1. Related Documents

Check the Eurotech support site (http://support.eurotech-inc.com/) for errata reports and for the latest releases of these documents.

Software Specifications

Eurotech provides an application-ready platform including BIOS, operating system, and development environment. This section gives a brief description of the software support available for the Catalyst LP Development Kit. For additional details, contact your local Eurotech representative.

Operating System Support

The Catalyst LP Development Kit is compatible with the following operating systems:

- Windows® Embedded Standard
- Wind River Linux 3.0 (future option)
- Select real-time operating systems

For details about available support of each operating system, contact your local Eurotech representative.

BIOS

The Catalyst LP incorporates a custom system BIOS developed by Eurotech.

Software Development Kit

Eurotech has developed a Software Development Kit (SDK) and its Application Programming Interface (API) for the following functions:

- System Management
- SMBus
- I^2C bus

For details about the availability of these SDKs, contact your local Eurotech representative.

Everyware™ Software Framework

Everyware Software Framework (ESF) is an inclusive software framework that puts a middleware layer between the operating system and the OEM application. It provides industry-standard interfaces that shorten development time, simplify coding, and allow software to be ported from one Eurotech hardware platform to another. ESF is a future option for the Catalyst LP. If your application requires ESF, contact your local Eurotech representative.

Information about ESF is available at http://esf.eurotech.com.

Hardware Specifications

Core Processor

The Catalyst LP provides the processing power on the development kit. This high-performance module is based on the Intel Atom processor N450 (single core) or Intel Atom processor D510 (dual core). The following sections describe how the features of the Catalyst LP work in conjunction with the carrier board to provide a complete out-of-the-box development platform. For a detailed description of the Catalyst LP, refer to the *Catalyst LP Design-In Guide (Eurotech document #110125-1000)*.

Memory

The Catalyst LP combined with a carrier board provides a variety of storage capabilities. The following sections describe the different types of memory supported by the Catalyst LP Development Kit.

Synchronous DRAM

Double Data Rate Synchronous DRAM (DDR-2) is used on the Catalyst LP for system main memory and frame buffer memory. Options up to 2 GB are available. The Intel Atom processor supports unified memory architecture in which the integrated 2D/3D graphics controller memory is “unified” with the system main memory. The default frame buffer is 4 MB with options in the BIOS Setup for selecting an 8 MB option. Extended graphics memory space is available up to 256 MB. The graphics driver controls this size based on usage.

Flash SSD (option)

The Catalyst LP supports an optional on-module eMMC flash SSD. An 8 GB option is available in the standard module configuration. Options of 16 GB and 32 GB are available as custom module configurations. In addition to providing mass storage, this memory is a system boot option.

Notes:
The eMMC flash SSD option on the Catalyst LP and PCIe 2 on socket J15 of the carrier board are mutually exclusive. If your module includes the eMMC flash SSD, the PCIe slot is no longer available on socket J15.

Non-Volatile Memory

The Catalyst LP includes non-volatile memory for system BIOS storage and a real-time clock (RTC) functionality.

BIOS and Configuration Data

A serial interface flash memory device stores the BIOS boot firmware, BIOS Setup settings, and module configuration data on the Catalyst LP. Standard configuration is 2 MB. The flash memory device connects to the Intel ICH8M using a serial peripheral interface (SPI).

Real-Time Clock

The Catalyst LP includes a RTC function to retain the system date and time when the system is powered down as long as the 3.3 V “always” power or backup power is provided to the module. To supply backup power, the carrier board includes a long-life 3 V battery. For further details, see Real-Time Clock, page 56.

External Memory Interfaces

Seven types of external memory interfaces provide mass storage options on the Catalyst LP Development Kit. The carrier board includes a CompactFlash socket, an IDE/PATA header, two SATA ports, four USB host ports, an SD/MMC socket, up to three PCIe sockets, and two Mini PCIe sockets that can connect external memory to the system.

For additional details about the signals provided by the Catalyst LP, including specific routing guidelines and design constraints, refer to the *Catalyst LP Design-In Guide (Eurotech document #110125-1000)*.

CompactFlash® Card or IDE/PATA Disk Drive

The carrier board supports a CompactFlash (CF) card in socket J71, page 48 or a 2.5-inch IDE/PATA magnetic or solid-state disk drive on header J8, page 33. Both media provide mass storage in a wide variety of capacities and are a cost-effective means to expand system storage.

See the following section for limitations of using SATA disk drives with a CF card or an IDE/PATA disk drive.

SATA Disk Drive

Two serial ATA (SATA) buses on header J67, page 47, and header J68, page 47 provide the option to add high-capacity, removable storage SATA disk drives to the development kit. These buses support the Serial ATA Specification, Revision 2.5 with data transfer rates of up to 3.0 Gbps.

Notes:
Development kits using a Catalyst LP revision A module support up to two SATA ports. SATA 2 on header J68 and the CF card slot J71 or IDE/PATA header J8 are mutually exclusive. If your application uses a CF card or IDE/PATA disk drive, only SATA 1 on header J67 is supported.

Development kits using a Catalyst LP revision B module support SATA 1, SATA 2, and IDE/PATA.

USB Mass Storage Device

A USB mass storage device can connect to one of two dual USB sockets on the carrier board: J3, page 32 and J4, page 32. For a description of these ports, see USB, page 17.

SD Cards

The carrier board includes a Secure Digital and MultiMediaCard (SD/MMC) socket J51, page 43 for memory and I/O expansion.

This SD/MMC interface is compliant with the following specifications:

- SD Spec. Part 1 Physical Layer Spec. Version 3.00
- SD Spec. Part A2 SD Host Controller Standard Spec. Version 2.00
- Compliant with SD Spec. Part E1 SDIO Spec. Version 2.00
- Compliant with SD Spec. Part 2 File System Spec. Version 2.00
- Compliant with MultiMediaCard System Spec. Version 4.2

PCIe or Mini PCIe Memory Card

A PCIe x1 or Mini PCIe memory card can provide additional memory on the development kit. Three PCIe sockets and two Mini PCIe sockets are available on the carrier board. For a description of the PCI Express capability, see PCI Express, page 17.

Communications

The Catalyst LP Development Kit implements several industry-standard channels for communication allowing development across a broad spectrum of end-use applications. These include PCIe, Mini PCIe, USB, serial, Gigabit Ethernet, I^2C bus, and SMBus. The following sections describe these interfaces.

For additional details about the signals provided by the Catalyst LP, including specific routing guidelines and design constraints, refer to the *Catalyst LP Design-In Guide (Eurotech document #110125-1000)*.

PCI Express

A key capability of the Catalyst LP Development Kit is its PCI Express (PCIe) connectivity. The carrier board provides up to three PCI Express sockets and two Mini PCIe sockets. Each slot is compliant with the PCI Express Base Spec. Revision 1.1 supporting 2.5 Gbps bandwidth in each direction.

The three PCIe sockets connect directly to the Catalyst LP, while the two Mini PCIe sockets route through a PEX 8505 PCIe switch located on the carrier board. The PLX Technology PEX 8505 is a 5-lane, 5-port PCIe switch. This switch connects directly to the Catalyst LP and provides up to four additional PCIe ports on the carrier board. The following table describes the PCIe connectivity on the carrier board.

Carrier Board Connector	Carrier Board PCIe Slot	Catalyst LP PCIe Slot	Intel ICH8M PCIe Port	PCIe Switch Port
J12	PCIe 0	0	1	
	(PCIe Switch)	1	2	
J14	PCIe 1	2	3	
J15	PCIe 2	3	4	
J16	Mini PCIe 0			3
J17	Mini PCIe 1			4

Table 2. PCI Express Connectivity

Notes:
PCIe 2 on J15 of the carrier board and the eMMC flash SSD option on the Catalyst LP are mutually exclusive. If your module includes the eMMC flash SSD, PCIe is no longer available on socket J15.

As a custom configuration, the four PCIe slots provided by the Catalyst LP connect directly to socket J12 supporting a PCI Express four lane (PCIe x4) slot. In this configuration, the PCIe switch connects to the LAN interface signals of the Catalyst LP. PCIe 1 on socket J14, PCIe 2 on socket J15, and the two Mini PCIe slots connect to the PCIe switch.

USB

The Catalyst LP Development Kit includes eight Universal Serial Bus (USB) host ports. These ports support the USB 2.0 specification operating at high speed (480 Mbps), full (12 Mbps), and low (1.5 Mbps) speeds. The following table describes the mapping of the Catalyst LP USB ports on the module and the carrier board.

Carrier Board Connector	Carrier Board USB Port	Catalyst TC USB Port	Intel ICH8M USB Port
J3 A	Host 0	0	0
J3 B	Host 1	1	1
J6	Host 2	2	2
J16 (Mini PCIe 0)	Host 3	3	3
	(Touch Panel Controller)	4	4
J17 (Mini PCIe 1)	Host 5	5	5
J4 A	Host 6	6	6
J4 B	Host 7	7	7
J62	Host 8	8	9

Table 3. USB Port Connectivity

The carrier board includes connectors and support circuitry including power switch, current limiter circuit, common mode chokes, and over-current protection for the USB host ports on J3, J4, and J6. The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The development kit supplies 5 V power to each USB host port through a power switch with over-current detection. Any USB client device that has USB drivers installed on the Catalyst LP can connect directly to the system using these sockets. For electrical specifications, see USB, page 52.

The USB host port signals on J16, J17, and J62 route directly from the Catalyst LP to the connectors on the carrier board. The carrier board does not include additional support circuitry for these USB host ports.

Gigabit Ethernet

For direct network connectivity, the Catalyst LP Development Kit provides a Gigabit Ethernet connection that conforms to the IEEE 802.3 standard for 10Base-T, 100Base-TX, and 1000Base-T applications. On the Catalyst LP, the Intel ICH8M includes a Gigabit Ethernet Controller. This device connects to an Intel® 82567 Gigabit Ethernet Physical Layer Transceiver located on the module, supporting a Media Dependent Interface (MDI). In addition, this transceiver drives three programmable LED control signals which are available to the carrier board. For information about this device, refer to www.intel.com.

The MDI provided by the Catalyst LP routes directly to RJ-45 socket J63, page 46 located on the carrier board. This RJ-45 socket includes built-in magnetics, integrated termination (75 Ω resistors to the center tap voltage on the MDI pins), and two Ethernet LEDs, page 31.

Carrier I²C Bus

I²C (Inter-IC) bus is a multi-master, "two-wire" synchronous serial bus for communications between integrated circuits (ICs) and for addressing peripherals in a system. The development kit includes an I²C bus with the Catalyst LP acting as the bus master. The following diagram illustrates the I²C architecture on the Catalyst LP Development Kit.

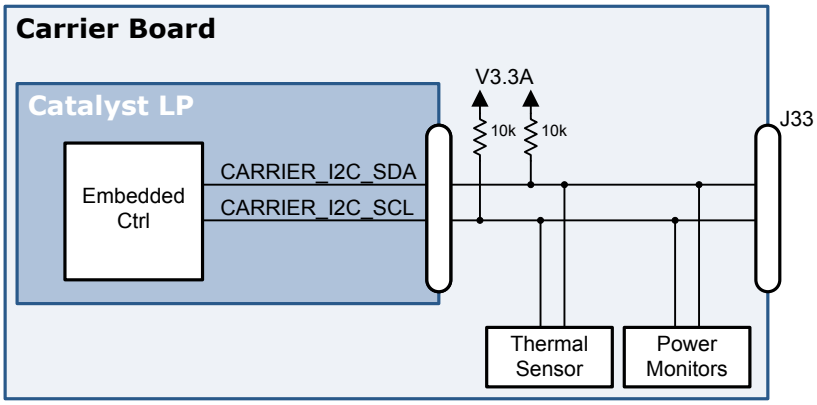


Figure 2. I²C Bus Architecture

The carrier board provides termination on the carrier I²C bus and an external connection on header J33, page 40. Power all devices connected to this bus using the 3.3 V “Always” (V3.3A) power or isolate the devices from the bus when powered off. When possible, use the SMBus to communicate with devices on the carrier board instead of the carrier I²C bus. For electrical specifications, see Carrier I²C Bus, page 52.

A thermal sensor and power monitors, also located on the carrier board, connect to the carrier I²C bus and provide hardware monitoring. For additional details, see System Monitoring, page 23.

The following table lists the addresses of the I²C devices on the carrier board.

Module Device	Address	Function
Thermal Sensor	1001 0000 1001 0001	Write Read
V3.3 Power Monitor	1000 0000 1000 0001	Write Read
V5S Power Monitor	1000 0010 1000 0011	Write Read
V3.3S Power Monitor	1000 1000 1000 1001	Write Read
V5A Power Monitor	1000 1010 1000 1011	Write Read
V3.3A Power Monitor	1000 1100 1000 1101	Write Read

Table 4. I²C Bus Addresses

System Management Bus

System Management Bus (SMBus) follows the same operating principles as I²C. Similar to I²C, SMBus is a "two-wire" interface allowing multiple devices to communicate with each other. The development kit includes a SMBus supporting the SMBus 2.0 Specification with hardware alerting on the SMBus using the I/O signal SMB_ALERT#. The Intel ICH8M on the Catalyst LP acts as bus master.

The following diagram illustrates the SMBus architecture on the development kit.

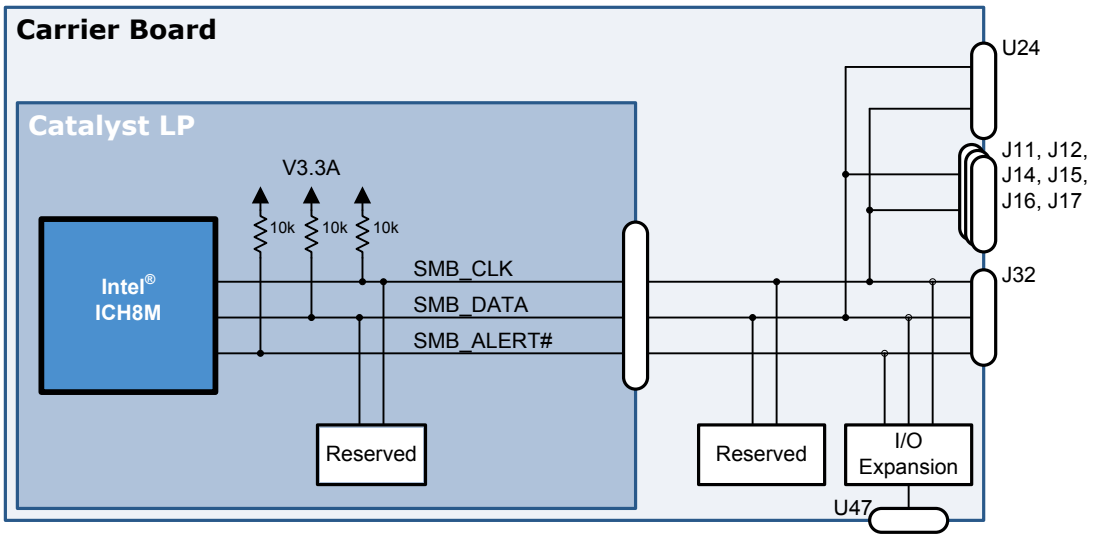


Figure 3. SMBus Architecture

The carrier board provides an external connection to the SMBus on header J32, page 40. Power all devices connected to this bus using the V3.3A power or isolate the devices from the bus when powered off. For electrical specifications, see SMBus, page 53.

Notes:
SMBus is not compatible with all I²C devices. Review the device data sheet carefully before connecting an I²C device to the SMBus.

The following table lists the addresses of the SMBus devices on the Catalyst LP and the carrier board.

Module Device	Address	Function
Catalyst LP		
Reserved	1101 0010 1101 0011	Write Read
Carrier Board		
I/O Expansion	0100 0000 0100 0001	Write Read
Reserved	1101 0100 1101 0101	Write Read

Table 5. SMBus Addresses

Serial Ports

The carrier board includes a Super I/O Controller that is connected to the Catalyst LP using the LPC Bus. This device provides six serial ports for general-purpose serial communication as described in the following table.

Carrier Board Connector	Carrier Board Serial Port	Super I/O Controller Serial Port	Communication
P1 A	Serial 1	1	EIA-232, 9-wire
J40	Serial 2	2	EIA-422
P1 B	Serial 3	3	EIA-232, 9-wire
J38	Serial 4	4	EIA-485
J39	Serial 5	5	EIA-422
J37	Serial 6	6	EIA-485

Table 6. Super IO Controller Serial Ports

Display and User Interface

The Catalyst LP Development Kit is a complete out-of-the-box development platform including a display subsystem and a VGA output for a secondary display. The display subsystem consists of the following components:

- 10.4-inch TFT LCD with SVGA resolution (800 x 600, 6-bit color) and cable
- 4-wire resistive touch panel and cable
- CCFL backlight inverter and cable
- Catalyst Module Display Adapter
- Display cable

The following sections provide an overview of the display subsystem. For a complete description, refer to the *Catalyst Module Display Adapter User Manual (Eurotech document #110122-4000)*.

LVDS Display and Backlight Control

The display is driven by an LVDS display output from the Catalyst LP, in conjunction with the Catalyst Module Display Adapter. This output consists of three LVDS data pairs, as well as an LVDS pixel clock, supporting 18-bit color. Additional signals from the module include the discrete signal L_VDDEN that controls power to the display and an I^2C bus (L_DDC_DATA, L_DDC_CLK) for communication with the LCD Display Data Channel (DDC).

To control the display subsystem's backlight inverter, the Catalyst LP drives three backlight control signals and an I^2C bus (L_CTLB_DATA, L_CTLA_CLK) for communication with the backlight. The following table describes the backlight control signals.

Signal	J11 Pin	Type	Description
L_BKLTCTL	A26	O	Controls the intensity of the backlight
L_BKLTEN	A29	O	Turns power to the backlight on or off
L_BKLTSEL	A25	O	Selects backlight control (PWM vs. I2C)

Table 7. Backlight Control Signals

The LVDS display output and backlight control signals are provided on socket J11, page 33 on the carrier board. This Eurotech-specific socket mates with the Catalyst Module Display Adapter and provides an interface between the carrier board and display subsystem.

User Interface

Touch Panel Controller

To drive the resistive touch panel, the carrier board includes a USB touch panel controller and separate analog multiplexer. This circuitry supports 4-, 5-, and 8-wire resistive touch panels. The pinout for header J26, page 38 easily interfaces to 4- and 5-wire touch panels, while the pinout for header J27, page 38 is suited for 8-wire touch panels. Standard Catalyst LP Development Kits include a 4-wire touch panel. The touch panel signals are routed from header J27 on the carrier board through the Catalyst Module Display Adapter to the touch panel. For electrical specifications, see Touch Panel Controller, page 53.

Carrier Board PS/2 Support

The carrier board supports a direct connection to a PS/2 mouse and keyboard using the dedicated keyboard/mouse interface of the Super I/O Controller. Connect these devices to socket J34, page 40.

Catalyst Module Display Adapter

The Catalyst Module Display Adapter (display adapter) is a custom board that provides the interface between the Catalyst LP and the LVDS display, touch panel, and backlight inverter. Its card edge connector mates to the Eurotech-specific socket J11 on the carrier board. An LVDS buffer/repeater with configurable pre-emphasis is included on the display adapter to boost the data and pixel clock signals from the Catalyst LP enabling transmission over the display cable. The maximum cable length is 24 inches for controlled impedance cables that target 97 Ω. ± 20%. The display cable should not introduce major impedance discontinuities that cause signal reflections.

In addition, the adapter includes an on-board power switch and fuse control power to the display, 2.2kΩ pull-up resistors to V3.3S on the LCD DDC I^2C bus (L_DDC_CLK and L_DDC_DATA), and 4.7kΩ pull-up resistors to V3.3S on the Backlight I^2C bus (L_CTLA_CLK and L_CTLB_DATA). For a complete description, refer to the *Catalyst Module Display Adapter User Manual (Eurotech document #110122-4000)*.

VGA Display

As a secondary display option, the Catalyst LP Development Kit provides a direct connection to a VGA display on J61, page 45. This output provides red, green, and blue data, as well as horizontal sync and vertical sync signals. The carrier board includes termination, output filters, and buffers for the VGA display signals. The following table summarizes the VGA display output capabilities.

Feature	Description
Resolution	Dual core: Up to 2048 x 1536 x 32 bpp at 60 Hz Single core: Up to 1400 x 1050 x 32 bpp at 60 Hz

Table 8. VGA Display Capabilities

In addition, socket J61 provides a Display Data Channel (DDC) serial interface for monitor Plug and Play capability with various computer displays. For electrical specifications, see VGA Output, page 54.

Inputs and Outputs

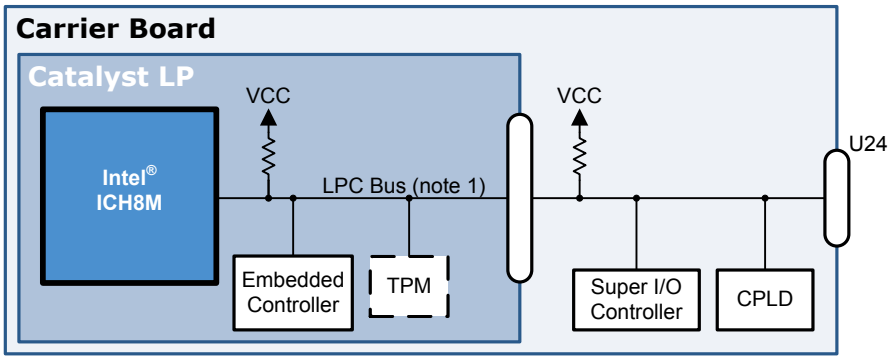
Several signals on the Catalyst LP Development Kit support I/O expansion and system management. The Catalyst LP provides a Low Pin Count bus supporting legacy I/O capabilities and GPIO; while the carrier board includes a Super I/O Controller on the LPC bus and additional GPIO.

For additional details about the signals provided by the Catalyst LP, including specific routing guidelines and design constraints, refer to the *Catalyst LP Design-In Guide (Eurotech document #110125-1000)*.

Low Pin Count Bus

In response to the transition from ISA-based systems, the Low Pin Count (LPC) bus provides a migration path for legacy I/O capabilities. This bus enables general-purpose I/O expansion and provides communication to low-bandwidth devices. For this purpose, the Catalyst LP Development Kit supplies a LPC bus supporting the Low Pin Count Interface Specification, Revision 1.1. On the Catalyst LP, this bus connects to the Intel ICH8M, the embedded controller, and an optional TPM. On the carrier board, the LPC bus provides general-purpose expansion and connects to a CPLD and Super I/O Controller. The LPC bus signals are available externally on U24, page 50.

The following diagram illustrates the LPC bus architecture on the development kit.



Note:

1. For details about the termination on individual signals of the LPC bus, refer to the Catalyst LP Design-In Guide (Eurotech document #110125-1000) and U24, page 50.

Figure 4. LPC Bus Architecture

Reset Signals

Two signals, BUF_RST# and SWX_RESET#, force a hard reset of the Catalyst LP Development Kit. The carrier board buffers the system reset (RST#, J1 B56) from the Catalyst LP and uses this buffered signal, BUF_RST#, to reset all devices on the carrier board and several external peripherals. BUF_RST# acts as a power-on reset forcing a complete system hardware reset and ensuring proper reset timing and logic synchronization. BUF_RST# is available on J11, page 33, J12, page 35, J14, page 35, J15, page 35, J16, page 35, J17, page 35, and U24, page 50.

The input signal SWX_RESET# connects to the on-board reset switch SW1, page 29 and is also available on header J55, page 45 for connection to an external switch. This signal drives the Catalyst LP front panel reset input (FP_RESET#, J1 A59). The FP_RESET# signal initiates a hardware reset including the Intel Atom processor and Intel ICH8M. However, do not use this signal as a power-on reset. For electrical specifications, see Reset Signals, page 53.

General-Purpose Inputs and Outputs

The Catalyst LP Development Kit includes twenty five GPIO signals. The following table describes the GPIO signals. For electrical specifications, see General-purpose Inputs and Outputs, page 54.

Header	# of GPIO	Device
U27	2	Embedded controller
	7	Super I/O Controller
U47	8	I/O expansion port
J64	8	CPLD

Table 9. General-Purpose Inputs and Outputs

The I/O expansion port on header U47 is implemented by a NXP PCA9554 device and is software-controlled using the SMBus. The GPIO are programmed as inputs at power up. For the SMBus address, see System Management Bus, page 19.

Carrier Board Super I/O Controller

On the carrier board., a Super I/O Controller connects to the LPC bus and provides system I/O control. This device's runtime registers control various discrete I/O on the carrier board. For detailed information about the control of the Super I/O Controller including a memory map, refer to the SMSC SCH3116 datasheet available at www.smsc.com. The following table lists the controls that are specific to the Catalyst LP Development Kit.

GPIO	Name	Type	Description
GP30	LVDS_PRESENT#	I	Indicates that the display adapter is installed in J11
GP34	SLOT1_PRESENT	I	Indicates that a card is installed in J14
GP36	H_INIT#	O	Initiates a soft reset of the module. (For details, contact Eurotech.)
GP37	SLOT2_PRESENT	I	Indicates that a card is installed in J15
GP40	IDE_PATADET	I	Indicates 40 or 80 conductor IDE cable
GP42	PCIE_WAKE#	I	Supports WAKE# functionality
GP60	SLP_LED	O	Control for external LED connection on J55
GP62	UART1_SHUTDOWN	O	Used in conjunction with J57 to control the Serial 1 transceiver
GP63	UART3_SHUTDOWN	O	Used in conjunction with J57 to control the Serial 3 transceiver
GP66	Reserved		

Table 10. System I/O Control

System Monitoring

Both the Catalyst LP and devices on the carrier board perform system monitoring of temperature, voltage, and power. This section describes how the development kit uses each of these capabilities.

Temperature Monitoring

On the Catalyst LP, the embedded controller performs temperature monitoring by measuring the temperatures on the Intel Atom processor die and near the memory chips. The carrier board includes three temperature sensors that are accessible using the Super I/O Controller hardware monitoring registers. The following table identifies these sensors and their location on the carrier board.

Sensor	Location
Internal	Internal to the Super I/O Controller
Remote 1 (Q61)	Component side near Super I/O Controller
Remote 2 (Q62)	Component side near Super I/O Controller

Table 11. Temperature Sensors

For external cooling applications or motor control, the Super I/O Controller includes two tachometer inputs and two pulse width modulation (PWM) outputs. These signals are available on header J35, page 40 and header J36, page 41.

In addition to the Super I/O Controller, the carrier board includes a National Semiconductor LM75. The LM75 is a temperature sensor, Delta-Sigma analog-to-digital converter, and digital over-temperature detector. This device is access-able using the carrier I^2C bus and drives the thermal monitor LED D29. For the I^2C bus address of the LM75, see Carrier I^2C Bus, page 18.

Voltage Monitoring

In addition to temperature monitoring, the embedded controller performs voltage monitoring of the input power and on-module voltage regulators. On the carrier board, the Super I/O Controller also provides the capability to monitor voltages generated on the carrier board. Four analog inputs to the Super I/O Controller monitor the on-board voltages, as described in the following table.

Super I/O Controller Input	On-board Voltage
VCCP_IN	V1.8S
+2.5V_IN	V3.3S
+12V_IN	V12S
+5V_IN	V5S

Table 12. Voltage Monitors

Power Monitoring

Power consumption varies based on the actual application. Several factors including level of processor activity and peripheral connections affect the total power consumption of a system. The Catalyst LP Development Kit includes power monitoring circuitry that allows the actual current draw of the system to be measured in real-time. Five Texas Instruments INA209 power monitor devices connect to the embedded controller I^2C bus. Each device monitors one of the five voltages supplied to the module on docking connector J2, page 32. For details about addressing these devices, see Carrier I^2C Bus, page 18.

Audio Interface

The Catalyst LP Development Kit offers a variety of audio inputs and outputs supporting a wide range of applications. On the Catalyst LP, the Intel ICH8M provides an Intel High Definition Audio (Intel HD Audio) interface that implements high quality audio in an embedded environment. The Intel HD Audio specification defines a uniform interface between a host computer and audio codec, specifying register control, physical connectivity, programming model, and codec architectural components. This Intel HD Audio interface connects to an IDT 92HD71B8 4-channel audio codec located on the carrier board and is available to a secondary codec on header J18, page 36. The Catalyst LP supports 3.3 V signalling levels.

The development kit provides the following audio inputs and outputs:

- SPDIF on RCA jack J19, page 36 (optional)
- Stereo Line Inputs and Headphones on stereo jack J20, page 37
- Digital Microphone on socket J22, page 37
- Stereo Line Out 1 on stereo phone jack J23, page 37
- Stereo Line Out 0 on stereo phone jack J53, page 44
- Microphone stereo phone jack J54, page 44

For electrical specifications, see Audio Codec, page 55.

Power and Power Management

Power and power management are especially critical on the Catalyst LP Development Kit. The Catalyst LP has very specific power and power-on sequence requirements in order to power-up and operate correctly. If the system does not meet the module's requirements, the module will not boot.

The following sections provide an overview of the Catalyst LP power requirements. For a complete description, refer to the *Catalyst LP Design-In Guide (Eurotech document #110125-1000)*. Custom carrier boards must implement the exact power supply sequencing described in the design-in guide.

Power Supply Architecture

The following diagram illustrates the power supply architecture of the Catalyst LP Development Kit. Notice that voltages ending with an "A" indicate "always" power (power states S0, S3, S4, and S5), voltages with no suffix indicate primary power (power states S0 and S3), and voltages ending with an "S" indicate normal operating power (power state S0).

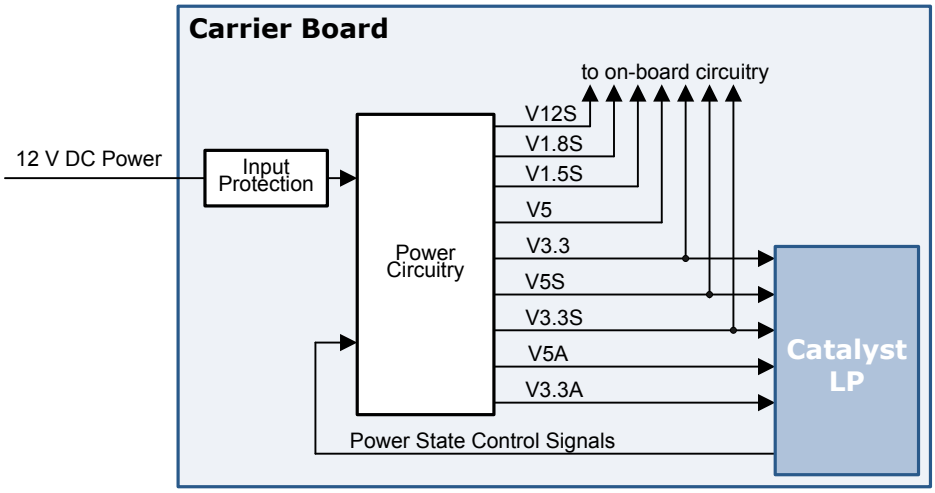


Figure 5. Power Supply Architecture

The architecture of the power supply partitions power distribution across the Catalyst LP and the carrier board. Power jack J29, page 39 accepts +12 VDC input power from an external supply such as the AC power adapter included with the Catalyst LP Development Kit. The maximum main input voltage is limited by input protection.

The development kit includes the capability to selectively turn off power to the display subsystem including LVDS Display, Touch Panel, and Backlight. For details, see Display and User Interface, page 20. This load-shedding feature can significantly reduce power consumption. Applications and the operating system determine how selective power management is utilized.

ACPI Power Management States

The Catalyst LP supports the Advanced Configuration and Power Interface (ACPI), version 2.0 which defines the low power states for ACPI-compliant systems. This capability allows the Catalyst LP to cycle into power saving states. Wake events transition the Catalyst LP from a low-power state back to full operation. For specific information about power management on the Catalyst LP, refer to the *Catalyst LP Design-In Guide (Eurotech document #110125-1000)*.

Mechanical

Mechanical Drawing

The following mechanical drawing specifies the dimensions of the carrier board, as well as locations of key components on the board. All dimensions are in inches.

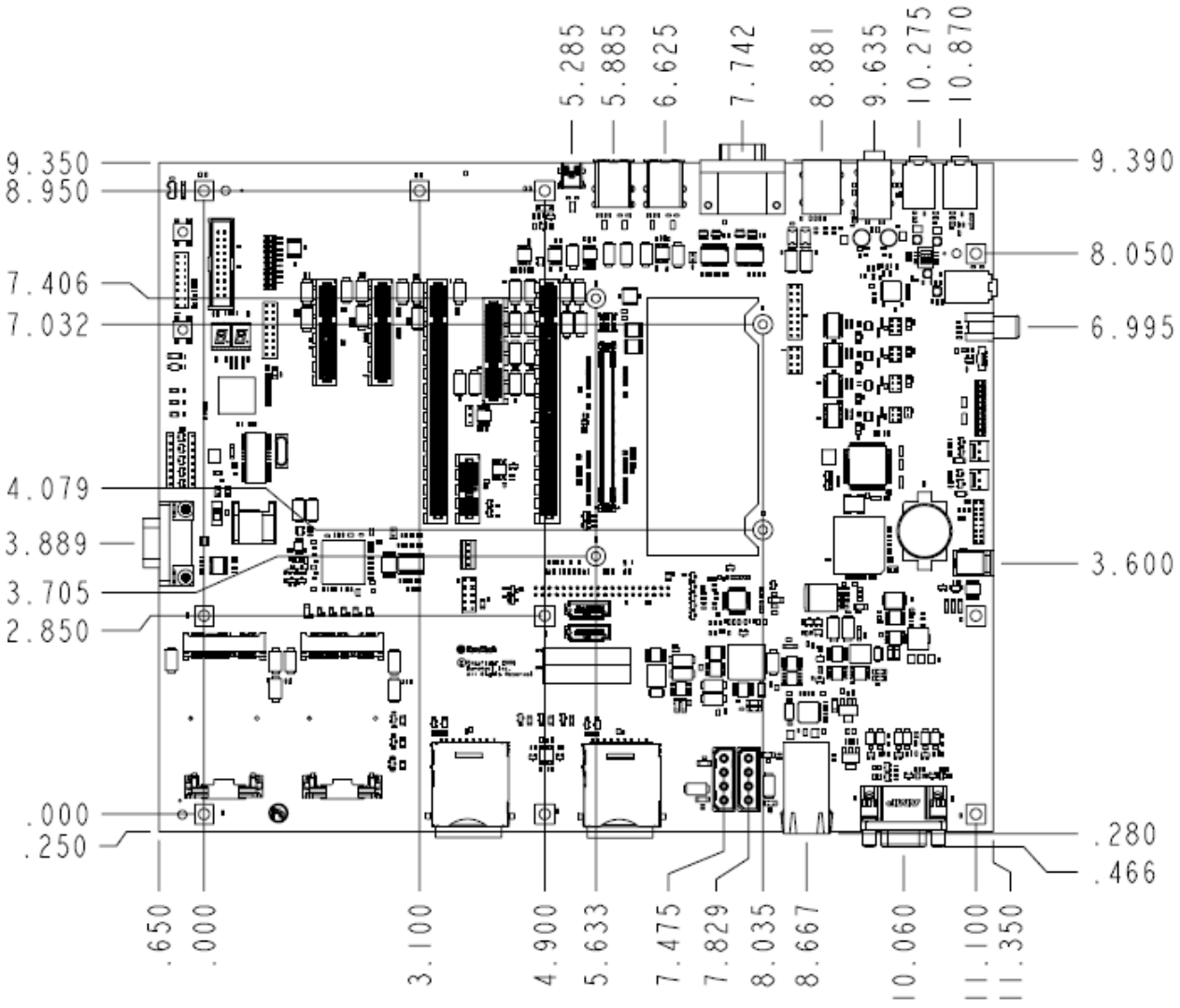


Figure 6. Catalyst LP Development Kit Carrier Board, Top View

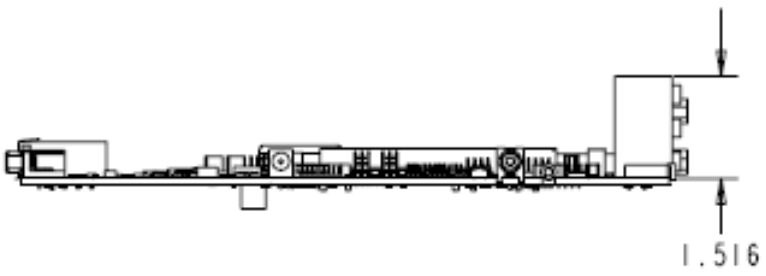


Figure 7. Catalyst LP Development Kit Carrier Board, Side View

Mounting Holes

The carrier board includes three sets of mounting holes that enable the following mountings:

- Catalyst LP to carrier board (MH11 - MH14)
- Carrier board to enclosure (MH5 – MH10)
- Carrier board to enclosure along I/O panel (MH1 – MH4)

The mounting holes for the Catalyst LP and carrier board connect electrically to the ground plane, while the mounting holes along the I/O panel connect electrically to chassis ground. The ground plane and chassis ground are electrically connected. All connections are made using 600 Ω inductors.

Per IPC-A-610D section 4.2.3, secure the board to standoffs using a flat washer against the board with a split washer on top between the flat washer and the screw head or nut. Do not use toothed star washers, as they cut into the plating and laminations of the board over time and will not produce an attachment that will withstand vibration and thermal cycling.

Installing and Removing the Catalyst LP

The Catalyst LP connects to the carrier board through two connectors that are in line with each other. A high-density, stacking board-to-board connector carries the data signals, while a smaller 2x7-pin 1 mm-pitch connector carries power. When fully connected, these fine pitch connectors provide reliable and durable connection. However, care is required when removing or installing the module onto the carrier board. If correct procedures for installation and removal are not followed, damage to the connectors and/or the connector pins can result.

For detailed procedures to install a module onto or remove a module from a carrier board, refer to the *Catalyst Module Installation and Removal (Eurotech document #110122-2014)*. Download this document from the Eurotech support site (http://support.eurotech-inc.com/, topic 2778).

Warning:
Observe industry-standard electronic handling procedures when handling the module. Eurotech recommends using a grounded wrist strap and heel strap. The connectors expose signals on the system bus that do not have ESD protection.

Connectors, Switches, Jumpers, and Indicators

Identifying Connectors

The following diagrams illustrate the location and numbering of the connectors on the carrier board. The Catalyst LP mates to two docking connectors, J1 and J2, which lie under the module when installed. Header J8 and socket J71 are located on the bottom side of the carrier board and are shown by dashed lines. Unlabeled connectors are not used on the standard Catalyst LP Development Kit.

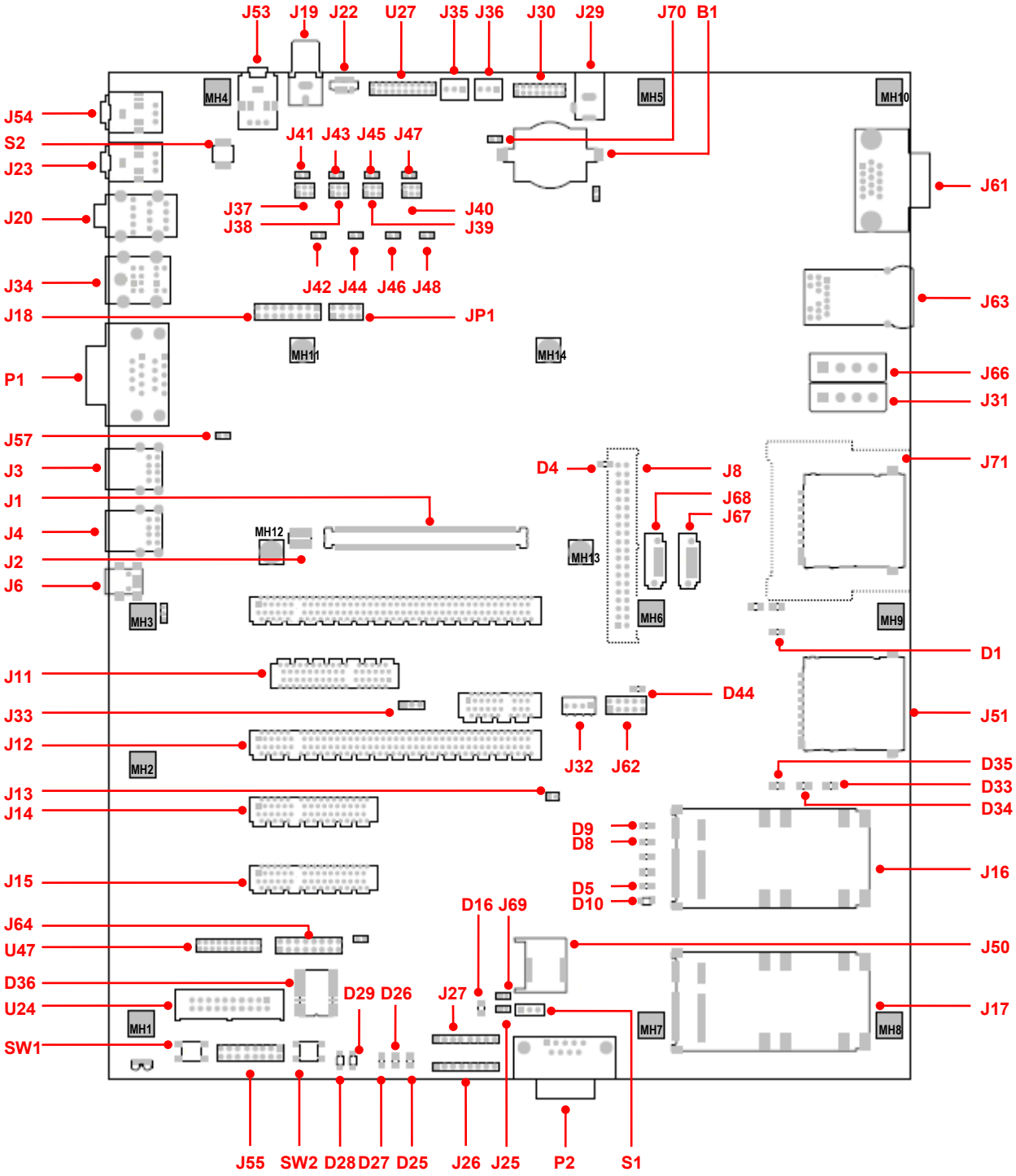
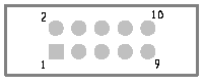


Figure 8. Connector Location

Determining Pin Numbers

Most double-row headers place even pins on one side and odd pins on the other. The diagram at right indicates how pins are numbered, as seen from the component side of the board.



To locate pin 1 of a connector or jumper, try the following:

1. Look for a visible number or marking on the board that indicates connector pin numbering. A notch or dot usually indicates pin 1.
2. Look at the underside of the board. The square pad is pin 1.

Switches, Jumpers, and Indicators

This section describes various switches, jumpers, and indicators on the carrier board.

SW1: Reset

SW1 is the reset button for the Catalyst LP Development Kit. Pressing SW1 initiates a hardware reset of module circuitry including the processor. Press this button to restart the system without cycling power. In addition, this switch connects to the front panel reset signal, SWX_RESET# (J55 pin 7) allowing connection of an external reset switch.

SW2: Power

SW2 is the power button for the Catalyst LP Development Kit. SW2 turns power used for normal operation on and off or indicates a power state change. The following table defines the functionality of the power button.

Power Button	Operation
Momentary press (less than 4 sec.)	From shutdown, initiates a power-up sequence to full operation. From full operation, initiates an orderly shutdown sequence and turns off power.
Press and hold (greater than 4 sec.)	Initiates a “4 second over-ride” and turns off power without notification to the operating system.

Table 13. Power Button

Switch SW2 also connects to the front panel power signal, SWX_ONOFF# (J55 pin 6) allowing connection of an external on/off switch.

S1: Radio Disable

S1 is a one-position slide switch that controls the radio operation of a wireless communications add-in card connected to J16, page 35.

Switch Setting	Configuration
On (toward pin 3)	Radio disabled
Off (toward pin 1)	Radio enabled (default)

S2: Audio Sense

S2 is a four-position dip switch that controls the audio sense input on J20, page 37.

Switch Setting	Configuration
All open	(default)
Position 1	Indicates jack inserted into Headphone port (J20 middle, green)
Position 2	Indicates jack inserted into Microphone port (J20 bottom, pink)
Position 3	Indicates jack inserted into Line In port (J20 top, blue)

J13: PCIe Switch EEPROM (option)

Type: 2-post header, 2 mm

Jumper J13 enables configuration of the carrier board PCIe switch using a serial EEPROM.

Jumper Setting	Configuration
1-2	Serial EEPROM output connects to the PCIe switch data out
NC	10kΩ pull-up resistor on PCIe switch data out (default)

J70: RTC Battery

Type: 2-post header, 2 mm

Jumper J70 completes the connection of the RTC battery to the Catalyst LP.

Jumper Setting	Configuration
1-2	RTC battery is connected. (default)
NC	RTC battery is disconnected.

Carrier Board LED Indicators

The carrier board has seventeen green light-emitting diodes (LEDs) and three red LEDs to indicate system operation. The following tables describe the LED functionalities.

D1: SD/MMC LEDs

LED	Type	Description
D1	Green	On indicates activity on the SD/MMC socket J51

D4: IDE/PATA LED

LED	Type	Description
D4	Green	Blinking indicates activity on the IDE/PATA interface

D5-D10: PCIe Switch LEDs

LED	Type	Description
D5	Green	On indicates PCIe connection between module and PCIe switch
D6	Green	Not used
D7	Green	Not used
D8	Green	On indicates a connection on the Mini PCIe 0 slot J16
D9	Green	On indicates a connection on the Mini PCIe 1 slot J17
D10	Red	On indicates a fatal error

D16: Touch Panel LED

LED	Type	Description
D16	Green	Blinking indicates activity on the touch panel

D25-D27: Power LEDs

LED	Type	Description
D25	Green	On indicates normal operating power (V3.3S)
D26	Green	On indicates primary supply voltage (V3.3)
D27	Green	On indicates power is connected (V3.3A)

D28-D29: Thermal Monitoring LEDs

LED	Type	Description
D28	Red	On indicates a SIO thermal alert
D29	Red	On indicates a carrier thermal alert

D33-D35: Mini PCIe 0 Status LEDs

LED	Type	Description
D33	Green	Indicates Wireless Personal Area Network (WPAN)
D34	Green	Indicates Wireless Local Area Network (WLAN)
D35	Green	Indicates Wireless Wide Area Network (WWAN)

D36: Port 80 Status Display

D36 displays the Port 80 POST codes from the Catalyst LP.

D44: USB Host 8 LED

LED	Type	Description
D44	Green	Dependent on the device connected to J62

Ethernet LEDs

Ethernet socket J63, page 46 includes two LEDs. The LED on the left side indicates speed as follows.

Color	Speed (Mbps)
Green	1000
Yellow	100
Off	10

The green LED on the right side indicates connection and activity as follows.

Operation	Link/Activity
On	Valid connection
Blinking	Ethernet activity
Off	No connection

Display Adapter LED Indicators

The display adapter, installed in J11, has two green light-emitting diodes (LEDs) to indicate system operation. The tables provided in this section describe the LED functionalities.

D1: Backlight On LED

This LED indicates the status of the backlight power on the display adapter.

LED	Type	Description
D1	Green	On indicates backlight power on

D2: Power On LED

This LED indicates when power is applied to the display adapter.

LED	Type	Description
D2	Green	On indicates 3.3 V power on

Signal Headers

The following tables describe the electrical signals available on the connectors of the carrier board. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions, and references to related sections.

For the location of the connectors, see Identifying Connectors, page 28.

J1: Docking Connector: Data

The Catalyst LP connector J1 mates to the carrier board connector J1. Most data signals are provided on this docking connector.

J2: Docking Connector: Power

The Catalyst LP receives the power input and controls for interfacing with an external power supply on this docking connector.

J3: USB Host 0 and USB Host 1

Board connector: USB Type A dual receptacle, Molex 67298-3091
Mating connector: USB Type A plug

The dual USB socket J3 provides USB Host 0 and USB Host 1. These ports support USB 2.0 high, full, and low speed devices. The connector shield is tied to chassis ground. For further details, see USB, page 17.

Socket	Pin	Name	Type	Description
A	1	5V_USB_PORT0	PO	5 V DC power output
	2	USB_PORT0_N	IO	USB Host 0
	3	USB_PORT0_P		
	4	GND	P	Ground
B	1	5V_USB_PORT1	PO	5 V DC power output
	2	USB_PORT1_N	IO	USB Host 1
	3	USB_PORT1_P		
	4	GND	P	Ground

J4: USB Host 6 and USB Host 7

Board connector: USB Type A dual receptacle, Molex 67298-3091
Mating connector: USB Type A plug

The dual USB socket J4 provides USB Host 6 and USB Host 7. These ports support USB 2.0 high, full, and low speed devices. The connector shield is tied to chassis ground. For further details, see USB, page 17.

Socket	Pin	Name	Type	Description
A	1	5V_USB_PORT6	PO	5 V DC power output
	2	USB_PORT6_N	IO	USB Host 6
	3	USB_PORT6_P		
	4	GND	P	Ground
B	1	5V_USB_PORT7	PO	5 V DC power output
	2	USB_PORT7_N	IO	USB Host 7
	3	USB_PORT7_P		
	4	GND	P	Ground

J6: USB Host 2

Board connector: Mini USB Type B receptacle, FCI 10033526-N3215LF
Mating connector: Mini USB Type B plug

The USB signals located on mini socket J6 support a USB 2.0 host operating at high, full, and low speeds. The connector shield is tied to chassis ground. Jumper J5 is included on the carrier board for backward compatibility with the Catalyst XL. This jumper must be installed on pin 2 and pin 3 for correct operation of the USB host port on J6. For further details, see USB, page 17.

Pin	Name	Type	Description USB Host (default)
1	USBPWR_CLIENT	PO	5 V DC output (Set by jumper J5)
2	USB_PORT2_N	IO	USB Host 2
3	USB_PORT2_P		
4	NC		
5	GND	P	Ground

Warning:
Socket J6 pin 1 is a power input or power output based on jumper J5. Check the jumper setting before connecting a USB device to this port.

J8: IDE/PATA Disk Drive (optional)

Board connector: 2x20 shrouded header, 0.1-inch, Neltron 2316S-40G-F1
Mating connector: 40-pin IDE socket

Header J8 conforms to the PATA Standard supporting an optional 2.5-inch PATA magnetic or solid-state disk drive. For a description of the external memory interfaces available on the Catalyst LP Development Kit, see External Memory Interfaces, page 15.

Notes:
The CF card socket J71 and the IDE/PATA header J8 are mutually exclusive. Install a CF card in socket J71 or connect an IDE/PATA disk drive to header J8.

For development kits using the Catalyst LP revision A module, SATA 2 on header J68 is mutually exclusive with the CF card slot J71 and the IDE/PATA header J8. If your application uses a CF card or IDE/PATA disk drive, SATA 2 is not supported.

J11: LVDS Display & Backlight

Board connector: PCIe x4 socket, Molex 87715-9106
Mating connector: Custom display adapter card

Socket J11 is a Eurotech-specific socket that includes the LVDS display and backlight control signals. The display adapter included with the Catalyst LP Development Kit mates to socket J11 and provides an interface between the carrier board and display subsystem. For further details, see Display and User Interface, page 20.

Warning:
Socket J11 is a Eurotech-specific socket. Install the Catalyst Module Display Adapter card in this socket only.

Pin	Name	Type	Description
A1	GND	P	Ground
A2	V12S	PO	12 V power
A3	V12S	PO	12 V power
A4	GND	P	Ground
A5	NC		
A6	NC		
A7	NC		
A8	NC		
A9	V3.3S	PO	Normal operating 3.3 V
A10	V3.3S	PO	Normal operating 3.3 V
A11	BUF_RST#	O-3.3	Buffered reset
A12	GND	P	Ground
A13	LA_CLKP	O-LVDS	LVDS clock
A14	LA_CLKN		
A15	GND	P	Ground
A16	L_DDC_CLK	O-OD	LCD DDC I^2C clock
A17	L_DDC_DATA	IO-OD	LCD DDC I^2C data
A18	GND	P	Ground
A19	NC		
A20	GND	P	Ground
A21	L_CTLA_CLK	O-OD	Backlight I^2C clock
A22	L_CTLB_DATA	IO-OD	Backlight I^2C data
A23	GND	P	Ground
A24	GND	P	Ground
A25	L_BKLTSEL0_GPIO#	O-3.3	Selects backlight control (PWM vs. I^2C)
A26	L_BKLTCTL	O-CMOS	Controls intensity of the backlight
A27	GND	P	Ground
A28	GND	P	Ground
A29	L_BKLTEN	O-CMOS	Turns power to the backlight on or off
A30	L_VDDEN	O-CMOS	LCD power enable
A31	GND	P	Ground
A32	NC		
B1	V12S	PO	12 V power
B2	V12S	PO	12 V power
B3	V12S	PO	12 V power
B4	GND	P	Ground
B5	SMB_CLK	O-LVTTL	SMBus clock
B6	SMB_DATA	IO-LVTTL	SMBus data
B7	GND	P	Ground
B8	V3.3S	PO	Normal operating 3.3 V
B9	NC		
B10	NC		
B11	LVDS_PRESENT	I-3.3	Display adapter detect (Super I/O Controller GP30)
B12	V5S	PO	Normal operating 5 V
B13	GND	P	Ground
B14	LA_DATAP0	O-LVDS	LVDS data 0
B15	LA_DATAN0		
B16	GND	P	Ground
B17	SLOT_PRESENCE	I-3.3	Card present
B18	GND	P	Ground
B19	LA_DATAP1	O-LVDS	LVDS data 1
B20	LA_DATAN1		
B21	GND	P	Ground
B22	GND	P	Ground
B23	LA_DATAP2	O-LVDS	LVDS data 2
B24	LA_DATAN2		
B25	GND	P	Ground
B26	GND	P	Ground
B27	Reserved		
B28	Reserved		
B29	GND	P	Ground
B30	NC		
B31	SLOT_PRESENCE	I-3.3	Card present
B32	GND	P	Ground

J12: PCIe 0 (x1 or x4)

Board connector: PCIe x16 socket, Molex 87715-9306
Mating connector: PCIe card

Socket J12 provides a direct PCIe x1 connection to the Catalyst LP. The socket accepts x1, x4, x8, and x16 cards. However, it automatically negotiates down to an x1 lane. PCIe 0 does not support the optional JTAG signals. For further details, see PCI Express Bus, page 17.

As a custom configuration, the four PCIe slots provided by the Catalyst LP connect directly to socket J12 supporting a PCIe x4 lane.

J14: PCIe 1 (x1)

Board connector: PCIe x4 socket, Molex 87715-9106
Mating connector: PCIe card

Socket J14 provides a direct PCIe x1 connection to the Catalyst LP. This socket accepts x1 and x4 cards. However, it automatically negotiates down to an x1 lane. PCIe 1 does not support the optional JTAG signals. For further details, see PCI Express Bus, page 17.

As a custom configuration, socket J14 connects to the 5-lane, 5-port PCIe switch instead of directly to the Catalyst LP.

J15: PCIe 2 (x1)

Board connector: PCIe x4 socket, Molex 87715-9106
Mating connector: PCIe card

Socket J15 provides a direct PCIe x1 connection to the Catalyst LP. This socket accepts x1 and x4 cards. However, it automatically negotiates down to an x1 lane. PCIe 2 does not support the optional JTAG signals. For further details, see PCI Express Bus, page 17.

As a custom configuration, socket J15 connects to the 5-lane, 5-port PCIe switch instead of directly to the Catalyst LP.

J16: Mini PCIe 0 with UIM

Board connector: 52-pin MiniCard, Molex 67910-0001
Mating connector: Mini PCIe card

The carrier board includes a 5-lane, 5-port PCIe switch for expanded PCIe capability. Socket J16 connects to this switch providing Mini PCIe 0. For further details, see PCI Express, page 17. Socket J16 supports an UIM interface which also connects to socket J50, radio operation of a wireless communications add-in card, and status indicators. For details about control of the radio operation, see S1, page 29. For details about the status indicators, see Carrier Board LED Indicators, page 30.

J17: Mini PCIe 1

Board connector: 52-pin MiniCard, Molex 67910-0001
Mating connector: Mini PCIe card

The carrier board includes a 5-lane, 5-port PCIe switch for expanded PCIe capability. Socket J17 connects to this switch providing Mini PCIe 1. For further details, see PCI Express, page 17. Unlike socket J16, socket J17 does not support a UIM interface, radio operation of a wireless communication add-in card, and status indicators.

J18: Secondary Audio Codec

Board connector: 2x8 header, 0.1-inch, Samtec HMTSW-108-07-LD-200
Mating connector: Samtec HCSD series socket

The Intel HD Audio interface provided on the Catalyst LP supports up to two audio codecs. The primary codec is populated on the carrier board, while header J18 provides a connection to an external secondary codec. For further details, see Audio Interface, page 24.

Pin	Name	Type	Termination	Description
1	GND	P		Ground
2	NC			
3	V3.3	PO		3.3 V primary supply voltage
4	NC			
5	NC			
6	HDA_SDATAIN1	I-HDA		Serial data in 1
7	V12S	PO		12 V power
8	Reserved			
9	V3.3	P		3.3 V primary supply voltage
10	HDA_SDATAOUT	O-HDA	R 33Ω	Serial data out
11	GND	P		Ground
12	HDA_SYNC	O-HDA	R 33Ω	Frame sync
13	DVDD_IO	PO		Reference voltage
14	HDA_RST#	O-HDA	R 33Ω	Audio reset
15	GND	P		Ground
16	HDA_BITCLK	O-HDA	R 33Ω	Bit clock

JP1: Secondary Audio Codec Jumper

Type: 2x4 header, 0.1-inch

Jumper JP1 provides additional signals for the secondary codec.

Pin	Name	Type	Termination	Description
1	HDA_PWRDN_NET	O	PD 10kΩ	Audio power down
2	SPKR	O-LVTTL		PC beep audio
3	GND	P		Ground
4	V5	PO		5 V primary supply
5	V3.3S	PO		Normal operating 3.3 V
6	NC			
7	HDA_DOCK_RST#	O-HDA		Docking function reset
8	HDA_DOCK_EN#	O-LVTTL		Docking function enable

J19: S/PDIF (optional)

Board connector: RCA jack, right angle, CUI Inc RCJ-041
Mating connector: RCA plug

Socket J19 provides an optional Sony/Philips Digital Interconnect Format (S/PDIF) output for connectivity to consumer electronic equipment. For further details, see Audio Interface, page 24.

Pin	Name	Type	Description
1	GND	P	Ground
2	SPDIF	O	S/PDIF

J20: Stereo Line Input, Microphone Input, and Headphone Output

Board connector: 3.5 mm stereo jack, stacked, Kycon STX-4335-5BGP-S1
Mating connector: 3.5 mm stereo plug

Socket J20 provides direct connections to two stereo line inputs and one headphone output. The shell of the socket is connected to chassis ground. For further details, see Audio Interface, page 24.

Socket	Pin	Name	Type	Description
Top, Blue	32	PORT_C_R_L	AI	Line In 1
	35	PORT_C_L_L		
Center, Green	22	PORT_A_R_L	AO	Headphone
	25	PORT_A_L_L		
Bottom, Pink	2	PORT_B_R_L	AI	Line In 0 (Microphone)
	5	PORT_B_L_L		
	1	GND_HDA	P	Audio ground

J22: Digital Microphone

Board connector: 6-pin FFC/FPC connector, 0.5 mm, Molex 52559-0672

In addition to the analog microphone input, the codec included on the carrier board supports a digital microphone input on socket J22. For further details, see Audio Interface, page 24.

Pin	Name	Type	Description
1	DMIC_CLK_OUT	O	Digital microphone clock
2	GND	P	Ground
3	V_DMIC_L	PO	Digital microphone power (default 3.3 V)
4	DMIC0	I	Digital microphone channel 0
5	GND	P	Ground
6	DMIC1	I	Digital microphone channel 1

J23: Stereo Line Out 1

Board connector: 3.5 mm stereo phone jack, Kobiconn 161-3503-EX
Mating connector: 3.5 mm stereo phone plug

Socket J23 provides the connection to one stereo line output capable of driving powered speakers. For further details, see Audio Interface, page 24.

Pin	Name	Type	Description
1	GND_HDA	P	Audio ground
2	PORT_D_L_L	AO	Line out 1, left channel
3	NC		
4	NC		
5	PORT_D_R_L	AO	Line out 1, right channel
6	NC		
7	GND_HDA	P	Audio ground
8	SENSE_A_PD	AI	Detects a connection on Port D

J26: Touch Panel (4- or 5-wire)

Board connector: 8-pin header, 0.1-inch, Samtec HMTSW-108-07-L-S-200
Mating connector: Samtec HCSS series socket

Header J26 supplies the signals for a 4- or 5-wire touch panel. Standard Catalyst LP Development Kits include a 4-wire touch panel. For further details, see Touch Panel Controller, page 21.

Pin	Name	Type	4-Wire	4-Wire (Alt)	5-Wire	5-Wire (Alt)	Description
1	TC0	AIO		Left	UR		Touch panel
2	TC1	AIO		Right	UL		
3	TC2	AIO		Top	Wiper		
4	TC4	AIO	Bottom	Bottom	LL	LL	
5	TC3	AIO	Right		LR	UL	
6	TC2	AIO	Top			Wiper	
7	TC1	AIO	Left			LR	
8	TC0	AIO				UR	

J27: Touch Panel (8-wire)

Board connector: 8-pin header, 0.1-inch, Samtec HMTSW-108-07-L-S-200
Mating connector: Samtec HCSS series socket

Header J27 supports an 8-wire touch panel by adding sense lines to the excite lines. Standard Catalyst LP Development Kits include a 4-wire touch panel. For further details, see Touch Panel Controller, page 21.

Pin	Name	Type	8-Wire	Description
1	TC2	AIO	Bottom	Touch panel
2	SY+	AIO	Bottom sense	
3	SX+	AIO	Right sense	
4	TC0	AIO	Right	
5	TC4	AIO	Top	
6	SY-	AIO	Top sense	
7	SX-	AIO	Left sense	
8	TC1	AIO	Left	

J25: Touch Panel Configuration Jumper

Type: 2-post header, 2 mm

Jumper J25 configures the development kit for support of 4-, 5- and 8-wire touch panels.

Jumper Setting	Configuration
1-2	4-, 5-, and 8-wire support (default)
NC	8-wire only support

J69: Touch Panel Enable Jumper

Type: 2-post header, 2 mm

Jumper J69 enables or disables the touch panel controller on the carrier board.

Jumper Setting	Configuration
1-2	Disables touch panel controller
NC	Enables touch panel controller (default)

J29: DC Power Input

Board connector: power jack, 2.1 mm x 5.5 mm, CUI Inc PJ-202AH
Mating connector: 2.1 mm power supply plug

Power jack J29 accepts +12 VDC input power from an external supply such as the AC power adapter included with the Catalyst LP Development Kit. The power input is on the center pin. For details about the power supply architecture, see Power Supply Architecture, page 25.

Warning:
Disconnect the power input before removing the module. Removing the module from a powered carrier board may result in damage to both the carrier board and to the module. For detailed instructions for removing the module, refer to the *Catalyst Module Installation and Removal (Eurotech document #110122-2014)*.

J30: JTAG

Board connector: 2x8 socket, 2 mm, Samtec SQT-108-01-L-D
Mating connector: Samtec TCMD series IDC assembly

The Catalyst LP Development Kit provides a full IEEE1149.1 JTAG port for factory test and for board-level software debugging; otherwise, the JTAG port is not supported for application use.

Pin	Name	Type	Description
1	JTAG_TRST#	I	JTAG interface
2	JTAG_TMS	I	
3	GND	P	
4	JTAG_TDI	I	
5	JTAG_TCK	I	
6	V3.3S	PO	
7	GND	P	
8	JTAG_TDO	O	
9	NC		
10	NC		
11	NC		
12	V5S	PO	
13	NC		
14	NC		
15	NC		
16	GND	P	

J31: Disk Drive Power Out 0

Board connector: 4-pin header, 0.2-inch, Molex 15-24-4449
Mating connector: Molex 15-24-4048 crimp housing

Header J31 supplies power to an optional external disk drive used for mass storage in the Catalyst LP Development Kit.

Warning:
J31 provides output power only. Do not connect to an input power source.

Pin	Name	Type	Description
1	V12S	PO	12 V power
2	GND	P	Ground
3	GND	P	Ground
4	V5S	PO	5 V normal operating power

J32: SMBus

Board connector: 4-pin shrouded header, 0.1-inch, FCI 69167-104HLF
Mating connector: PV CTW housings and contacts

The SMBus provides I/O expansion capabilities on header J32. Use this interface to communicate with external devices. For further details, see System Management Bus, page 19.

Pin	Name	Type	Description
1	SMB_DATA	IO-LVTTL	SMBus data
2	SMB_CLK	O-LVTTL	SMBus clock
3	SMB_ALERT#	IO-LVTTL	SMBus interrupt
4	GND	P	Ground

Notes:
The SMBus is not compatible with all I^2C devices. Review the device data sheet carefully before connecting an I^2C device to the SMBus.

J33: Carrier I^2C Bus

Board connector: 3-pin header, 0.1-inch, Samtec HMTSW-103-07-L-S-200-LL
Mating connector: Samtec HCSS series socket

Header J33 provides an external connection to the I^2C bus of the Catalyst LP embedded controller. For further details, see Carrier I^2C Bus, page 18.

Pin	Name	Type	Description
1	CARRIER_I2C_SDA	IO	I^2C bus data
2	CARRIER_I2C_SCL	O	I^2C bus clock
3	GND	P	Ground

J34: PS/2 Keyboard & Mouse

Board connector: double-stacked Mini-DIN socket, Kycon KMDGX-6SG/P-S4N
Mating connector: Mini-DIN plug

The Catalyst LP Development Kit supports a PS/2 keyboard and PS/2 mouse on socket J34. The connector shield is tied to chassis ground. For further details, see Carrier Board PS/2 Support, page 21.

Socket	Description
Top	PS/2 Mouse
Bottom	PS/2 Keyboard

J35: Tachometer 1

Board connector: 3-pin header, 0.1-inch, Molex 22-23-2031
Mating connector: Molex 22-01-2031 crimp terminal housing

Two tachometer outputs are available on header J35 and header J36 for motor control or external cooling applications. For further details, see Temperature Monitoring, page 23.

Pin	Name	Type	Description
1	TACH1	O	Tachometer 1
2	V12S	PO	12 V power
3	TACH1_PWR	AO	Switched adjustable control 1

J36: Tachometer 2

Board connector: 3-pin header, 0.1-inch, Molex 22-23-2031
Mating connector: Molex 22-01-2031 crimp terminal housing

Two tachometer outputs are available on header J35 and header J36 for motor control or external cooling applications. For further details, see Temperature Monitoring, page 23.

Pin	Name	Type	Description
1	TACH2	O	Tachometer 2
2	V12S	PO	12 V power
3	TACH2_PWR	AO	Switched adjustable control 2

J37: Serial 6

Board connector: 2x3 header, 2 mm, Samtec TMM-103-03-T-D
Mating connector: Samtec TCSD series socket

Header J37 supports an EIA-485 serial port. For further details, see Serial Ports, page 20.

Pin	Name	Type	Description
1	RX6_485+	I	Non-inverting Receive Data 6
2	RX6_485-	I	Inverting Receive Data 6
3	485_6_GND	P	Ground (through ferrite bead)
4	TX6_485+	O	Non-inverting Transmit Data 6
5	TX6_485-	O	Inverting Transmit Data 6
6	GND	P	Ground

J41: Serial 6 Receive Termination Jumper

Type: 2-post header, 2 mm

Jumper J41 provides termination across the inverting and non-inverting receive lines.

Jumper Setting	Configuration
1-2	121Ω termination resistor
NC	No termination (default)

J42: Serial 6 Transmit Termination Jumper

Type: 2-post header, 2 mm

Jumper J42 provides termination across the inverting and non-inverting transmit lines.

Jumper Setting	Configuration
1-2	121Ω termination resistor
NC	No termination (default)

J38: Serial 4

Board connector: 2x3 header, 2 mm, Samtec TMM-103-03-T-D
Mating connector: Samtec TCSD series socket

Header J38 supports an EIA-485 serial port. For further details, see Serial Ports, page 20.

Pin	Name	Type	Description
1	RX4_485+	I	Non-inverting Receive Data 4
2	RX4_485-	I	Inverting Receive Data 4
3	485_4_GND	P	Ground (through ferrite bead)
4	TX4_485+	O	Non-inverting Transmit Data 4
5	TX4_485-	O	Inverting Transmit Data 4
6	GND	P	Ground

J43: Serial 4 Receive Termination Jumper

Type: 2-post header, 2 mm

Jumper J43 provides termination across the inverting and non-inverting receive lines.

Jumper Setting	Configuration
1-2	121Ω termination resistor
NC	No termination (default)

J44: Serial 4 Transmit Termination Jumper

Type: 2-post header, 2 mm

Jumper J44 provides termination across the inverting and non-inverting transmit lines.

Jumper Setting	Configuration
1-2	121Ω termination resistor
NC	No termination (default)

J39: Serial 5

Board connector: 2x3 header, 2 mm, Samtec TMM-103-03-T-D
Mating connector: Samtec TCSD series socket

Header J39 supports an EIA-422 serial port. For further details, see Serial Ports, page 20.

Pin	Name	Type	Description
1	RX5_422+	I	Non-inverting Receive Data 5
2	RX5_422-	I	Inverting Receive Data 5
3	422_5_GND	P	Ground (through ferrite bead)
4	TX5_422+	O	Non-inverting Transmit Data 5
5	TX5_422-	O	Inverting Transmit Data 5
6	GND	P	Ground

J45: Serial 5 Receive Termination Jumper

Type: 2-post header, 2 mm

Jumper J45 provides termination across the inverting and non-inverting receive lines.

Jumper Setting	Configuration
1-2	121Ω termination resistor
NC	No termination (default)

J46: Serial 5 Transmit Termination Jumper

Type: 2-post header, 2 mm

Jumper J46 provides termination across the inverting and non-inverting transmit lines.

Jumper Setting	Configuration
1-2	121Ω termination resistor
NC	No termination (default)

J40: Serial 2

Board connector: 2x3 header, 2 mm, Samtec TMM-103-03-T-D
Mating connector: Samtec TCSD series socket

Header J40 supports an EIA-422 serial port. For further details, see Serial Ports, page 20.

Pin	Name	Type	Description
1	RX2_422+	I	Non-inverting Receive Data 2
2	RX2_422-	I	Inverting Receive Data 2
3	422_2_GND	P	Ground (through ferrite bead)
4	TX2_422+	O	Non-inverting Transmit Data 2
5	TX2_422-	O	Inverting Transmit Data 2
6	GND	P	Ground

J47: Serial 2 Receive Termination Jumper

Type: 2-post header, 2 mm

Jumper J47 provides termination across the inverting and non-inverting receive lines.

Jumper Setting	Configuration
1-2	121Ω termination resistor
NC	No termination (default)

J48: Serial 2 Transmit Termination Jumper

Type: 2-post header, 2 mm

Jumper J46 provides termination across the inverting and non-inverting transmit lines.

Jumper Setting	Configuration
1-2	121Ω termination resistor
NC	No termination (default)

J50: SIM

Board connector: Slide-in SIM card socket, AVX 00-9162-006-206-175
Mating connector: Micro SIM cards

The carrier board includes a standard Subscriber Identity Module (SIM) socket supporting handheld devices requiring secure subscriber identification.

J51: SD/MMC

Board connector: SD/MMC socket, 3M™ SD-RSMT-2-MQ-WF
Mating connector: SD/MMC card

The Catalyst LP Development Kit provides a SD/MMC card slot on socket J51 for memory and I/O expansion. Power to this socket is software-controlled. For further details, see SD Cards, page 16.

J53: Stereo Line Out 0

Board connector: 3.5 mm stereo phone jack, Kobiconn 161-3503-EX
Mating connector: 3.5 mm stereo phone plug

Socket J53 provides the connection to one stereo line output capable of driving powered speakers. For further details, see Audio Interface, page 24.

Pin	Name	Type	Description
1	GND_HDA	P	Audio ground
2	PORT_F_L_L	AO	Line out 0, left channel
3	NC		
4	NC		
5	PORT_F_R_L	AO	Line out 0, right channel
6	NC		
7	GND_HDA	P	Audio ground
8	SENSE_B_PF	AI	Detects a connection on Port F

J54: Microphone

Board connector: 3.5 mm stereo phone jack, Kobiconn 161-3503-EX
Mating connector: 3.5 mm stereo phone plug

Socket J54 provides the connection for a microphone. For further details, see Audio Interface, page 24.

Pin	Name	Type	Description
1	GND_HDA	P	Audio ground
2	PORT_E_L_L	AI	Microphone, left channel
3	NC		
4	NC		
5	PORT_E_R_L	AI	Microphone, right channel
6	NC		
7	GND_HDA	P	Audio ground
8	SENSE_B_PE	AI	Detects a connection on Port E

J55: Front Panel

Board connector: 16-pin header, 0.1-inch, Samtec HTSW-116-07-F-D
Mating connector: Samtec HCSD series socket

Header J55 allows connections of external switches and LEDs to the carrier board.

Pin	Name	Type	Termination	Description
1	FRONT1	O-5	PU 332Ω V5S 470pF to GND	Front 1
2	FRONT2	O-5	PU 332Ω V5A 470pF to GND	Front 2
3	IDE_PDACTIVE#	O	470pF to GND	IDE drive active
4	GND	P		Ground
5	GND	P		Ground
6	SWX_ONOFF#	I-5	PU 10kΩ V5A 470pF to GND	Front panel power button (BTN_ONOFF#)
7	SWX_RESET#	I-3.3	PU 10kΩ V3.3S 470pF to GND	Front panel reset switch (FP_RESET#)
8	GND	P		Ground
9	V5	PO		5 V primary supply voltage
10	NC			
11	NC			
12	GND	P		Ground
13	GND	P		Ground
14	NC			
15	SLP_LED	O-3.3		External LED control (Super I/O Controller GP60)
16	V5	PO		5 V primary supply voltage

J61: VGA Output

Board connector: 15-pin D-sub socket, Tyco Electronics 1734530-3
Mating connector: D-sub plug

Connector J61 provides a direct connection to a standard VGA monitor. This connector includes an analog RGB output and DDC serial bus that identifies the type of monitor connected. The connector shield connects electrically to the ground plane and chassis ground through 0 Ω resistors. For further details, see VGA Display, page 21.

Pin	Name	Type	Description
1	RED_OUT	AO	Red data
2	GREEN_OUT	AO	Green data
3	BLUE_OUT	AO	Blue data
4	NC		
5	GND	P	Ground
6	GND		
7	GND		
8	GND		
9	V5S_VGA	PO	5 V
10	GND	P	Ground
11	NC		
12	DDC_DATA	IO	VGA DDC I^2C data
13	HSYNC_OUT	AO	Horizontal sync
14	VSYNC_OUT	AO	Vertical sync
15	DDC_CLK	O	VGA DDC I^2C clock

J62: USB Host 8

Board connector: 2x5 header, 0.1-inch, Samtec HMTSW-105-07-L-D-200
Mating connector: Samtec HCSD series socket

Header J62 provides the signals for a USB host port. Notice that this port routes directly to the Catalyst LP and does not include additional support circuitry on the carrier board. For further details, see USB, page 17.

Pin	Name	Type	Description
1	V5S	PO	Normal operating 5 V
2	NC		
3	USB_PN8	IO	USB Host 8, negative signal
4	NC		
5	USB_PP8	IO	USB Host 8, positive signal
6	NC		
7	GND	P	
8	NC		
9	NC		(Pin 9 is keyed)
10	USB_HD_LED#	I-5	Control for LED D44, page 31

J63: Gigabit Ethernet

Board connector: RJ-45 socket with LEDs, Pulse Engineering JK0-0036NL
Mating connector: RJ-45 plug

Socket J63 provides a direct connection to a Gigabit Ethernet network. The socket includes two Ethernet LEDs, page 31 and built-in magnetics. The connector shield is tied to chassis ground. For further details, see Gigabit Ethernet, page 18.

J64: CPLD GPIO

Board connector: 16-pin header, 0.1-inch, Samtec HTSW-116-07-F-D
Mating connector: Samtec HCSD series socket

The CPLD on the carrier board provides eight general-purpose inputs and outputs on header J64. For further details, see General-Purpose Inputs and Outputs, page 22.

Pin	Name	Type	Description
1	CPLD_IO_B1_68	IO-CMOS	CPLD IO row B1 pin 68
2	GND	P	Ground
3	CPLD_IO_B1_69	IO-CMOS	CPLD IO row B1 pin 69
4	GND	P	Ground
5	CPLD_IO_B1_70	IO-CMOS	CPLD IO row B1 pin 70
6	GND	P	Ground
7	CPLD_IO_B1_76	IO-CMOS	CPLD IO row B1 pin 76
8	GND	P	Ground
9	CPLD_IO_B1_97	IO-CMOS	CPLD IO row B1 pin 97
10	GND	P	Ground
11	CPLD_IO_B1_98	IO-CMOS	CPLD IO row B1 pin 98
12	GND	P	Ground
13	CPLD_IO_B1_99	IO-CMOS	CPLD IO row B1 pin 99
14	GND	P	Ground
15	CPLD_IO_B1_100	IO-CMOS	CPLD IO row B1 pin 100
16	GND	P	Ground

J66: Disk Drive Power Out 1

Board connector: 4-pin header, 0.2-inch, Molex 15-24-4449
Mating connector: Molex 15-24-4048 crimp housing

Header J66 supplies power to an optional external disk drive used for mass storage in the Catalyst LP Development Kit.

Warning:
J66 provides output power only. Do not connect to an input power source.

Pin	Name	Type	Description
1	V12S	PO	12 V power
2	GND	P	Ground
3	GND	P	Ground
4	V5S	PO	5 V normal operating power

J67: SATA 1

Board connector: 7-pin header, 0.05-inch, Molex 67800-5002
Mating connector:

Header J67 provides connection to a SATA disk drive. For a description of the external memory interfaces available on the Catalyst LP Development Kit, see External Memory Interfaces, page 15.

Pin	Name	Type	Description
1	GND	P	Ground
2	SATA1_TX+	IO	SATA 1 Transmit pair
3	SATA1_TX-		
4	GND	P	Ground
5	SATA1_RX-	IO	SATA 1 Receive pair
6	SATA1_RX+		
7	GND	P	Ground

J68: SATA 2

Board connector: 7-pin header, 0.05-inch, Molex 67800-5002
Mating connector:

Header J67 provides connection to a second SATA disk drive.

Pin	Name	Type	Description
1	GND	P	Ground
2	SATA2_TX+	IO	SATA 2 Transmit pair
3	SATA2_TX-		
4	GND	P	Ground
5	SATA2_RX+	IO	SATA 2 Receive pair
6	SATA2_RX-		
7	GND	P	Ground

Notes:
Development kits using a Catalyst LP revision A module support up to two SATA ports. SATA 2 on header J68 and the CF card slot J71 or IDE/PATA header J8 are mutually exclusive. If your application uses a CF card or IDE/PATA disk drive, only SATA 1 on header J67 is supported.

Development kit using a Catalyst LP revision B module support SATA 1, SATA 2, and IDE/PATA.

J71: CompactFlash

Board connector: Type I and II CompactFlash card header, 3M™ N7E50-Q516RB-40
Mating connector: CompactFlash card

The Catalyst LP Development Kit includes a CF card slot on socket J71. The 50-pin CF socket conforms to the CompactFlash standard for Type I and II cards operating at 3.3 V. For a description of the external memory interfaces available on the development kit, see External Memory Interfaces, page 15.

Notes:
The CF card socket J71 and the IDE/PATA header J8 are mutually exclusive. Install a CF card in socket J71 or connect an IDE/PATA disk drive to header J8.

For development kits using the Catalyst LP revision A module, SATA 2 on header J68 is mutually exclusive with the CF card slot J71 and the IDE/PATA header J8. If your application uses a CF card or IDE/PATA disk drive, SATA 2 is not supported.

P1: Serial 1 and Serial 3

Board connector: DB-9 plug-over-plug, Tyco 1734280-3
Mating connector: DB-9 socket

The dual plug P1 supports two full-feature EIA-232 serial ports. The connector shield is tied to chassis ground. For further details, see Serial Ports, page 20.

Pin		Name	Type	Description
Top	B1	DCD3	I	Data Carrier Detect 3
	B2	RXD3	I	Receive Data 3
	B3	TXD3	O	Transmit Data 3
	B4	DTR3	O	Data Terminal Ready 3
	B5	UART1_UART2_GND	P	Ground (through ferrite bead)
	B6	DSR3	I	Data Set Ready 3
	B7	RTS3	O	Request To Send 3
	B8	CTS3	I	Clear To Send 3
	B9	RI3	I	Ring Indicator 3
Bottom	A1	DCD1	I	Data Carrier Detect 1
	A2	RXD1	I	Receive Data 1
	A3	TXD1	O	Transmit Data 1
	A4	DTR1	O	Data Terminal Ready 1
	A5	UART1_UART2_GND	P	Ground (through ferrite bead)
	A6	DSR1	I	Data Set Ready 1
	A7	RTS1	O	Request To Send 1
	A8	CTS1	I	Clear To Send 1
	A9	RI1	I	Ring Indicator 1

J57: Serial 1 and Serial 3 Control Jumper

Type: 2-post header, 2 mm

Both Serial 1 and Serial 3 are driven by a Sipex SP3243 transceiver. These EIA-232 transceivers include automatic shutdown circuitry that allows the device to automatically shutdown, saving power when an EIA-232 cable is disconnected or a connected peripheral is turned off.

Notes:
If two connected serial ports enable automatic shutdown, neither port will turn on. Disable automatic shutdown if your device connects to another device that also uses automatic shutdown of the serial port.

Jumper J57 and the signal UARTx_SHUTDOWN control the operation of each EIA-232 transceiver. The on-board Super I/O Controller drives the signals UART1_SHUTDOWN and UART2_SHUTDOWN. For further details about these signals, see Carrier Board Super I/O Controller, page 23.

The following table describes the operation of the EIA-232 transceivers.

UARTx_SHUTDOWN	J57	Signal at Rcvr Input	Transceiver Operation
Logic level low	NC (default) or 1-2	yes or no	Shutdown mode Drivers are shut down
Logic level high	NC (default)	yes or no	Automatic shutdown circuitry is disabled Drivers remain active
Logic level high	1-2	yes	Automatic shutdown circuitry enabled Normal operation
Logic level high	1-2	no	Automatic shutdown circuitry enabled Drivers are shut down

P2: Maintenance Port

Board connector: DB-9 plug, Tyco 5747840-4
Mating connector: DB-9 socket

Connector P2 provides a serial maintenance port for the Catalyst LP embedded controller. The connector shield is tied to chassis ground. This maintenance serial port is extremely important in bring-up of a new carrier board design, troubleshooting, and software debug. For additional information about using this port, see Appendix C – Maintenance Port, page 60.

Notes:
The pinout of P2 does not follow the EIA-232 standard. The signals on pin 2 and pin 3 should be swapped for a standard DB-9 plug. If you are directed to use this port, use a gender changer or create a custom cable. Refer to forum topic 2556.

Pin	Name	Type	Description
1	NC		
2	DEBUG_TX	O	Transmit Data
3	DEBUG_RX	I	Receive Data
4	NC		
5	GND	P	Ground
6	NC		
7	NC		
8	NC		
9	NC		

U24: LPC Bus

Board connector: 2x10 shrouded header, 0.1-inch, Adam Tech BHR20VUA
Mating connector: IDC socket

The LPC bus is available for general-purpose I/O expansion on header U24. For further details, see Low Pin Count Bus, page 22.

Pin	Name	Type	Termination	Description
1	Reserved			
2	GND	P		Ground
3	LPC_FRAME#	O-LVTTL	PU 10kΩ V3.3S	LPC bus frame sync
4	NC			
5	BUF_RST#	O-3.3	PD 100kΩ	Buffered reset
6	V5S	PO		Normal operating 5 V
7	LPC_AD3	IO-LVTTL	PU 5kΩ V3.3S	LPC bus address/data 3
8	LPC_AD2	IO-LVTTL	PU 5kΩ V3.3S	LPC bus address/data 2
9	V3.3S	PO		Normal operating 3.3 V
10	LPC_AD1	IO-LVTTL	PU 5kΩ V3.3S	LPC bus address/data 1
11	LPC_AD0	IO-LVTTL	PU 5kΩ V3.3S	LPC bus address/data 0
12	GND	P		Ground
13	SMB_CLK	O-LVTTL	PU 10kΩ V3.3A	SMBus clock
14	SMB_DATA	IO-LVTTL	PU 10kΩ V3.3A	SMBus data
15	V3.3	PO		3.3 V primary supply
16	INT_SERIRQ	IO-LVTTL	PU 5kΩ V3.3S	LPC bus interrupt
17	GND	P		Ground
18	PM_CLKRUN#	IO-LVTTL	PU 8.25kΩ V3.3S	Initiates active clock output from LPC bus master
19	LPCPD#	O-LVTTL		(For details, contact Eurotech)
20	NC			

U27: Super I/O Controller GPIO and Embedded Controller GPIO

Board connector: 2x10 terminal strip, 2 mm, Samtec TMM-110-03-T-D
Mating connector: Samtec TCSD series socket

The Catalyst LP Development Kit includes nine GPIO signals on header U27. Nine pull-up resistors connect to U27 for termination of each GPIO. Two GPIOs connect directly to the Catalyst LP embedded controller, while the remaining seven GPIOs connect to the Super I/O Controller located on the carrier board. For further details, see General-Purpose Inputs and Outputs, page 22.

Pin	Name	Type	Description
1	GPIO1	IO-CMOS	Embedded controller GPIO
2	PU1		100kΩ pull-up resistor to V3.3S
3	GPIO2	IO-CMOS	Embedded controller GPIO
4	PU2		100kΩ pull-up resistor to V3.3S
5	GPIO3	IO-3.3	Super I/O Controller GP61
6	PU3		100kΩ pull-up resistor to V3.3
7	NC		
8	PU4		100kΩ pull-up resistor to V3.3
9	GPIO5	IO-3.3	Super I/O Controller GP56
10	PU5		100kΩ pull-up resistor to V3.3
11	GPIO6	IO-3.3	Super I/O Controller GP57
12	PU6		100kΩ pull-up resistor to V3.3
13	GPIO7	IO-3.3	Super I/O Controller GP50
14	PU7		100kΩ pull-up resistor to V3.3
15	GPIO8	IO-3.3	Super I/O Controller GP51
16	PU8		100kΩ pull-up resistor to V3.3
17	GPIO9	IO-3.3	Super I/O Controller GP31
18	PU9		100kΩ pull-up resistor to V3.3
19	GPIO10	IO-3.3	Super I/O Controller GP46
20	PU10		100kΩ pull-up resistor to V3.3

U47: I/O Expansion

Board connector: 2x10 terminal strip, 2 mm, Samtec TMM-110-03-T-D
Mating connector: Samtec TCSD series socket

The carrier board includes an I/O expansion port on header U47 providing eight GPIO signals that are accessible using the SMBus. Eight pull-up resistors connect to U47 for termination of each GPIO. For further details, see General-Purpose Inputs and Outputs, page 22.

Pin	Name	Type	Description
1	SMB_GPIO0	IO-3.3	I/O Expansion P0
2	SMB_PU0	P	10kΩ pull-up resistor to V3.3S
3	SMB_GPIO1	IO-3.3	I/O Expansion P1
4	SMB_PU1	P	10kΩ pull-up resistor to V3.3S
5	SMB_GPIO2	IO-3.3	I/O Expansion P2
6	SMB_PU2	P	10kΩ pull-up resistor to V3.3S
7	SMB_GPIO3	IO-3.3	I/O Expansion P3
8	SMB_PU3	P	10kΩ pull-up resistor to V3.3S
9	SMB_GPIO4	IO-3.3	I/O Expansion P4
10	SMB_PU4	P	10kΩ pull-up resistor to V3.3S
11	SMB_GPIO5	IO-3.3	I/O Expansion P5
12	SMB_PU5	P	10kΩ pull-up resistor to V3.3S
13	SMB_GPIO6	IO-3.3	I/O Expansion P6
14	SMB_PU6	P	10kΩ pull-up resistor to V3.3S
15	SMB_GPIO7	IO-3.3	I/O Expansion P7
16	SMB_PU7	P	10kΩ pull-up resistor to V3.3S
17	NC		
18	V3.3S	PO	Normal operating 3.3 V
19	V3.3A	PO	“Always” power
20	GND	P	Ground

System Specifications

Power Supply

The Catalyst LP Development Kit accepts input power on jack J29, page 39. For a description of the power supply, see Power Supply Architecture, page 25.

Symbol	Parameter	Min	Typ.	Max	Units
AC Power Adapter					
V_{OUT}	Supply voltage		12		V
I_{OUT}				5	A
System Power Outputs					
V3.3	Primary supply voltage	3.135	3.3	3.465	V
V3.3A	"Always" power	3.135	3.3	3.465	V
V3.3S	Normal operating power	3.135	3.3	3.465	V
V5A	"Always" power	4.75	5.0	5.25	V
V5S	Normal operating power	4.75	5.0	5.25	V
V12S			12		V
V_ON			12		V
SWX_ONOFF# (note 2)					
V_{IH}	High-level input voltage	2.5	5		V
V_{IL}	Low-level input voltage			1.0	V
R_{PU}	Pull-up resistance		10		kΩ
V_{PU}				5	V

Note:

2. SWX_ONOFF# connects to the Catalyst LP signal BTN_ONOFF# through a 0 Ω resistor on the carrier board. The module includes a pull-up resistor to V5A.

Electrical

This section provides electrical specifications for the Catalyst LP Development Kit. For additional details about termination of individual signals, see the signal connectors in Signal Headers, page 32.

USB

The Catalyst LP Development Kit provides five full-function USB host ports: J3, J4, J6. Each port supplies 5 V power through a power switch with over-current detection. For a description of the USB host ports, see USB, page 17.

Symbol	Parameter	Min	Typ.	Max	Units
USB Host Ports					
I_{USB}	USB current			500	mA

Carrier I²C Bus

The Catalyst LP Development Kit includes an external connection to the carrier I²C bus on connector J33, page 40. For a description of this bus, see Carrier I²C Bus, page 18.

Symbol	Parameter	Min	Typ.	Max	Units
CARRIER_I2C_SDA, CARRIER_I2C_SCL					
$F_{CARRIER\_I2C\_SCL}$	Bus clock	100		400	kHz
R_{PU}	Pull-up resistance (note 3)		10		kΩ
V_{PU}				3.3	V

Notes:

3. CARRIER_I2C_SDA and CARRIER_I2C_SCL include pull-up resistors to V3.3A on the carrier board.

SMBus

The Catalyst LP Development Kit includes an external connection to the SMBus on connector J32, page 40. For a description of this bus, see System Management Bus, page 19.

Symbol	Parameter	Min	Typ.	Max	Units
SMB_CLK, SMB_DATA, SMB_ALERT#					
F_{SMB_CLK}	Bus clock	10		100	kHz
R_{PU}	Pull-up resistance (note 4)		10		kΩ
V_{PU}				3.3	V

Notes:

4. SMB_CLK, SMB_DATA, and SMB_ALERT# include pull-up resistors to V3.3A on the Catalyst LP.

Touch Panel Controller

A Hampshire TSHARC USB controller and separate analog multiplexer included on the carrier board drives a resistive touch panel on header J26, page 38 or header J27, page 38. Standard systems include a 4-wire touch panel. All touch-panel signals include protection diodes. For a description of this interface, see Touch Panel Controller, page 21.

Symbol	Parameter	Min	Typ.	Max	Units
V_{DD}	Supply voltage		5.0		V

Reset Signals

The Catalyst TC Development Kit includes two reset signals. For a description of these signals, see Reset Signals, page 22.

Symbol	Parameter	Min	Typ.	Max	Units
BUF_RST#					
V_{OH}	High-level output voltage I_{OH} = -24 mA, V_{CC} = 3.3 V	2.2	3.3		V
V_{OL}	Low-level output voltage I_{OL} = 24 mA, V_{CC} = 3.3 V			0.55	V
R_{PU}	Pull-down resistance		100		kΩ
V_{PU}		0			V
SWX_RESET# (note 5)					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
R_{PU}	Pull-up resistance		10		kΩ
V_{PU}				3.3	V

Notes:

5. SWX_RESET# connects to the Catalyst TC signal FP_RESET# through a 0Ω resistor on the carrier board. The module includes debounce circuitry and a pull-up resistor to V3.3S.

General-purpose Inputs and Outputs

The Catalyst LP Development Kit provides twenty five GPIO on header U27, page 50, header U47, page 51 and header J64, page 46. For a description of these signals, see General-Purpose Inputs and Outputs, page 22.

Symbol	Parameter	Min	Typ.	Max	Units
GPIO1, GPIO2, CPLD_IO_B1_xx (note 6)					
V_{IH}	High-level input voltage	1.7	3.3		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage I_{OH} = -0.1 mA, V_{CC} = 3.3 V	V_{CC}-0.2			V
V_{OL}	Low-level output voltage I_{OL} = 0.1 mA, V_{CC} = 3.3 V			0.2	V
GPIO3-10 (note 7)					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage I_{OH} = -4 mA	2.4			V
V_{OL}	Low-level output voltage I_{OL} = 8 mA			0.4	V
SMB_GPIO0-7 (note 8)					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage I_{OH} = -8 mA, V_{CC} = 3.0 V	2.6			V
V_{OL}	Low-level output voltage I_{OL} = 8 mA, V_{CC} = 3.0 V			0.5	V

Notes:

6. Specifications per the Altera MAX II Device Handbook, August 2009 (MII5V1-3.3).
7. Specifications per the SMSC SCH3116 Super I/O Controller data sheet.
8. Specifications per the NXP PCA9554 Product data sheet, Rev. 07 – 13 November 2006.

System I/O Control

The Super I/O Controller supports common I/O capabilities on the development kit that include several discrete I/O. One of these I/O controls an external LED on J55, page 45. For additional details this signal, see Carrier Board Super I/O Controller, page 23.

Symbol	Parameter	Min	Typ.	Max	Units
SLP_LED (note 9)					
V_{OH}	High-level output voltage I_{OH} = -6 mA	2.4	3.3		V
V_{OL}	Low-level output voltage I_{OL} = 12 mA			0.4	V

Notes:

9. Specifications per the SMSC SCH3116 Super I/O Controller data sheet.

VGA Output

As a secondary display option, the Catalyst LP Development Kit provides a direct connection to a VGA display on J61, page 45. For a description of the VGA display output, see VGA Display, page 21.

Symbol	Parameter	Min	Typ.	Max	Units
R_{VGA}	Display cable impedance		75		Ω
DDC_DATA, DDC_CLK					
R_{PU}	Pull-up resistance (note 10)		10		kΩ
V_{PU}			5		V

Notes:

10. DDC_DATA, DDC_CLK include pull-up resistors to V5S.

Intel High Definition Audio

The Catalyst LP Development Kit provides a connection to an external codec that complies with the Intel High Definition Audio specification. For a description of the audio interface, see Audio Interface, page 24.

Symbol	Parameter	Min	Typ.	Max	Units
HDA (note 11)					
V_{CC}	Supply voltage		3.3		V
V_{IH}	High-level input voltage	$0.65*V_{CC}$			V
V_{IL}	Low-level input voltage			$0.35*V_{CC}$	V
V_{OH}	High-level output voltage I_{OH} = -500 µA	$0.9*V_{CC}$			V
V_{OL}	Low-level output voltage I_{OL} = 1500 µA			$0.10*V_{CC}$	V
F_{HDA_SDIx}	Data rate		24		Mbps

Note:

11. Specifications per the Intel High Definition Audio Specification Revision 1.0.

Audio Codec

The IDT 92HD71B8 4-channel HD audio codec provides the audio interface for the Catalyst LP Development Kit. This audio codec supports three audio inputs and three audio outputs on socket J20, page 37, socket J23, page 37, socket J53, page 44, and socket J54, page 44.

In addition, the codec provides an optional S/PDIF output on J19, page 36 and a digital microphone input on J22, page 37. For a description of the audio interface, see Audio Interface, page 24.

Symbol	Parameter	Min	Typ.	Max	Units
D_{VDD}	Codec digital supply voltage		3.3		V
A_{VDD}	Codec analog supply voltage		3.3		V
f_S	Sample rate		192		kHz
---	A/D sample resolution		24		bit
Line In					
V_{IN}	Full scale input voltage	0.707	1.03		Vrms
$Gain_{IN}$	Microphone boost	0		30	dB
R_{IN}	Input impedance		50		kΩ
C_{IN}	Input capacitance		15		pF
Line Out					
V_{OUT}	Full scale output voltage, 10kΩ load	0.707	0.758		Vrms
Headphone					
P_{OUT}	Output power, 32Ω load	31	42		mW(peak)
Digital Microphone (note 12)					
$V_{V\_DMIC\_L}$		1.8	3.3	3.3	V
$F_{DMIC\_CLK\_OUT}$			2.352		MHz

Notes:

12. Power for the digital microphone, V_DMIC_L, is dependent on the digital microphone selected. The carrier board supports 1.8 V or 3.3 V. Standard Catalyst LP Development Kits are configured for 3.3 V. Contact your local Eurotech technical support if your application requires 1.8 V.

General

This section provides general specifications for the Catalyst LP Development Kit.

Crystal Frequencies

Agencies certifying the Catalyst LP for compliance for radio-frequency emissions typically need to know the frequencies of on-system oscillators. The following table lists the frequencies of all crystals on the Catalyst LP and carrier board.

Crystals	Device	Typ.	Units
Catalyst LP			
X3	RTC	32.768	kHz
X4	Clock Generator	14.31818	MHz
X5	Embedded Controller	14.7456	MHz
X8	Ethernet Controller	25.000	MHz
Carrier Board			
OS1	Super I/O Controller	14.31818	MHz
X1	Touch Panel Controller	4.000	MHz

Real-Time Clock

The Catalyst LP includes a RTC function that retains the system date and time. To supply backup power when the power input is disconnected, the carrier board includes a long-life battery. For a description of this function, see Real-Time Clock, page 15.

Parameter	Typ.	Units
Accuracy per month @ 25°C	+/-55	sec
Battery	3	V
Operating temperature	-30 to +80	°C

Environmental

The Catalyst LP is designed to meet the environmental specifications listed in the following table. For additional details about the module, refer to the *Catalyst LP Design-In Guide (Eurotech document #110125-1000)*.

Parameter	Min	Typ.	Max	Units
Commercial operating temperature	0		+70	°C
Storage temperature	-40		+85	°C
Relative humidity, non-condensing	5		95	%

Appendix A – Reference Information

Product Information

Product notices, updated drivers, support material:
www.eurotech.com

Intel

Information about the Intel products, High Definition Audio specification, and LPC bus specification:
www.intel.com

Trusted Computing Group

Trusted Computer Group specification:
www.trustedcomputinggroup.org

SATA

Serial ATA specification:
www.sata-io.org

USB

Universal Serial Bus specification:
www.usb.org

SDIO Card

SD Card Association and SDIO specification:
www.sdcard.org

MMC Card

MultiMediaCard specification:
www.jedec.org

PCI SIG

PCI Express specification:
www.pcisig.com

PLX Technology

Information about the PCI Express switch:
www.plxtech.com

I^2C Bus

I^2C bus specification and information about the I/O expansion port:
www.nxp.com

SMBus

SMBus specification:
www.smbus.org

SMSC

Information about the Super I/O Controller:
www.smsc.com

National Semiconductor

Information about the LM75 temperature sensor:
www.national.com

TI

Information about the INA209 current/power monitor:
www.ti.com

IDT

Information about the HD audio codec:
www.idt.com

ACPI Specification

ACPI specification:
www.acpi.info

Appendix B – Board Revision

This manual applies to the current revision of the Catalyst LP Development Kit carrier board as given in the following sections. For the Catalyst LP revision history, refer to the *Catalyst LP Design-In Guide (Eurotech document #110125-1000)*.

Identifying the Board Revision

The revision number of the carrier board is printed on the underside of the printed wiring board. That number is 170125-400Rx, where "x" is the revision level of the PWB.

Carrier Board Revision History

The following is an overview of the revisions to the carrier board.

Revision B

Initial release

Appendix C – Maintenance Port

The serial port located on connector P2, page 49 is not available for application use. This port is intended for maintenance functions such as reprogramming the embedded controller, troubleshooting, and software debug. If you are directed to use this port when working with Eurotech staff, use the information provided in this appendix to connect the port to your computer.

Cable Connection

Connect any available serial port of your computer to connector P2 on your development kit. Use the DB9FF gender changer supplied with the Catalyst LP Development Kit or create a custom cable using the information given on page 49.

Port Settings

Use a terminal emulation application such as HyperTerminal or TeraTerm to access the maintenance port. Configure the port settings as follows:

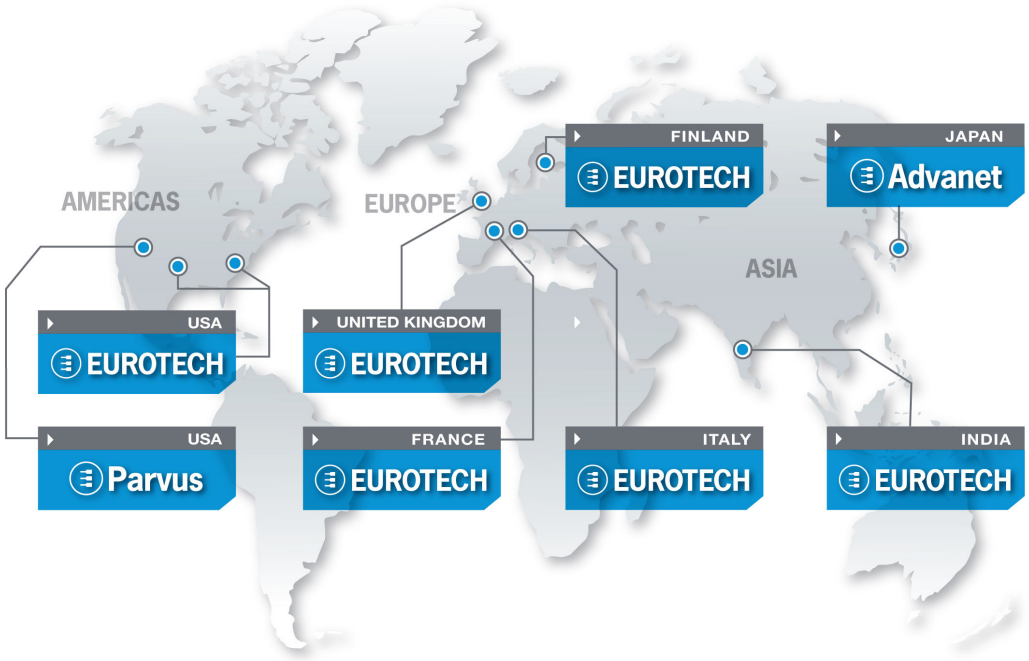
- Baud: 57600 bps
- Data bits: 8
- Parity: None
- Stop Bits: 1
- Flow control: none

Port Output

Connect power to the carrier board. The power LED D27 lights, and the following text is displayed on the terminal.

```
EUROTECH, INC.
Catalyst Core Module:  Embedded Controller Firmware
Copyright (c) 2007 EuroTech, Inc. All rights reserved.
==========================================================================
```

Eurotech Worldwide Presence



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