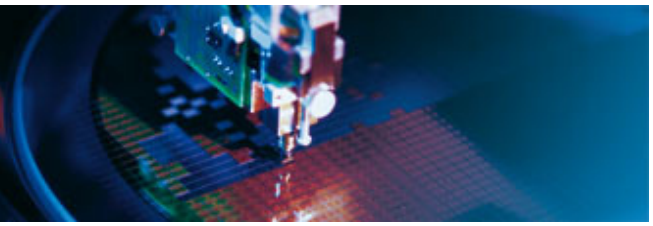
DESIGN-IN GUIDE



Catalyst TC

High Performance Module

Rev 3 – June 2011 – 110125-50003

www.eurotech.com

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Document Revision History

REVISION	DESCRIPTION	DATE
1	Preliminary release – For Internal Use Only	October 2010
2	Preliminary release – For Limited Distribution Only	February 2011
3	Initial release	June 2011

Table of Contents

Important User Information

In order to lower the risk of personal injury, electric shock, fire, or equipment damage, users must observe the following precautions as well as good technical judgment, whenever this product is installed or used.

All reasonable efforts have been made to ensure the accuracy of this document; however, Eurotech assumes no liability resulting from any error/omission in this document or from the use of the information contained herein.

Eurotech reserves the right to revise this document and to change its contents at any time without obligation to notify any person of such revision or changes.

Safety Notices and Warnings

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Eurotech assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Eurotech is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Installation in Enclosures

In the event that the product is placed within an enclosure, together with other heat generating equipment, ensure proper ventilation.

Do Not Operate in an Explosive Atmosphere

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Alerts that can be found throughout this manual

The following alerts are used within this manual and indicate potentially dangerous situations.

Danger, electrical shock hazard:
Information regarding potential electrical shock hazards:

- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Warning:
Information regarding potential hazards:

- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

Information and/or Notes:
These will highlight important features or instructions that should be observed.

Use an Appropriate Power Supply

- Only start the product with a power supply that conforms to the voltage requirements as specified in Power Supply, page 48. In case of uncertainty about the required power supply, please contact your local Eurotech Technical Support Team.
- Use power supplies that are compliant with SELV regulation.
- Avoid overcharging power-points.

Antistatic Precautions

To avoid damage caused by ESD (Electro Static Discharge), always use appropriate antistatic precautions when handing any electronic equipment.

Life Support Policy

Eurotech products are not authorized for use as critical components in life support devices or systems without the express written approval of Eurotech.

Warranty

For Warranty terms and conditions users should contact their local Eurotech Sales Office.
See Eurotech Worldwide Presence page 55 for full contact details.

WEEE

The information below is issued in compliance with the regulations as set out in the 2002/96/EC directive, subsequently superseded by 2003/108/EC. It refers to electrical and electronic equipment and the waste management of such products. When disposing of a device, including all of its components, subassemblies, and materials that are an integral part of the product, you should consider the WEEE directive.

This device is marketed after August 13, 2005 and you must separate all of its components when possible and dispose of them in accordance with local waste disposal legislations.

- Because of the substances present in the equipment, improper use or disposal of the refuse can cause damage to human health and to the environment.
- With reference to WEEE, it is compulsory not to dispose of the equipment with normal urban refuse and arrangements should be instigated for separate collection and disposal.
- Contact your local waste collection body for more detailed recycling information.
- In case of illicit disposal, sanctions will be levied on transgressors.

RoHS

This device, including all its components, subassemblies and the consumable materials that are an integral part of the product, has been manufactured in compliance with the European directive 2002/95/EC known as the RoHS directive (Restrictions on the use of certain Hazardous Substances). This directive targets the reduction of certain hazardous substances previously used in electrical and electronic equipment (EEE).

Technical Assistance

If you have any technical questions, cannot isolate a problem with your device, or have any enquiry about repair and returns policies, contact your local Eurotech Technical Support Team.

See Eurotech Worldwide Presence page 55 for full contact details.

Transportation

When transporting any module or system, for any reason, it should be packed using anti-static material and placed in a sturdy box with enough packing material to adequately cushion it.

Warning:
Any product returned to Eurotech that is damaged due to inappropriate packaging will not be covered by the warranty.

Conventions

The following table describes the conventions for signal names used in this document.

Convention	Explanation
GND	Digital ground plane
#	Active low signal
_P	Positive signal in differential pair
_N	Negative signal in differential pair

The following table describes the abbreviations for direction and electrical characteristics of a signal used in this document.

Type	Explanation
I	Signal is an input to the system
O	Signal is an output from the system
IO	Signal may be input or output
P	Power and ground
A	Analog signal
OD	Open-drain
CMOS	3.3 V CMOS
LVCMOS	1.05 V CMOS
LVTTL	Low Voltage TTL
3.3	3.3 V signal level
5	5 V signal level
HDA	High Definition Audio, 3.3 V signal
LVDS	Low Voltage Differential Signalling
PCIe	PCI Express signal, not 3.3 V tolerant
SATA	SATA differential signal
SDVO	Serial-DVO differential buffer, not 3.3 V tolerant
NC	No Connection
Reserved	Use is reserved to Eurotech

Some signals include termination on the Catalyst TC. The following table describes the abbreviations that specify the signal termination.

Termination	Explanation
PU	Pull-up resistor to the specified voltage
PD	Pull-down resistor
R	Series resistor
C	Series capacitor

Product Overview

The Catalyst TC is a high-performance, low-power module based on the Intel® Atom™ E6xx processor. It uses an integrated two-chip solution comprised of the Intel Atom processor and Intel® Platform Controller Hub (Intel® PCH EG20T). The Intel Atom processor contains an integrated 2D/3D graphics engine supporting hardware-accelerated graphics display and video processing capabilities, while the Intel PCH EG20T supports extensive I/O and data storage capabilities. The Catalyst TC conforms to the same footprint as Eurotech's Catalyst XL and Catalyst LP allowing existing customers to migrate to the Catalyst TC with minimal effort. The Catalyst TC allows embedded users to gain higher performance with greater energy efficiency.

An application-specific carrier board integrates with the Catalyst TC for a total production solution. This flexible, modular architecture enables easy customization and quick time-to-market. A Eurotech carrier board is available that implements several industry-standard interfaces allowing development across a broad spectrum of end-use applications.

The Catalyst TC is available with a variety of operating systems. Support is also available for the Java Virtual Machine and Eurotech's Everyware™ Software Framework, which offers an easy-to-use, Java-based development environment that minimizes time to market and allows for easy portability for future expansion.

Block Diagram

The following diagram illustrates the system organization of the Catalyst TC. Notice that the data connector has been divided into two sections for this illustration. Dotted lines indicate options.

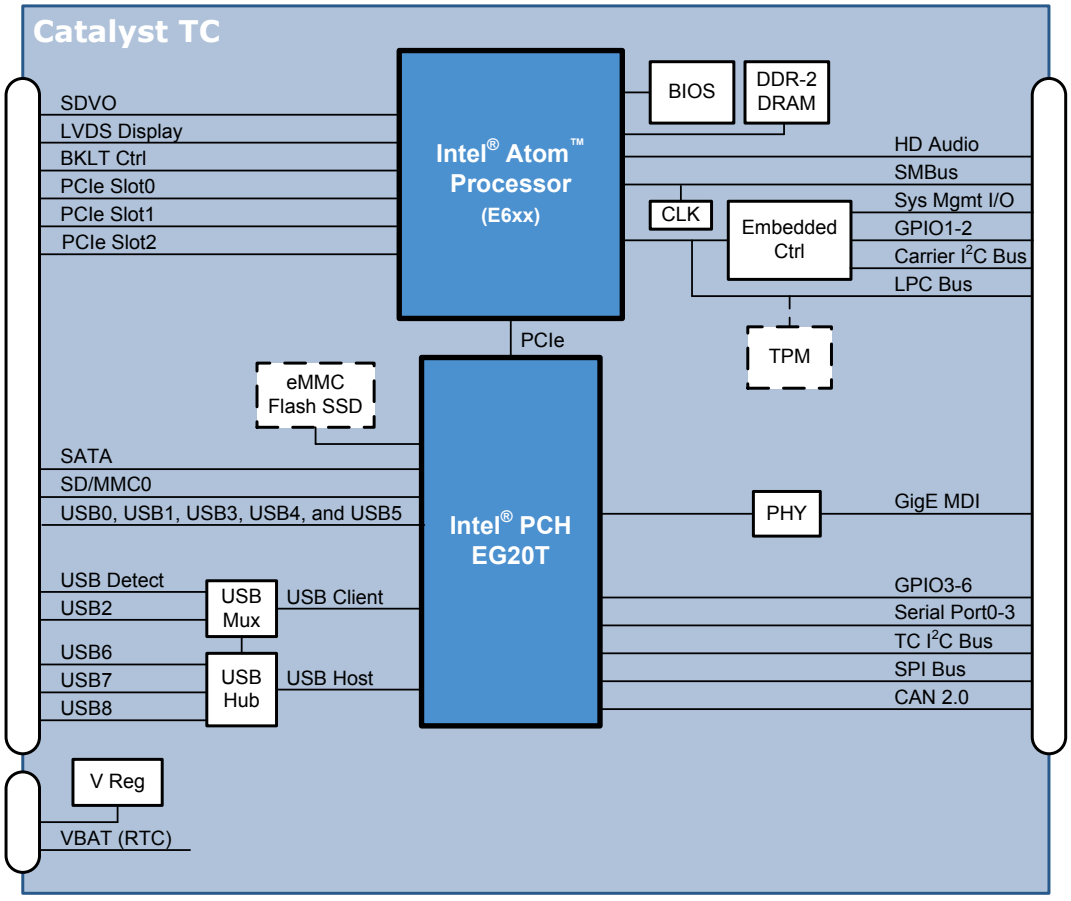


Figure 1. Catalyst TC Block Diagram

Features

Processor

- Intel® Atom™ E6xx processor, up to 1.6 GHz (Contact Eurotech for availability details)
- Intel® Platform Controller Hub EG20T

Integrated System Functions

- Embedded Controller
- Optional Trusted Platform Management (Contact Eurotech for details)

Memory

- Up to 2 GB DDR-2 DRAM
- Integrated system BIOS
- Battery-backed real-time clock
- Optional on-board eMMC flash SSD (Contact Eurotech for details)
- External memory support
  - SATA disk drive
  - USB disk drive
  - SD/MMC card
  - PCI Express card

Communications

- Three PCI Express one lane slots
- Nine Universal Serial Bus 2.0 ports including one USB client port
- Four serial ports (1 x full-function, 3 x RX/TX only)
- Gigabit Ethernet with physical layer transceiver
- CAN 2.0 interface
- Two I^2C buses
- SPI bus
- System Management Bus

User Interface and Display

- Independent LVDS display output and Serial Digital Video output
- Backlight interface with control signals for intensity and power

Inputs and Outputs

- Low Pin Count bus for general-purpose I/O expansion
- Six general-purpose inputs and outputs

Audio Interface

- Intel® High Definition Audio interface

Power Supply

- 3.3 V and 5 V main power inputs
- ACPI power management

Mechanical

- 67 mm x 100 mm dimensions
- Less than 10 mm total stack height

Design Checklist

Eurotech provides a host of services to ensure that your product is up and running from the first prototype release. We recommend the following process for every Catalyst TC carrier board design:

Kickoff Stage

During the Kickoff Stage, you will develop your block diagram and identify any customizations your application may require.

☐ **Gather your reference materials**

Eurotech provides several documents that include key information for designing a custom carrier board. Use the following resources and ask questions:

- Catalyst TC Design-In Guide
- Catalyst TC Development Kit User Manual
- Carrier Board Routing Guidelines
- 3D CAD models
- Reference Carrier Board Schematic
- Reference Carrier Board Bill of Materials

☐ **Define your requirements**

Define your system's requirement. Be sure to include requirements such as the product features, the input power, the type of transient protection on the power supply, connectivity to the module, and all I/O to your system.

☐ **Create a block diagram**

Create a block diagram of your proposed design. This step helps to formulate the best way to connect different devices to the module.

☐ **Identify customizations**

Identify any customizations that your application requires. Examples of customizations are custom LCD panel timings and backlight control, custom module configurations, or supporting a device that is not included on Eurotech's standard carrier board. Customizations may require updates to the BIOS.

☐ **Utilize the Catalyst TC Development Kit**

Utilize the Catalyst TC Development Kit for validating your proposed design. For example, if a USB device is to be used on USB port 6, test that device by connecting it to USB port 6 on the Catalyst TC Development Kit. This testing also allows you to validate your OS image with all required drivers loaded.

☐ **Kickoff review**

Early in the development of your carrier board, meet with your Eurotech representative to review your block diagram and discuss customizations. Incorporate any changes into your design.

Preliminary Design Stage

During the Preliminary Design Stage, you will finalize your block diagram, agree on customizations, and begin your preliminary schematic.

☐ **Use the reference schematic**

Use Eurotech's reference carrier board schematic as a starting point for your design. This schematic includes many commonly used interfaces. Using the same connectivity to the module will minimize the time spent in debugging your design.

- **Select components from the reference bill of materials**

  Select the same components as those used in Eurotech's reference carrier board bill of materials. Eurotech selects components that are optimized for embedded systems based on quality, low-power consumption, availability, reliability, and industrial temperature options. Selecting the same components also allows you to use the drivers Eurotech has already integrated with the OS builds.

- **Follow the design requirements and recommendations**

  Follow the design requirements and recommendations listed in Carrier Board Design, page 37 of this design-in guide. This section provides details about circuitry to include on the carrier board.

- **Preliminary design review**

  Stay in contact with your Eurotech representative during your preliminary design. Together, finalize your block diagram and agree on customizations needed. Continue to ask questions as you move towards finalizing your design.

Critical Design Stage

During the Critical Design Stage, you will finalize your schematic making sure that you have met all the module's electrical, thermal, and mechanical design requirements.

- **Implement power supply sequencing**

  Implement the exact power supply sequencing described in Power State Signals, page 27 of this design-in guide. The module has very specific power-on sequence requirements in order to power-up and operate correctly. Power sequencing the multiple voltage rails, as described in this section, is CRITICAL. If your design does not meet these requirements, the module will not boot.

- **Provide a system-level reset**

  Buffer and use the system reset signal RST# (J1 B56), described in Reset Signals, page 23, to reset all devices on the carrier board. The embedded controller controls the de-assertion of this signal with appropriate timings relative to power being stable. Timing requirements for power stable to reset de-asserted and reset de-asserted to device available are critical.

- **Create a power budget**

  Create a power budget that takes into account the current requirement of the module, as specified in Power Supply, page 48, and of the devices that are used with the module. Design your power supply to handle the maximum current requirement.

- **Determine thermal management**

  Determine what type of thermal management is required for your design. Use your power budget and the information provided in Thermal Management, page 35 of this design-in guide to design a heat spreader, if necessary.

- **Follow the module's mechanical requirements**

  Follow the exact mechanical requirements given in Mechanical Design, page 33 for mounting holes placement, position of the board-to-board connectors, and stack height on your carrier board design.

- **Use advanced layout and high-speed routing techniques**

  Follow the design constraints and routing guidelines described in Design Guidelines, page 37 of this design-in guide. Adhering to good design practices for high-speed PCB design is essential. You should have your schematic 95% complete, especially the high-speed signals and buses of the module, power sequencing, and system reset, before you start board layout. Meet with your Eurotech representative to review your schematic before you begin layout. After your layout is complete, meet again to review your complete design.

- **Have a strategy to debug your design**

  Review your strategy to bring-up and to debug your design. Ensure that you have included the necessary support in your design. The maintenance serial port is extremely important in bring-up of a new design. Eurotech highly recommends including an external connection to SMC_UART_RX (J1 B57) and SMC_UART_TX (J1 B106) on your carrier board.

- **Critical design review**

  Do an in-depth review of your finished design, including final schematic and board layout, to ensure that you have met all the requirements described in this checklist and throughout this design-in guide. Again, ask your Eurotech representative questions.

Prototype Bring-up Stage

Eurotech provides assistance in bringing-up your prototype at your site or ours. We have several tools that can assist the process including "carrier-board-free" BIOS releases, BIOS modifications to meet specific platform or test requirements, and power monitoring applications for the module.

- **Begin with the basics**

  Begin by checking basic functionality such as power, reset, and clocks. Verify that the power sequencing is as it should be and that the voltage regulator outputs are at nominal levels. Check that the system reset signal is asserted and deasserted according to the power sequencing requirements. Ensure all clocks necessary for bring-up are running properly.

- **Start with minimal devices**

  Minimize the number of devices required for bring-up. Using Eurotech's Bring-up BIOS is a good start. This BIOS disables several subsystems by default and allows each subsystem to be turned on as needed through the BIOS setup. Adding one device at a time will help determine which subsystem, if any, is having problems.

- **Utilize the maintenance port**

  Utilize the maintenance port output to identify problems during bring-up. This port provides important debug information including BIOS POST codes and error messages that enable you to monitor the operation of the module.

- **Use your Catalyst TC Development Kit**

  Use your Catalyst TC Development Kit to isolate problems. If a problem occurs during bring-up of your carrier board, try to duplicate the problem on the development kit.

- **Prototype bring-up review**

  Review your bring-up process and share lessons learned with your Eurotech representative.

Acceptance of Customizations

Eurotech is committed to your design success. Using our support services throughout the development cycle ensures a complete and robust solution with which to move forward.

- **Customization Acceptance**

  Meet with your Eurotech representative to discuss acceptance of any customizations and to plan the steps toward production of your Catalyst TC design.

Development Kit

The Catalyst TC Development Kit is designed to get the developer up and running quickly. The development kit includes the Catalyst TC, a standard development kit carrier board, and supporting peripheral devices. To provide flexibility and allow development across a broad spectrum of end-use applications, the carrier board maximizes the Catalyst TC functionality and implements many industry-standard interfaces. This configuration allows you to become familiar with the Catalyst TC functionality prior to customization for your specific application. In addition, the standard development kit carrier board provides a reference for custom carrier board design.

For a complete description of the Catalyst TC Development Kit, refer to the *Catalyst TC Development Kit User Manual (Eurotech document 110125-9001)*.

Related Documents

This guide provides details about the various features of the Catalyst TC and about how it creates a system that meets your application needs. It extends the information provided in the *Catalyst TC Development Kit User Manual* and is intended for hardware design engineers. Design details are provided as guidelines for custom carrier board design.

The following documents are also important resources for the Catalyst TC.

Document	
Catalyst XL - Catalyst TC Compatibility Technical Bulletin	110125-5002
Catalyst TC Carrier Board Routing Guidelines	110125-5001
Catalyst TC Development Kit User Manual	110125-9001
Catalyst Module Display Adapter User Manual	110122-4000
Catalyst Module Installation and Removal Technical Support Bulletin	110122-2014
Catalyst System Management Programmer Reference	110122-2021
Catalyst SMBus Programmer Reference	110122-2022
Catalyst I2C Bus Programmer Reference	110122-2023

Table 1. Related Documents

Check the Eurotech support site (http://support.eurotech-inc.com/) for errata reports and for the latest releases of these documents.

Software Specification

Eurotech provides an application-ready platform including BIOS, operating system, and development environment. This section gives a brief description of the software support available for the Catalyst TC. For additional details, contact your local Eurotech representative.

Operating System Support

The Catalyst TC is compatible with the following operating systems:

- Windows Embedded Standard
- Windows CE 6.0
- Windows® 7
- Wind River Linux
- Select real-time operating systems

For details about available support of each operating system, contact your local Eurotech representative.

BIOS

The Catalyst TC incorporates a custom system BIOS developed by Eurotech.

Software Development Kit

Eurotech has developed a Software Development Kit (SDK) and its Application Programming Interface (API) for the following functions:

- System Management
- SMBus
- I^2C bus

For details about the availability of these SDKs, contact your local Eurotech representative.

Everyware™ Software Framework

Everyware Software Framework (ESF) is an inclusive software framework that puts a middleware layer between the operating system and the OEM application. It provides industry-standard interfaces that shorten development time, simplify coding, and allow software to be ported from one Eurotech hardware platform to another. The Catalyst TC supports ESF. If your application requires ESF, contact your local Eurotech representative.

Information about ESF is available at http://esf.eurotech.com.

Hardware Specification

Core Processor

The Catalyst TC bases its architecture on an integrated two-chip solution comprised of the Intel Atom processor and Intel Platform Controller Hub EG20T (Intel PCH EG20T). In addition, the Catalyst TC fully integrates system functions that include system management and control implemented by an advanced chip level solution, tightly integrated power management controls, system BIOS firmware memory, and optional Trusted Platform Management (TPM) for industry-standard secure data encryption. This fully integrated and flexible feature set increases product readiness and compliance. The following sections describe the functionality and feature set of this processor technology as it relates to the Catalyst TC architecture.

Intel Atom Processor

At the core of the Catalyst TC is the Intel Atom E6xx processor. This processor's architecture offers high-performance processing with hardware-accelerated 2D/3D graphics display and video processing capabilities. For performance specifications, see Performance, page 49.

External Interrupts

The Catalyst TC provides several sources for external interrupts capable of generating a processor interrupt when the system is in power state S0. The following table lists these interrupt signals.

Signal	J1 Pin	Description
GPIO1	A108	Embedded controller GPIO
GPIO2	A3	Embedded controller GPIO
GPIO3	B40	Intel PCH EG20T GPIO2
GPIO4	B52	Intel PCH EG20T GPIO3
GPIO5	B54	Intel PCH EG20T GPIO4
SMB_ALERT#	A33	SMBus activity alert
INT_SERIRQ	A39	LPC bus interrupt
PCIE_WAKE#	B55	Standard I/O device wake event
PCIe slot 0 **PCIe slot 1**		PCIe message-based interrupts

Table 2. External Interrupts

For additional details about interrupts, including restrictions on INT_SERIRQ, contact your local Eurotech representative.

Intel Platform Controller Hub

The Intel Atom processor operates in conjunction with the Intel PCH EG20T. This companion device provides a wide range of capabilities that include USB, CAN, Gigabit Ethernet, I^2C, SPI, SATA, SD/MMC, GPIO, and serial ports. Subsequent sections describe each capability.

Embedded Controller

An embedded controller included on the Catalyst TC performs two main functions: ACPI power management and hardware monitoring. It connects to the Intel Atom processor using the LPC bus. Combined with the on-module power switch, the embedded controller supports ACPI power management. It ensures proper start-up, shutdown, and power saving transitions by sequencing the voltages and monitoring the input power and on-module voltage regulators. For further details about power management, see Power Supply Architecture, page 25.

As a second function, the embedded controller performs temperature monitoring, measuring the temperatures on the Intel Atom processor die and near the memory chips. You can also monitor temperatures on your carrier board by connecting an external temperature sensor to the embedded controller I^2C bus provided on connector J1.

In addition to the two main functions, the embedded controller performs extended functionality that includes optional battery management, device initialization, GPIO functions, and wake event control. For further details about the extended functionality, contact your local Eurotech representative.

Trusted Platform Management (option)

The optional on-module TPM function is compliant with the Trusted Computer Group specification version 1.2. This function provides public key generation, public key storage encryption/decryption, storage of hashes, key endorsement, and TPM initialization. As an option, the TPM is included on the LPC bus.

Memory

The Catalyst TC combined with a carrier board provides a variety of storage capabilities. The following sections describe the different types of memory supported and provide details about implementation.

Synchronous DRAM

Double Data Rate Synchronous DRAM (DDR-2) is used on the Catalyst TC for system main memory and frame buffer memory. Options up to 2 GB are available. The maximum burst bandwidth is 3.2 GB/s (4 B @ 800 MHz). The Intel Atom processor supports unified memory architecture in which the integrated 2D/3D graphics controller memory is “unified” with the system main memory. The default frame buffer is 8 MB with options in the BIOS Setup for selecting various sizes from 4 MB to 64 MB. Extended graphics memory space is available up to 256 MB. The graphics driver controls this size based on usage.

Non-Volatile Memory

The Catalyst TC includes non-volatile memory for system BIOS storage and a real-time clock (RTC) functionality.

BIOS and Configuration Data

A serial interface flash memory device stores the BIOS boot firmware, BIOS Setup settings, and module configuration data on the Catalyst TC. Standard configuration is 2 MB. The flash device connects to the Intel Atom Processor using a serial peripheral interface (SPI). This system BIOS memory supports pre-programmability at the device level, in-circuit programming on module, and updates using a run-time flash utility. In addition, programmable write protection is available using multiple flash sectors.

Real-Time Clock

The Intel Atom processor includes a RTC function. It retains the system date and time when the system is powered down as long as the 3.3 V “always” power or backup power is provided to the chip. For further details, see Real-Time Clock, page 52.

Flash SSD (option)

The Catalyst TC supports an optional on-module eMMC flash SSD. An 8 GB option is available in the standard module configuration. Options of 16 GB and 32 GB are available as custom module configurations. In addition to providing mass storage, this memory is a system boot option.

External Memory Interfaces

Five types of external memory interfaces provide mass storage options on a carrier board. The Catalyst TC supplies the signals for a SATA port, nine USB ports, a SD/MMC interface, and three PCIe slots that can connect external memory to the module. Connector J1 provides the signals for each option. Include support circuitry and connectors on your carrier board.

The high-speed differential and single-ended signals associated with these external memory interfaces require strict routing constraints on the carrier board. For routing guidelines, see Design Constraints, page 37.

SATA Disk Drive

The Catalyst TC provides a serial ATA (SATA) bus providing the option for a high-capacity, removable storage SATA disk drive. This interface supports the Serial ATA Specification, Revision 2.6 with data transfer rates of up to 3.0 Gb/s.

USB Mass Storage Device

A USB mass storage device can connect to one of nine USB ports on the Catalyst TC. Any USB device that has USB drivers installed on the Catalyst TC can connect to the USB host ports. For a description of these ports, see Universal Serial Bus, page 18.

SD Cards

The Catalyst TC includes a Secure Digital and MultiMediaCard (SD/MMC) interface for memory and I/O expansion. You can use this interface to implement a SD/MMC socket on a carrier board providing mass storage or to develop custom unique add-in cards.

The SD/MMC interface is compliant with the following specifications:

- SD Memory Card Specifications Part 1 Physical Layer Specification Ver2.0
- SDIO Card Specification Ver1.10
- MMC System Specification Ver4.1

In addition to the SD/MMC signals, connector J1 includes signals to control SD/MMC support circuitry on the carrier board. The interface includes signals to control a power FET and to drive a LED. For routing guidelines, see Design Constraints, page 37.

PCIe Memory Card

A PCIe x1 memory card can connect to one of three PCIe x1 slots available on the Catalyst TC. For a description of the PCI Express capability, see PCI Express, page 17.

Communications

The Catalyst TC supports several industry-standard channels for communication with peripheral and peer devices on the carrier board. These include PCI Express, USB, Gigabit Ethernet, I^2C bus, SPI bus, SMBus, CAN, and serial ports. The Catalyst TC does not limit flexibility by integrating fixed function I/O components. All communication signals are available on connector J1 providing flexibility and ease of implementation on the carrier board. This allows development of a unique carrier board optimized for your requirements.

PCI Express

A key capability of the Catalyst TC is its PCI Express (PCIe) support. Three of the four Intel Atom E6xx processor PCIe one lane (PCIe x1) ports are available on connector J1. The processor PCIe 0 port connects to the Intel PCH EG20T on the module. For details about the Catalyst TC's compliance with the PCI Express Base Specification, Revision 1.0a, contact your local Eurotech representative. These high-speed differential pairs require strict routing constraints on the carrier board and AC coupling. For routing guidelines, see Design Constraints, page 37.

The following table shows the mapping of connector J1 to the processor's PCIe ports.

Connector J1 Pin	Connector J1 Signal Name	Intel Atom Processor PCIe Port
A99, A98 **B95, B94**	PCIE_TX_SLOT0_P, PCIE_TX_SLOT0_N PCIE_RX_SLOT0_P, PCIE_RX_SLOT0_N	1
B99, B98 **A95, A94**	PCIE_TX_SLOT1_P, PCIE_TX_SLOT1_N PCIE_RX_SLOT1_P, PCIE_RX_SLOT1_N	2
B16, B17 **B18, B19**	PCIE_TX_SLOT2_P, PCIE_TX_SLOT2_N PCIE_RX_SLOT2_P, PCIE_RX_SLOT2_N	3

Table 3. PCIe Slot Mapping

An on-module clock buffer supplies the PCIe clocks for two of the three ports: PCIe slot 0 and PCIe slot 1. Additional input signals, CLK_SLOTx_OE#, control each reference clock. On a carrier board, these signals connect to the PCIe slots indicating the presence of a PCIe device. When activated, this signal enables the PCIe clock for the device. For electrical specifications, see PCIe Clock Generator, page 49.

Universal Serial Bus

The Catalyst TC provides nine Universal Serial Bus (USB) ports. Eight of the nine ports function as general-purpose USB host ports, while the ninth port functions as a USB host or USB client port. USB host ports support the USB 1.1 specification operating at low (1.5 Mbps) and full (12 Mbps) speeds and the USB 2.0 specification operating at high speed (480 Mbps). The USB client port supports full and high speeds. For electrical specifications, see Universal Serial Bus, page 49.

The following table describes the USB connectivity on the Catalyst TC.

Connector J1 Pin	Connector J1 Signal Name	Intel PCH EG20T USB Port	USB Hub Port
A71, A72	**USB0_P, USB0_N**	EG20T Port 0	
B71, B72	**USB1_P, USB1_N**	EG20T Port 1	
A68, A69	**USB2_P, USB2_N**	USB Client	Hub Port 4
B67, B68	**USB3_P, USB3_N**	EG20T Port 2	
A65, A66	**USB4_P, USB4_N**	EG20T Port 3	
B64, B65	**USB5_P, USB5_N**	EG20T Port 4	
A62, A63	**USB6_P, USB6_N**		Hub Port 1
B61, B62	**USB7_P, USB7_N**		Hub Port 2
B49, B50	**USB8_P, USB8_N**		Hub Port 3
		EG20T Port 5	Upstream Port

Table 4. USB Port Connectivity

USB Host

The Intel PCH EG20T provides USB0, USB1, USB3, USB4, and USB5 with the associated over-current detection inputs. Use these USB host ports to connect to devices external to the carrier board. USB mouse and keyboard are the most common client devices, but you can connect any USB device that has USB drivers installed on the Catalyst TC. A USB Hub located on the module provides USB6, USB7, and USB8. These USB ports do not include the associated over-current detection signals. When possible, connect these ports to devices on the carrier board.

In order to create a fully functioning USB host port, include the host power supply, current limiter circuits, EMI chokes, and over-voltage protection on your carrier board. The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The carrier board must supply the 5 V power required by client devices. Use a power switch with the corresponding over-current detection for each port. For routing guidelines, see Design Constraints, page 37.

USB Client or USB Host

USB2 functions as a USB host or USB client. The Catalyst TC includes a multiplexer and the input signal USB_CLIENT (J1 pin B53) to select the functionality. A logic-level high input selects the USB client; while a low-level low selects the USB host. When the port is used as a USB client, this signal can be used to detect a USB cable connection. Connect this pin to a 4.7kΩ pull up resistor to 3.3 V on the carrier board when a USB client is connected. When no client is connected or the port is used as a USB host, this signal should be actively driven low on the carrier board. As a USB host, this port includes an over-current detection signal.

Gigabit Ethernet

The Intel PCH EG20T includes a Gigabit Ethernet MAC that conforms to the IEEE 802.3 standard. This MAC device connects to a Realtek RTL8211CL Gigabit Ethernet Physical Layer Transceiver located on the module, supporting a Media Dependent Interface (MDI) for 10Base-T, 100Base-TX, and 1000Base-T applications. For information about this device, refer to www.realtek.com. In addition, the transceiver drives three programmable LED control signals which are available on connector J1. Include magnetics and an RJ-socket on your carrier board to complete the connection to your network. Contact your local Eurotech representative for additional information about the magnetics recommended for use on the carrier board. For routing guidelines, see Design Constraints, page 37.

I²C Bus

I²C (Inter-IC) bus is a multi-master, "two-wire" synchronous serial bus for communications between integrated circuits (ICs) and for addressing peripherals in a system. The Catalyst TC provides external connections to two I²C buses with the Catalyst TC acting as the bus master for each bus. The carrier I²C bus connects to the Catalyst TC embedded controller, while the TC I²C bus connects to the Intel PCH EG20T. This section provides details about the two I²C buses. For electrical specification, see I²C Bus, page 50.

Carrier I²C Bus

The carrier I²C bus connects to the embedded controller located on the Catalyst TC. The following diagram illustrates the I²C architecture on the Catalyst TC.

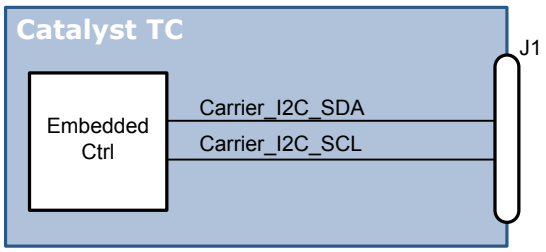


Figure 2. Carrier I²C Bus Architecture

When possible, use the TC I²C bus or SMBus to communicate with devices on the carrier board instead of the carrier I²C bus. When this bus is used on your carrier board, power all devices connected to it using the 3.3 V “Always” (V3.3A) power or isolate the devices from the bus when powered off. Notice that the module does not include termination on this I²C bus. Include 10kΩ pull-up resistors to V3.3A on the carrier board.

TC I²C Bus

The TC I²C bus connects to the Intel PCH EG20T located on the Catalyst TC and is available for external connections on connector J1. This bus supports the I²C Bus Specification, version 2.1. The following diagram illustrates the I²C architecture on the Catalyst TC.

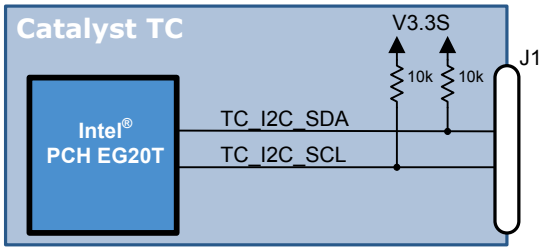


Figure 3. TC I²C Bus Architecture

Notice that the module includes 10kΩ pull-up resistors to V3.3S on the TC I²C bus. On your carrier board, power all devices connected to this bus using the V3.3S power or isolate the devices from the bus when powered off.

SPI Bus

The Serial Peripheral Interface (SPI) is a synchronous serial port that consists of a clock, transmit, receive, ground, and one or more device selects. Each device on the bus requires its own select line. Buses may be full or half duplex, clocking data one or both directions at the same time, respectively. The Catalyst TC provides an external connection on connector J1 to its SPI bus with the Intel PCH EG20T acting as the bus master. This bus supports transfer rates up to 5 Mbps.

System Management Bus

System Management Bus (SMBus) follows the same operating principles as I^2C. Similar to I^2C, SMBus is a "two-wire" interface allowing multiple devices to communicate with each other. Devices function as bus masters and bus slaves. SMBus enables communication between devices and allows connection of devices that require legacy software accessibility thru standard SMB addressing.

The Catalyst TC provides an external connection on connector J1 to its SMBus with the Intel Atom processor acting as bus master. This bus supports the SMBus Specification, Version 1.0. In addition, the module supports hardware alerting on the SMBus using the I/O signal SMB_ALERT#. Consider this capability when you are selecting between connectivity to this bus or the TC I^2C bus.

Notes:
SMBus is not compatible with all I^2C devices. Review the device data sheet carefully before connecting an I^2C device to the SMBus.

The following diagram illustrates the SMBus architecture.

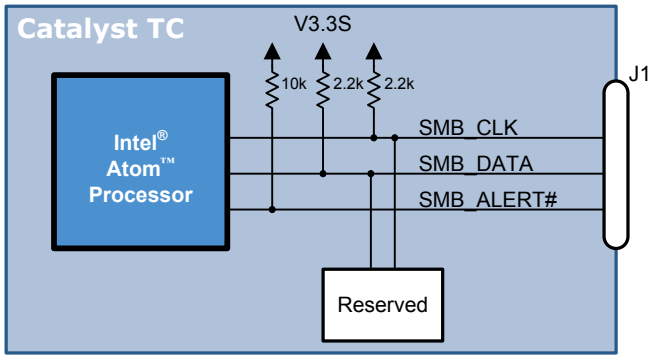


Figure 4. SMBus Architecture

Notice that the module includes pull-up resistors to V3.3S on the SMBus. On your carrier board, power all devices connected to this bus using the V3.3S power or isolate the devices from the bus when powered off. For electrical specifications, see SMBus, page 50.

The following table lists the addresses of the SMBus devices on the Catalyst TC.

Module SMBus Device	Address	Function
Reserved	1101 0010 1101 0011	Write Read

Table 5. SMBus Addresses

CAN 2.0B Bus

The Intel PCH EG20T includes a CAN controller supporting the CAN Protocol Version 2.0B Active supporting bit rates up to 1 Mbps. This bus is available on connector J1. Include a transceiver, common mode filter, and ESD protection on your carrier board.

Serial Ports

The Catalyst TC provides the signals for four serial ports on connector J1. These LVTTL signals route directly to the Intel PCH EG20T. If your application requires EIA-232/422/485, include transceivers on your carrier board. One serial port is a full-function UART supplying the full complement of modem control signals; while the remaining three serial ports provide receive and transmit signals only.

The following table describes the serial ports on the Catalyst TC.

Connector J1 Pin	Connector J1 Signal Name	Intel PCH EG20T Serial Port	Description	Baud Rate (bps)
A49 **A50** **A52** **A53** **A54** **A55** **A56** **B42**	**SP0_TX** **SP0_RX** **SP0_RTS** **SP0_RI** **SP0_DTR** **SP0_DSR** **SP0_DCD** **SP0_CTS**	0	Full-function	300 to 4M
B43 **B44**	**SP1_TX** **SP1_RX**	1	RX/TX only	300 to 1M
B45 **B46**	**SP2_TX** **SP2_RX**	2	RX/TX only	300 to 1M
B47 **B48**	**SP3_TX** **SP3_RX**	3	RX/TX only	300 to 1M

Table 6. Serial Ports

Display and User Interface

The Intel Atom Processor includes an integrated 2D/3D graphics engine supporting hardware-accelerated graphics display and video processing capabilities. The processor provides two independent display outputs. A LVDS output drives the primary display, while a Serial Digital Video Out (SDVO) interface drives a secondary display. In addition, the processor provides discrete backlight control signals.

This section summarizes the Catalyst TC graphics display and video processing capabilities. Display resolutions are specified at the maximum refresh rate and color depth. Higher resolutions may be possible at lower refresh rates and color depths. This relationship is due primarily to the increased processing bandwidth required at higher output resolutions.

LVDS Display and Backlight Control

The growing demand for higher resolution displays has been meet with design limitations on the interface between the LCD and graphics controller. Increased resolution LCDs require an increased clock speed, a larger number of data lines, and a higher power consumption. LVDS serial data transmission addresses these issues by providing a high-speed, low-power interface on a single pair of wires per channel. The Catalyst TC supplies a LVDS output to drive a primary display.

The following table summarizes the LVDS display output capabilities.

Feature	LVDS Display
Resolution	Up to 1280 x 768 at 60 Hz

Table 7. LVDS Display Capabilities

The LVDS display output consists of four LVDS data pairs, as well as a LVDS pixel clock, supporting 18-bit and 24-bit color. If your application requires transmission over a display cable greater than 7 inches, include an LVDS buffer/repeater on your carrier board to boost the data and pixel clock signals. Use controlled impedance cables that target 97 Ω. ± 20%. Cables should not introduce major impedance discontinuities that cause signal reflections. The differential pairs also require strict routing constraints on the carrier board. For routing guidelines, see Design Constraints, page 37.

Additional capabilities include the discrete signal L_VDDEN (J1 pin A32) that controls power to the display and an I²C interface (L_DDC_DATA on J1 pin B28, L_DDC_CLK on J1 pin A29) for communication with the LCD Display Data Channel (DDC). For electrical specifications, see LVDS Display and Backlight, page 50.

Backlight

Most LCDs include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Backlight inverters drive the panel backlights. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. To reduce power consumption, most backlight inverters include control signals to dim and turn off the backlight.

To support these features, the Catalyst TC supplies three backlight control signals and an I²C interface (L_CTLB_DATA on J1 pin B25, L_CTLA_CLK on J1 pin B29) for communication with the backlight. For electrical specifications, see LVDS Display and Backlight, page 50. The following table describes the three backlight control signals.

Signal	J1 Pin	Type	Description
L_BKLTCTL	B33	O	Controls the intensity of the backlight
L_BKLTEN	B32	O	Turns power to the backlight on or off
L_BKLTSEL0_GPIO#	B58	O	Selects backlight control (PWM vs. I²C)

Table 8. Backlight Control Signals

Serial Digital Video Out

In addition to the LVDS display output, the Intel Atom processor drives a secondary display on the SDVO interface. SDVO allows for an additional video interface using a PCIe x16 slot implemented on a carrier board or a direct connection to an on-board device. This secondary interface supports external devices that convert the SDVO protocol to DVI, HDMI, LVDS Analog-CRT, and TV-Out interfaces. The Catalyst TC supports only ADD2-N cards. ADD2-R cards are not supported. For recommended Intel/HP SDVO cards, contact your local Eurotech representative. The following table summarizes the SDVO capabilities.

Feature	SDVO
Resolution	Up to 1280 x 1024 at 85 Hz

Table 9. SDVO Display Capabilities

The SDVO interface includes seven high-speed differential pair signals. Routing the high-speed differential pairs on the carrier boards requires strict design constraints. For routing guidelines, see Design Constraints, page 37.

In addition, the SDVO interface includes an I²C interface (SDVO_CTLDATA on J1 pin A30, SDVO_CTLCLK on J1 pin B30). This bus connects to a SDVO panel DDC. The Catalyst TC does not include termination on the I²C signals. Include 3.3KΩ pull-up resistors to +2.5V on the carrier board. If your carrier board does not generate +2.5V and your design does not use the SDVO I²C signals, these signals can be pulled to V3.3S with 1MΩ resistors.

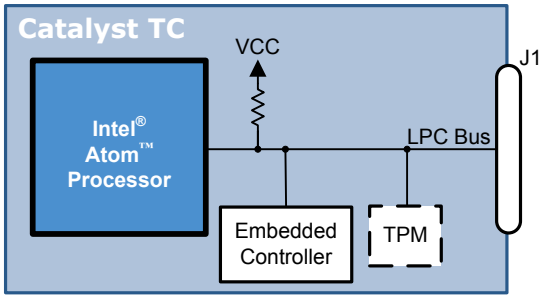
Inputs and Outputs

Several signals on the Catalyst TC support I/O expansion and system management. The module includes a Low Pin Count bus supporting legacy I/O capabilities and multiple discrete I/O signals performing system reset, power control, and general-purpose input and output. Connector J1 includes all I/O signals.

Low Pin Count Bus

In response to the transition from ISA-based systems, the Low Pin Count (LPC) bus provides a migration path for legacy I/O capabilities. This interface enables general-purpose I/O expansion and provides communication to low-bandwidth devices. For this purpose, the Intel Atom processor supplies a LPC bus supporting the LPC1.1 Specification. On the Catalyst TC, the LPC bus connects to the processor, the embedded controller, and an optional TPM.

The following diagram illustrates the LPC bus architecture.



Note:
1. For details about the termination on individual signals, see J1, page 42.

Figure 5. LPC Bus Architecture

Externally, the LPC bus provides general-purpose expansion. A common application on the carrier board includes a Super I/O Controller that provides I/O capabilities such as additional serial ports, keyboard, mouse, IrDA, and general-purpose I/O. Ensure that the LPC signals are routed as critical nets on your carrier board and include 10kΩ pull-up resistors to V3.3S on the LPC_ADx signals. For routing guidelines, see Design Constraints, page 37.

The LPC bus power down signal, LPCPD# (J1 pin B2), is not presently implemented. If this signal is needed for your specific application usage, contact your local Eurotech representative for functional details. In addition, the Catalyst TC does not support Direct Memory Access (DMA) on the LPC bus.

Reset Signals

One of two signals resets the circuitry on the module and carrier board. One signal originates from the module, while the second signal originates from the carrier board. The output signal RST# is buffered on the module; however, include additional buffering on the carrier board to drive multiple loads. The following table compares the reset signals.

Signal	J1 Pin	Type	Description
RST#	B56	O	Use as a power-on reset to reset all devices on the carrier board. Output is driven by the module, forces complete system hardware reset, and is used for proper reset timing and logic synchronization.
FP_RESET#	A59	I	Do not use this signal as a power-on reset. FP_RESET# will not be detected until RST# is de-asserted. Input initiates a hardware reset including the Intel Atom processor and Intel PCH EG20T.

Table 10. Reset Signals

In addition to the hardware resets, the input signal H_INIT# (J1 pin B3) initiates a soft reset of the module. For electrical specifications, see Reset Signals, page 51.

General-Purpose Input and Output

The Catalyst TC provides six general-purpose input and output (GPIO) signals, as described in the following table. For electrical specifications, see General-purpose Inputs and Outputs, page 51.

Signal	J1 Pin	Description
GPIO1	A108	Embedded controller GPIO
GPIO2	A3	Embedded controller GPIO
GPIO3	B40	Intel PCH EG20T GPIO2
GPIO4	B52	Intel PCH EG20T GPIO3
GPIO5	B54	Intel PCH EG20T GPIO4
GPIO6	A2	Intel PCH EG20T GPIO1

Table 11. GPIO Signals

GPIO1 and GPIO2 are software-controlled using the Catalyst System Management API. For details about this API, refer to the *Catalyst System Management Programmer Reference (Eurotech document #110122-2021)*. Future revisions of the API will support the Intel PCH EG20T GPIO.

Intel High Definition Audio

The Intel High Definition Audio (Intel HD Audio) Specification implements high quality audio in a PC environment. The specification defines a uniform interface between a host computer and audio codec specifying register control, physical connectivity, programming model, and codec architectural components. The Intel Atom processor provides an Intel HD Audio interface capable of supporting up to two external audio codecs. Docking functionality is supported allowing control of an external switch for isolation of the codec within a docking station during normal docking request and acknowledge cycles.

All Intel HD Audio signals are available on connector J1. The Intel Atom processor supports only 3.3 V signalling levels. For electrical specifications, see Intel High Definition Audio, page 51. Include audio codecs along with amplifiers, switches, and connectors on your carrier board. For routing guidelines, see Design Constraints, page 37.

Power Requirements

Power management is especially critical in high-performance systems that also require low power dissipation. Handheld and portable systems available today never really turn "off". They make use of power management techniques that cycle the electronics into power saving modes, but never fully remove power from the full system.

Embedded system designers using the Catalyst TC should have a clear understanding of how the system design allocates power usage. Create a power budget that takes into account the types of devices that are used with the Catalyst TC. This section provides information about power and power management on the Catalyst TC.

Low Power States

The Catalyst TC supports the Advanced Configuration and Power Interface (ACPI) version 3.0. Unlike previous power standards that were BIOS-based, ACPI allows OS-directed power management. It specifies an industry-standard interface for both hardware and software that facilitates power and thermal management. This section describes how the Catalyst TC makes use of the ACPI low power modes.

The ACPI specification defines the low power states for ACPI-compliant systems. The following table describes the states supported by the Catalyst TC.

State	Mode	Description
S0	Full Operation	All devices are operational with dynamic power management functions active.
S3	Standby or Sleep	The Intel Atom processor and Intel PCH EG20T are powered down. Active operating system context stored in DRAM is retained using low-power self-refresh. Wake events are active and enable a transition back to full operation.
S4	Hibernation	The Intel Atom processor, Intel PCH EG20T, and DRAM are powered down. Operating system context is saved to disk storage prior to powering down system voltage rails. Limited wake events are active. Resume to full operation is dependent on numerous system components including the disk storage device.
S5	Power down	The Intel Atom processor, Intel PCH EG20T, and DRAM are powered down. The embedded controller is active but may be in low-power mode. No operating system context is preserved.

Table 12. ACPI Power States

Wake events transition the Catalyst TC from a low-power state back to full operation. The following table lists the signals that can function as wake events. These signals are valid as wake event inputs in power state S3.

Wake Event	J1 Pin	Description
USB_CLIENT	B53	USB2 client detection when programmed as GPIO
PCIE_WAKE#	B55	Standard I/O device wake event signal
BTN_ONOFF#	B59	Power button

Table 13. Wake Events

Power Supply Architecture

The architecture of the power supply partitions the power generation across the Catalyst TC and the carrier board. The module requires 5 V and 3.3 V input voltages supplied by the carrier board. It is the responsibility of the carrier board designers to provide input power protection as required by their application. This is especially important if the power supply wires will be subject to EMI/RFI or ESD. On-module regulators generate the core power and all other powers required by the supporting circuitry. For electrical specifications and details about each power rail, see Power Supply, page 48.

Input Power Voltages

The following table describes the input power voltages required by the Catalyst TC.

Name	Power State	Description
V3.3A	S4 exit, S5 exit, S0 operation, and S3 operation	3.3 V “always” power for up/down circuitry only
V3.3S	S0 operation	3.3 V normal operating power
V3.3	S0 operation and S3 operation	3.3 V primary supply voltage for most of the on-board regulated voltages
V5A	S4 exit, S5 exit, S0 operation, and S3 operation	5 V “always” power for up/down circuitry only
V5S	S0 operation	5 V normal operating power
V_BATTERY		Backup power for the RTC

Table 14. Input Power Voltages

Each power rail should be routed as a power plane on your carrier board with sufficient bulk decoupling and local decoupling on each plane. For additional details about carrier board design, see Design Guidelines, page 37.

Notes:
The V5A rail should lead the V3.3A rail during ramp up.

The V5S rail should lead the V3.3S rail during ramp up or not lag by more than 0.7 V. It is acceptable for these two voltage rails to ramp up at the same time.

For an example circuit, see the Eurotech reference carrier board schematic.

The following diagram illustrates the layout of the Catalyst TC power supply.

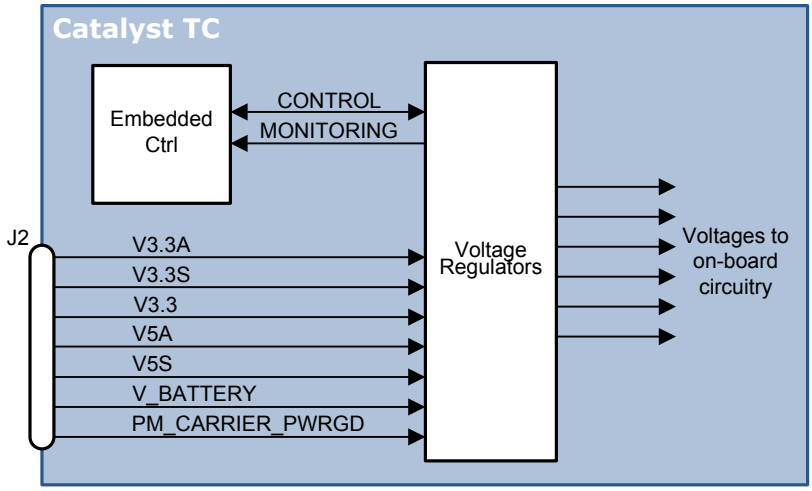


Figure 6. Power Supply Architecture

In addition to the input power voltages, connector J2, page 47 includes the signal PM_CARRIER_PWRGD. This input from the carrier board indicates that all input power voltages are fully operational and within tolerance.

Notes:
The carrier board must provide the PM_CARRIER_PWRGD signal to represent the readiness for operation.

The embedded controller functions, in conjunction with an on-module power switch, to control proper sequencing of voltages allowing for proper start-up, shutdown, and power saving transitions. In addition, it monitors input power voltages and the on-module voltage regulators. For additional details about the embedded controller, see Embedded Controller, page 15.

RTC Backup Power

The Catalyst TC includes a RTC function that retains the system date and time when the system is powered down as long as the 3.3 V “always” power or backup power is provided to the module. Including a long-life 3 V battery on a carrier board is a common method to supply backup power. Use series elements, such as a diode and resistor, on the V_BATTERY output from your carrier board based on your specific requirements.

On the Catalyst TC, the V_BATTERY power input has a diode-OR with V3.3A, as shown in the following diagram.

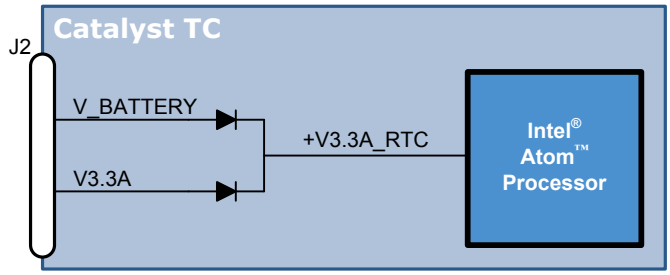


Figure 7. RTC Backup Power Architecture

For specifications, see Power Supply, page 48 and Real-Time Clock, page 52.

Power Switch

The input signal BTN_ONOFF# (J1 pin B59) controls a power switch included on the Catalyst TC. The function of the BTN_ONOFF# signal is dependent on the embedded controller/BIOS setup and the configuration of the operating system. The response of the system can be managed by this combination. On the standard development kit, this input is connected to a momentary button on the carrier board. Pressing this external momentary button turns the power on and off. For electrical specifications, see Power Supply, page 48.

The following table details the operation of the BTN_ONOFF#.

BTN_ONOFF#	Operation
Momentary assertion (less than 4 seconds)	On standard development kit: From shutdown, initiates a power-up sequence to full operation. From full operation, initiates an orderly shutdown sequence and turns off power. Options based on system configuration: From full operation, enters system sleep state. From sleep, returns to full operation.
Continuous assertion (greater than 4 seconds)	Initiates a “4 second over-ride” and turns off power without notification to the operating system.

Table 15. BTN_ONOFF#

Notes:
Once the V5A and V3.3A rails are applied, the BTN_ONOFF# signal is not detected for up to 500 ms.

Power State Signals

The Catalyst TC provides three control signals on connector J1 indicating the power state. The embedded controller drives the two power state signals, PM_EN_S0# (J1 pin B104) and PM_EN_S3# (J1 pin B107). The on-module power switch controls the remaining signal, PM_EN_PWR (J1 pin B105). For electrical specifications, see Power Supply, page 48.

The following table lists these signals with the power states and input power voltages active in each state.

State	Active power rails	PM_EN_PWR	PM_EN_S3#	PM_EN_S0#
S0	V3.3, V5S V3.3S V5A, V3.3A	High	Low	Low
S3	V3.3, V5A, V3.3A	High	Low	High
S4	V5A, V3.3A	Low	High	High
S5	V5A, V3.3A	Low	High	High

Table 16. Low Power States

Notes:
Implement the exact power supply sequencing as described in this section. The module has very specific power-on sequence requirements in order to power-up and operate correctly. Power sequencing the multiple voltage rails is CRITICAL. If your design does not meet these requirements, the module will not boot.

The following timing diagrams describe the relationship of the power state control signals on the Catalyst TC.

Power-on initiated by power button press

During system power-on, the falling edge of BTN_ONOFF# drives PM_EN_PWR high. A hardware latch on the Catalyst TC controls PM_EN_PWR. The embedded controller monitors BTN_ONOFF# until the rising edge of BTN_ONOFF#. If the power button was pressed for less than 4 seconds and the power is presently off, a power-on sequence will begin. After sampling BTN_ONOFF# high, the embedded controller waits for PM_CARRIER_PWRGD to be asserted high before driving PM_EN_S3# active (logic level low). The embedded controller will wait up to 1 second for PM_CARRIER_PWRGD. If PM_CARRIER_PWRGD is not asserted within one second, the embedded controller will print an error message on the maintenance port and halt the power-on sequence.

After PM_CARRIER_PWRGD is asserted, S3 power rails internal to the Catalyst TC are enabled with the assertion of PM_EN_S3# and powered by V3.3. PM_CARRIER_PWRGD is not monitored for 10 ms following the assertion of PM_EN_S3#. This provides time for the carrier board power supply to power all rails required in S3. If PM_CARRIER_PWRGD is not asserted within 100 ms, the embedded controller will print an error message on the maintenance port and halt the power-on sequence.

After the S3 power rails are within specification on the module and on the carrier board, the embedded controller asserts PM_EN_S0# (logic level low). The time from PM_EN_S3# active to PM_EN_S0# active depends on how quickly the carrier board supplies V3.3. Typically, the Catalyst TC transitions from S3 to S0 within 50 ms. Once again PM_CARRIER_PWRGD is not monitored for 10 ms following the assertion of PM_EN_S0#. This allows the carrier board time to provide all power rails required in S0. On-module regulators for the processor and other devices are powered on at this time. The embedded controller monitors on-module power good signals as well as the PM_CARRIER_PWRGD signal from the carrier board to verify all S0 rails are within specification. If PM_CARRIER_PWRGD is not asserted within 1 second, the embedded controller will print an error message on the maintenance port and halt the power-on sequence. A minimum of 100 ms after all S0 power supplies are on, the RST# signal is de-asserted.

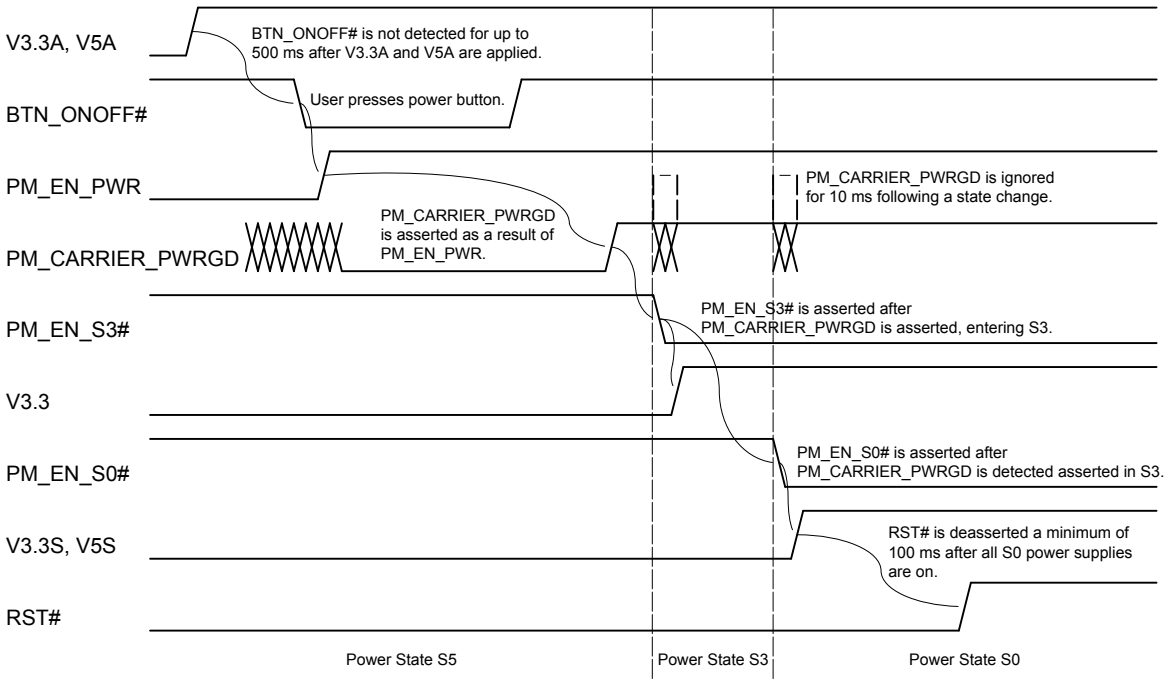


Figure 8. Power-on initiated by power button press

Standby (Enter S3)

The following diagram shows the Catalyst TC transitioning from S0 to S3. This transition can be initiated by the operating system or the BTN_ONOFF# input in combination with the operating system. The PM_EN_S0# signal will be de-asserted, and all S0 power rails on the Catalyst TC module will be turned off. The PM_CARRIER_PWRGD signal is not monitored for 10 ms following the de-assertion of PM_EN_S0#. This allows the carrier board S0 power rails to be turned off and PM_CARRIER_PWRGD to provide status of the power rails remaining on in S3. RST# will be de-asserted while the system is in S3.

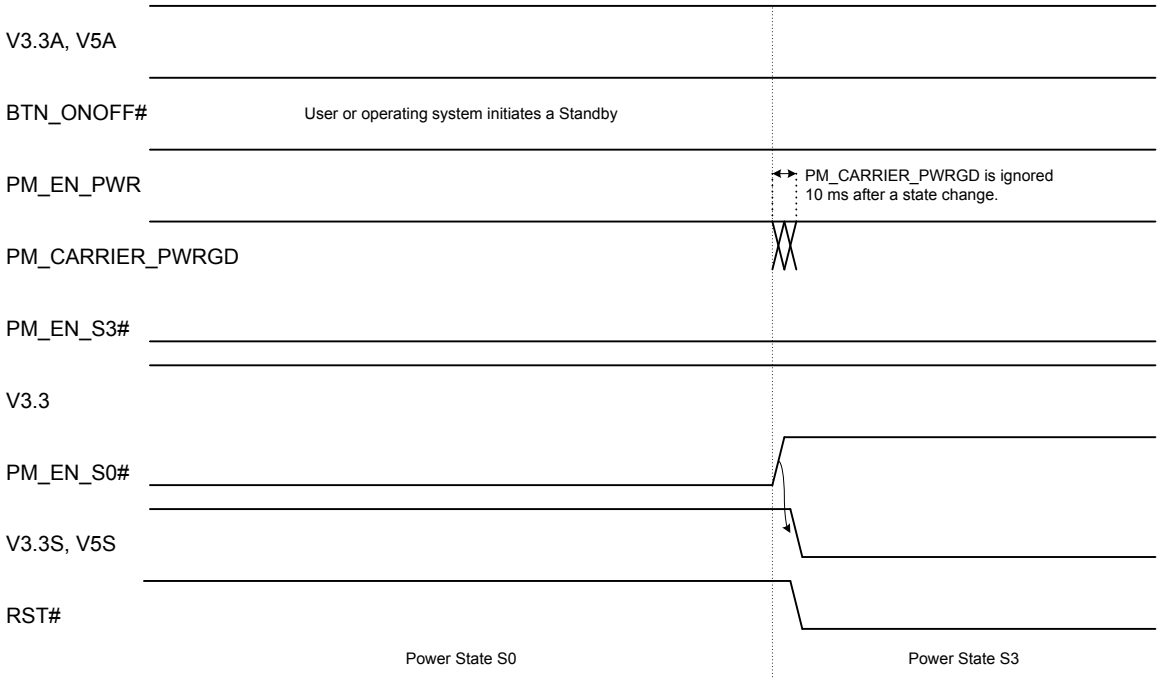


Figure 9. Standby (Enter S3)

Standby (Exit S3)

The following diagram shows the system exiting S3. The system may wake from S3 because of any event shown in Table 12, page 25. PM_EN_S0# will be asserted causing all S0 power rails on the Catalyst TC to be turned on. PM_CARRIER_PWRGD will not be monitored for 10 ms after PM_EN_S0# is de-asserted. This provides time for all S0 power rails on the carrier board to be turned on and within specification. A minimum of 100 ms after all on-module supplies and carrier board S0 power supplies are within specification, RST# will be de-asserted.

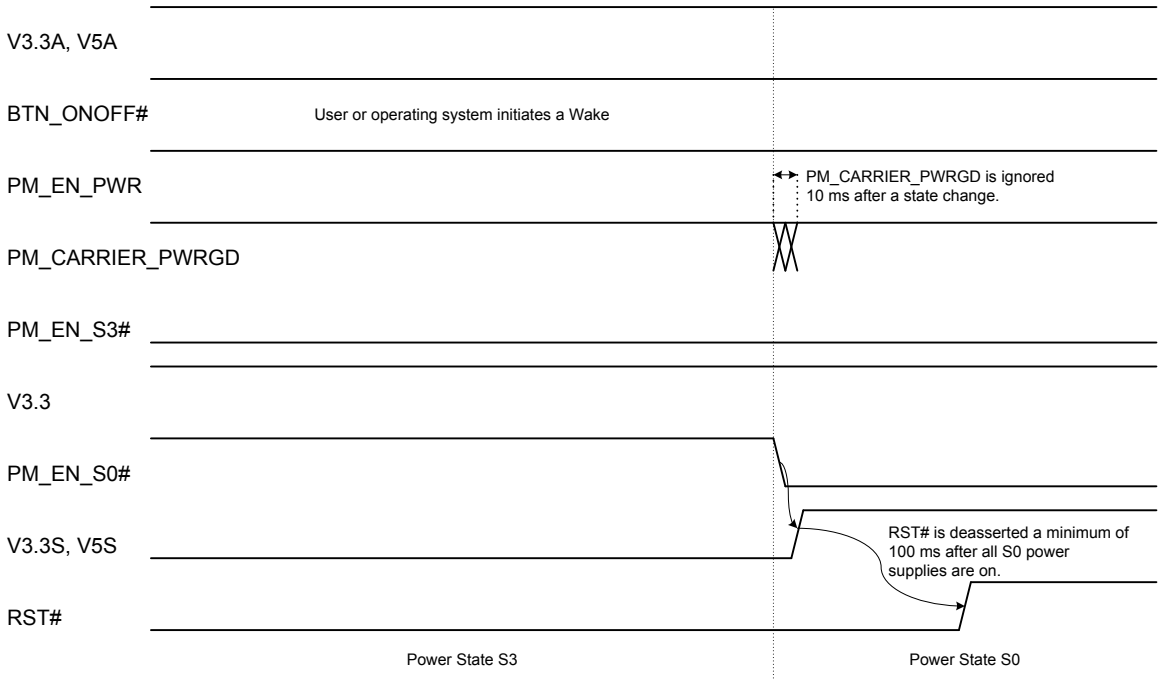


Figure 10. Standby (Exit S3)

Power off initiated by power button press

The following diagram shows a system powering off because of an assertion of the BTN_ONOFF# signal. Depending on operating system settings, a system may power off or sleep due to asserting BTN_ONOFF#. If set for a power off, the operating system will save all information needed and signal the embedded controller to perform a graceful shutdown. PM_EN_S0# will be de-asserted, followed by PM_EN_S3# and PM_EN_PWR being de-asserted. RST# will be asserted when in S5.

If BTN_ONOFF# is asserted for more than 4 seconds, a “4 second over-ride” will be initiated and the power will be turned off without notification to the operating system.

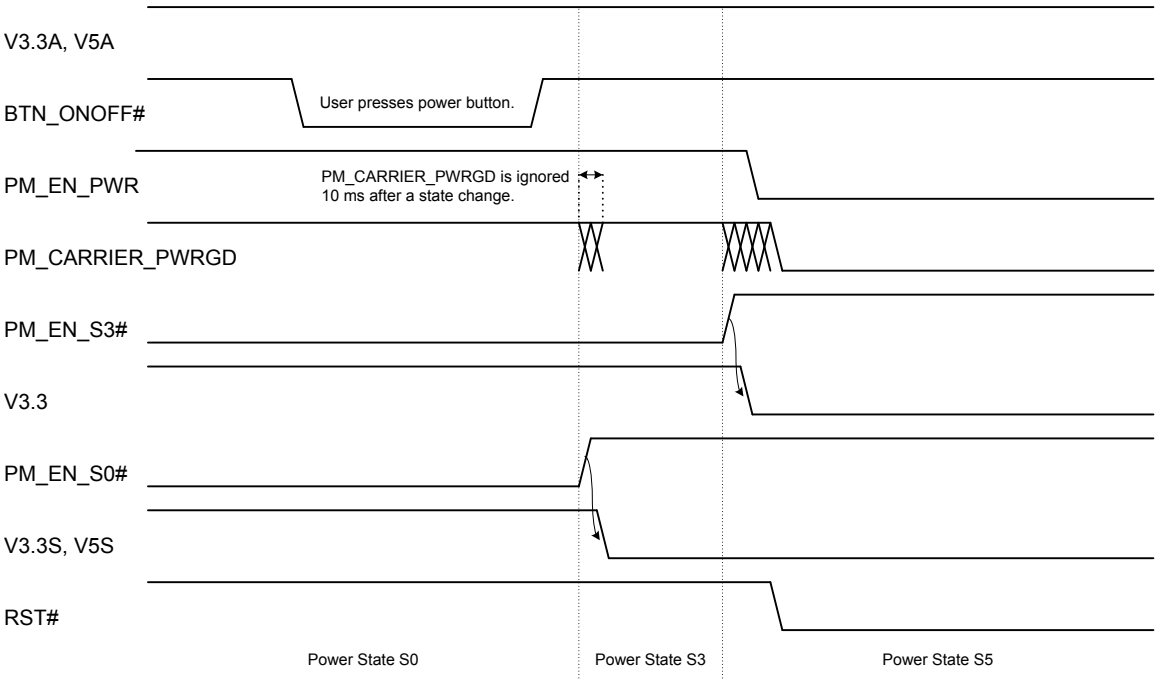


Figure 11. Power off initiated by BTN_ONOFF#

System shutdown initiated by operating system

The following diagram shows a system powering at the request of the operating system. The user could initiate this via software control. The operating system will save all information needed and signal the embedded controller to perform a graceful shutdown. PM_EN_S0# will be de-asserted, followed by PM_EN_S3# and PM_EN_PWR being de-asserted. RST# will be asserted when in S5.

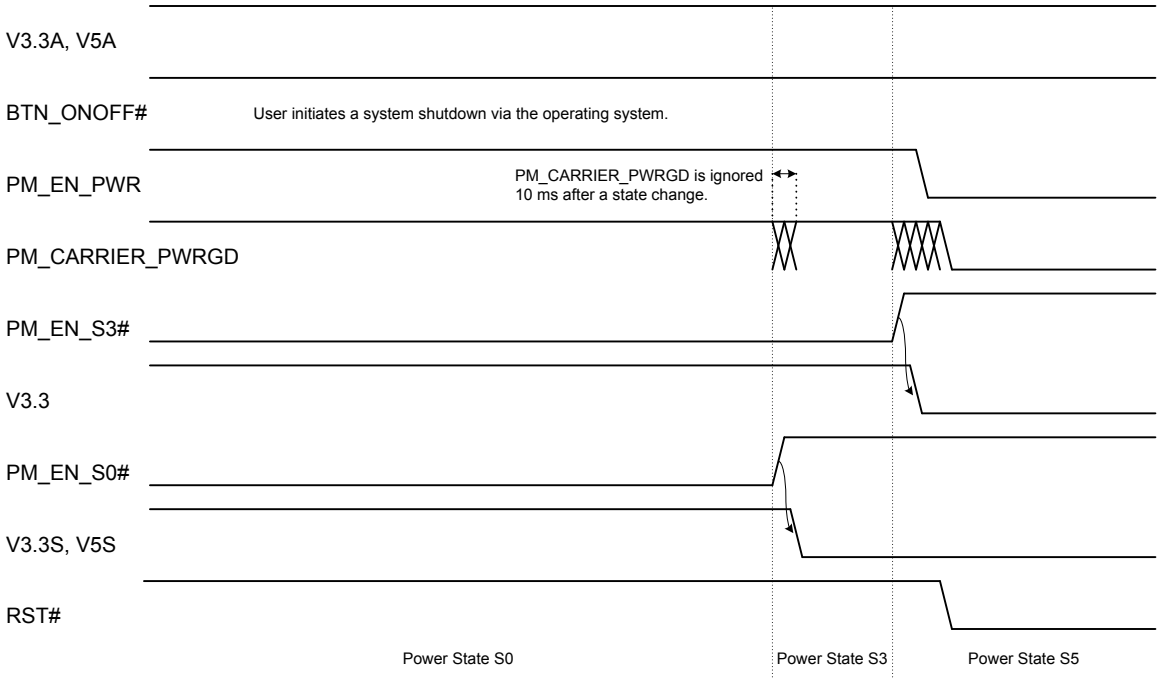


Figure 12. System shutdown initiated by operating system

Mechanical Specifications

This section describes mechanical and thermal design guidelines for the Catalyst TC.

Mechanical Design

Mechanical Drawing

The following mechanical drawing specifies the dimensions of the Catalyst TC, as well as locations of key components on the board. All dimensions are in inches.

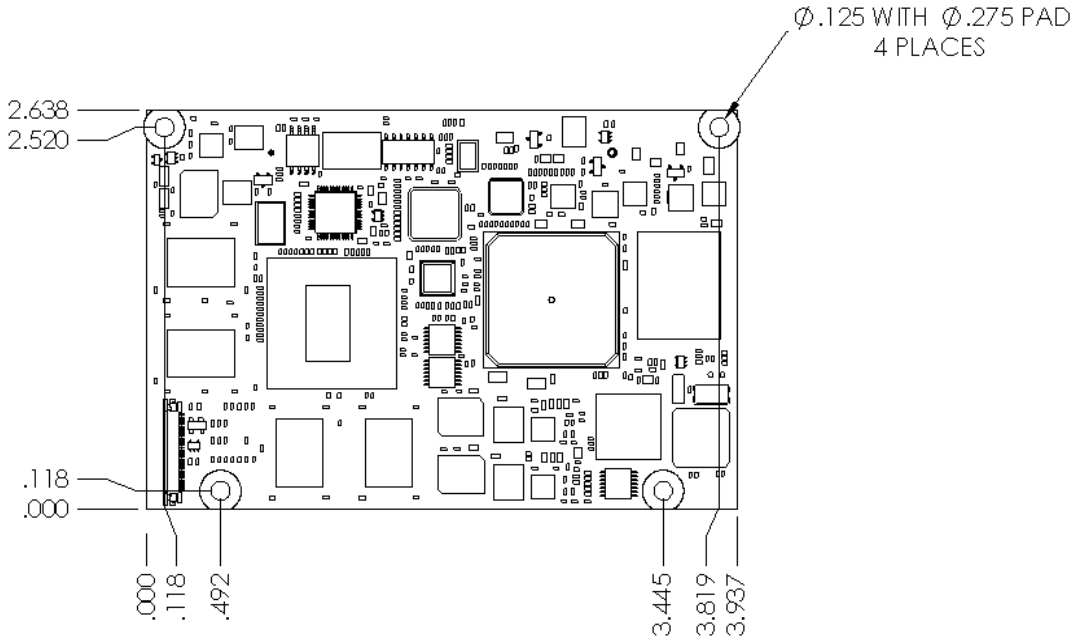


Figure 13. Catalyst TC, Top View

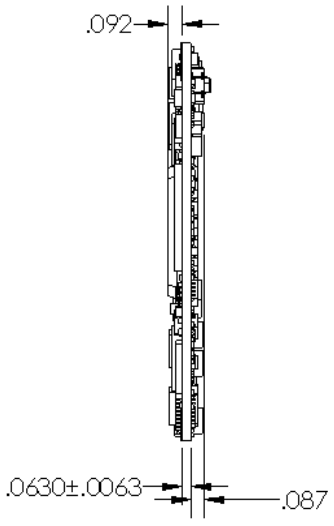


Figure 14. Catalyst TC, Side View

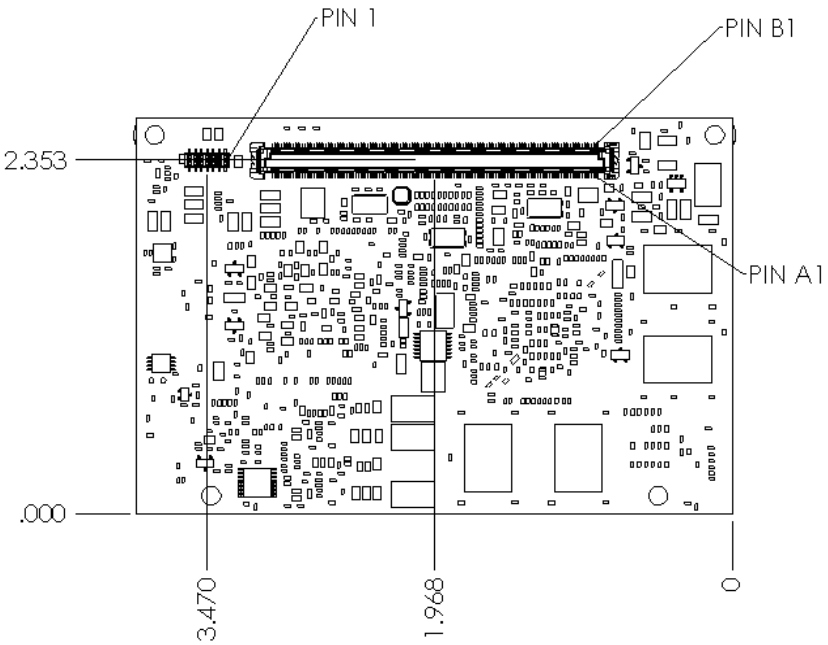


Figure 15. Catalyst TC, Bottom View

Notes:
For a 2D CAD drawing and 3D CAD model, check the Eurotech support site (http://support.eurotech-inc.com/) or contact your local Eurotech representative.

Total Stack Height

Selection of low profile stacking connectors and components minimizes the total stack height of the Catalyst TC and carrier board. The module uses stacking board-to-board connectors to mate with a carrier board. The mating connectors on the carrier board can be either 5 mm or 8 mm stacking height. When 5 mm stacking board-to-board connectors are used, the total board height combined with the connector clearance results in a total stack height of less than 10 mm. You may place components under the module on a custom carrier board. However, the design must allow adequate heat dissipation.

The following diagram illustrates the total stack height using 5 mm stacking connectors on the carrier board.

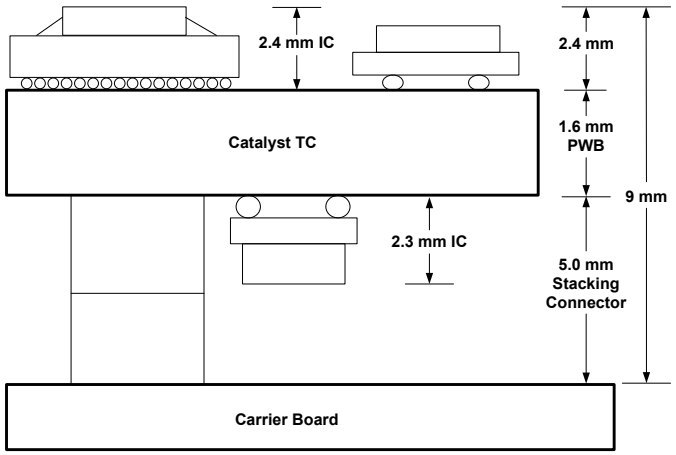


Figure 16. Total Stack Height

Mounting

Four holes enable mounting on the carrier board. Along one side, two mounting holes are located on each corner. The mounting holes are offset from the corners along the opposite side of the module. The Catalyst TC ground plane connects electrically to the mounting holes through 0Ω resistors.

Per IPC-A-610D section 4.2.3, secure the board to standoffs using a flat washer against the board with a split washer on top between the flat washer and the screw head or nut. Do not use toothed star washers, as they cut into the plating and laminations of the board over time and will not produce an attachment that will withstand vibration and thermal cycling.

Insertion and Removal

The Catalyst TC connects to the carrier board through two connectors that are in line with each other. A high-density, stacking board-to-board connector carries the data signals, while a smaller 2x7-pin 1 mm-pitch connector carries power. When fully connected, these fine pitch connectors provide reliable and durable connection. However, care is required when removing or installing the module onto the carrier board. If correct procedures for installation and removal are not followed, damage to the connectors and/or the connector pins can result.

For detailed procedures to install a module onto or remove a module from a carrier board, refer to the *Catalyst Module Installation and Removal Technical Support Bulletin (Eurotech document 110122-2014)*.

Warning:
Observe industry-standard electronic handling procedures when handling the module. The connectors expose signals on the system bus that do not have ESD protection.

Thermal Management

This section provides detailed data about the thermal interface for the Catalyst TC including thermal design power and mechanical load limit for the key components on the module.

The Thermal Design Power (TDP) is a representation of the expected peak power dissipation of each component or component group as viewed separately. The actual power consumption in real-world applications is not expected to reach this level for any given device and never in combination. However, the thermal management solution should accommodate proper control of temperature rise so as not to exceed the maximum thermal design interface temperatures as identified for key components.

The mechanical load limit specifies the maximum allowable load applied to the component during heat sink installation and removal, mechanical stress testing, or standard shipping conditions. Do not exceed this limit in your thermal management solution or use any portion of the component substrate as a mechanical reference or load bearing surface in either static or dynamic compressive load conditions.

The following table summarizes the thermal design interface for three key components on the Catalyst TC. The local ambient temperature of the module is defined by the temperatures at these three thermal design interface contact points.

Component (Interface temperature - +85°C max.)		Thermal Design Power – Max Point (W)	Mechanical Load Limit
Intel Atom processor (note 1)	600 MHz	2.7	14.88 lbf
	1.3 GHz	3.6	
	1.6 GHz	3.9	
Intel PCH EG20T (note 2)		1.55	
DDR-2 DRAM 8 devices (4 top, 4 bottom), Combined power		(To Be Determined)	

Notes:
1. TDP and mechanical load limit per the Intel Atom Processor E6xx Series Thermal and Mechanical Design Guidelines, February 2011, #324210-002. Mechanical load limit applied normal to the surface of a 22 x 22 mm, 676-ball micro-FCBGA package.
2. TDP per the Intel Platform Controller Hub EG20T Datasheet, February 2011, #324211-004US.

Table 17. Thermal Design Power and Mechanical Load Limit

The following diagrams illustrate the location of the three key thermal design interface contact points.

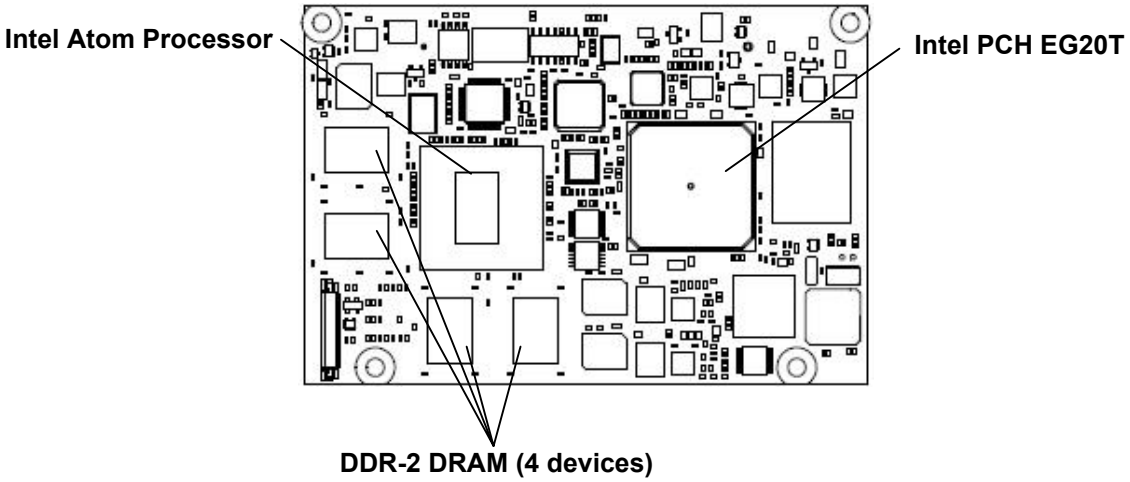


Figure 17. Thermal Interface, Top Side

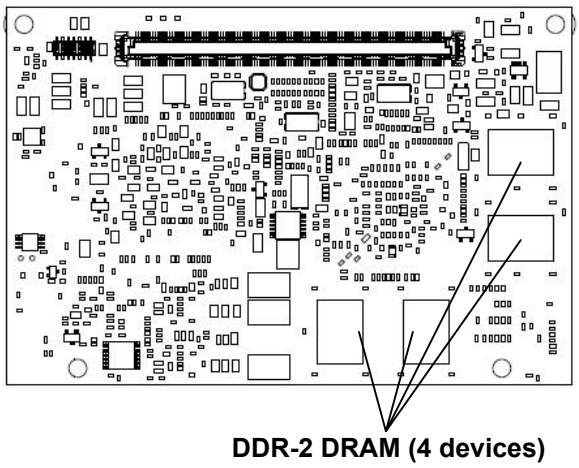


Figure 18. Thermal Interface, Bottom Side

Carrier Board Design

An application-specific carrier board integrates with the Catalyst TC to meet various system requirements. The Catalyst TC Development Kit includes a carrier board designed to maximize the Catalyst TC functionality. This carrier board implements many industry-standard interfaces and provides a reference for custom carrier boards optimized for your requirements. This section includes many of the considerations followed in the design of the Catalyst TC Development Kit carrier board.

Design Guidelines

Design Constraints

Increasing reliability is a key consideration in the Catalyst TC design. Several constraints followed in the module design and printed wiring board (PWB) layout ensure superior product reliability and compatibility. Use similar constraints in the carrier board design.

The following are the design considerations used to improve the Catalyst TC reliability:

- Advanced high-speed signal routing techniques
  - Strict adherence to signal routing rules as collaborated with Intel design and simulation teams
    - Minimum and maximum trace lengths
    - Total, segment, and multi-segment including package length compensation
    - Bus and group length matching to tight tolerances
    - Continuous trace matching for differential pair routing
  - Impedance matching and controlled design
    - Consideration of I/O buffer characteristic variances over extended temperature ranges for improved electrical performance
    - 100% continuous ground return path for all high-speed signals
    - Routing over continuous planes for consistent transmission line impedance and clean, reliable signal transitions
- Conservative printed wiring design construction
  - Durable feature sizes and construction elements
    - Pads, fills, and holes optimized for RoHS processing and long term reliability
  - Buried power planes between ground layers to eliminate coupling with high-speed signals
  - De-rating for current loading on the power regulation circuit and interface
  - No bottom side “hot” power regulation components underneath the Intel Atom processor or the Intel PCH EG20T that would reduce thermal performance

EMI/RFI Protection

Many products using Eurotech single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. The Catalyst TC incorporates the following design considerations that reduce emission and improve immunity:

- Four extra solid ground planes
- High-speed signal routing on internal ground referenced layers
- No high-speed signal return currents passed thru coupling capacitors
- Option for EMI ring on module perimeter

Routing Guidelines

Proper signal routing is critical to a successful carrier board design. The Catalyst TC supports high-speed differential and single-ended signals that require strict routing constraints. Use the following recommendations to route high-speed signals:

- Ground references
- Continuous reference planes
- Matched lengths
- Bend minimization
- Layer-to-layer connection reduction

The following are the high-speed differential pairs that require strict routing constraints on a carrier board:

- PCIe
  The PCIe x1 port consists of differential signal pairs for transmit, receive, and reference clock. The module includes AC coupling capacitors on the transmit pair. Include AC coupling capacitors on the receive pair driven from the carrier board to the Catalyst TC. The recommended coupling capacitor is a 0.1µF surface mount 0402 discrete capacitor of type X7R/X5R. Place the 0.1µF capacitors near the PCIe device on the carrier board.
- USB
  These signal pairs can be routed to USB sockets for external connections or directly to USB devices on the carrier board. Include an EMI choke between connector J1 and the USB connector when driving a USB cable. Applications with USB devices hardwired on-board do not require an EMI choke.
- LVDS display
  The LVDS display output includes four LVDS data pairs and a LVDS pixel clock.
- SDVO Interface
  The SDVO interface consists of seven high-speed differential signal pairs.
- SATA
  The SATA interface includes two high-speed differential pairs.
- Ethernet
  The Gigabit Ethernet signals include four high-speed differential pairs.

The following are the high-speed single-ended signals that require strict routing constraints on a carrier board:

- SD/MMC
- LPC bus
- HD Audio

For additional signal routing details, refer to the *Catalyst TC Carrier Board Routing Guidelines (Eurotech document 110125-5002)*.

Power Planes

The following voltages are inputs to the module on J2, page 47. These nets should be power planes on your carrier board:

- V3.3
- V3.3A
- V3.3S
- V5A
- V5S

Be sure to include sufficient bulk decoupling and local decoupling on each plane.

Requirements and Recommendations

The previous sections provided details about the various features of the Catalyst TC including design requirements and design recommendations. This section summarizes these design guidelines and provides a checklist for custom carrier board design.

Required Circuitry

The following table lists circuitry required on the carrier board.

Name	Pin	Carrier Board Design Requirement
Cat_TC_Detect	J1 B103	See Carrier Board Configuration, page 39.
FP_RESET#	J1 A59	Include momentary button.
BTN_ONOFF#	J1 B59	Include momentary button.
PCIE_RX_SLOT0_P **PCIE_RX_SLOT0_N**	J1 B95 J1 B94	Include 0.1µF AC coupling capacitors.
PCIE_RX_SLOT1_P **PCIE_RX_SLOT1_N**	J1 A95 J1 A94	Include 0.1µF AC coupling capacitors.
PCIE_RX_SLOT2_P **PCIE_RX_SLOT2_N**	J1 B18 J1 B19	Include 0.1µF AC coupling capacitors.
SDVO_CLK_P **SDVO_CLK_N**	J1 B91 J1 B92	Include 0.1µF AC coupling capacitors. Place near Catalyst TC connector J1.
CARRIER_I2C_SDA **CARRIER_I2C_SCL**	J1 B108 J1 B109	Include 10kΩ pull-ups to V3.3A.
V_BATTERY	J2 4	Include 3 V battery.
SMC_UART_RX **SMC_UART_TX**	J1 B57 J1 B106	Include access to these nets using test points or connector to aid in carrier board bring up. Include a 10kΩ pull-up to V3.3A to SMC_UART_RX.
L_DDC_CLK **L_DDC_DATA**	A29 B28	Include 2.2kΩ pull ups to V3.3S.

Table 18. Circuitry Required on the Carrier Board

Carrier Board Configuration

The Catalyst TC conforms to the same footprint as other Eurotech modules. However, the modules are not pin-compatible. Each module has a unique pinout on connector J1 providing different feature sets. When installed in a carrier board, the Catalyst TC reads the input signal Cat_TC_Detect (J1 B103) to determine the configuration of the carrier board. Your carrier board must include a 10kΩ pull-up resistor to V3.3A and a 10kΩ pull-down resistor on this input. If the Cat_TC_Detect input is connected incorrectly on the carrier board, the Catalyst TC will not boot.

Recommended Circuitry

The following table lists recommendations for circuitry on the carrier board.

Name	J1 Pin	Carrier Board Design Recommendation
JTAG_TDO	A106	Include 10kΩ pull-up to V3.3S.
CLK_LPC_FWH	A36	Include no more than one load.
CLK_LPC_SIO	B37	Connect to legacy IO controller if required.
SDVO_CTLCLK **SDVO_CTLDATA**	B30 A30	Include 3.3K Ω pull-ups to 2.5V.
LPC_AD3 **LPC_AD2** **LPC_AD1** **LPC_AD0**	B38 B34 B39 B36	Include 10kΩ pull-ups to V3.3S.
RST#	B56	Buffer for signal drive strength.
L_CTLA_CLK **L_CTLB_DATA**	B29 B25	Include 4.7kΩ pull ups to V3.3S.
USB0_P **USB0_N**	A71 A72	Include an EMI choke between connector J1 and the USB connector.
USB1_P **USB1_N**	B71 B72	Include an EMI choke between connector J1 and the USB connector.
USB2_P **USB2_N**	A68 A69	Include an EMI choke between connector J1 and the USB connector.
USB3_P **USB3_N**	B67 B68	Include an EMI choke between connector J1 and the USB connector.
USB4_P **USB4_N**	A65 A66	Include an EMI choke between connector J1 and the USB connector.

Name	J1 Pin	Carrier Board Design Recommendation
USB5_P **USB5_N**	B64 B65	Include an EMI choke between connector J1 and the USB connector.
USB6_P **USB6_N**	A62 A63	Include an EMI choke between connector J1 and the USB connector.
USB7_P **USB7_N**	B61 B62	Include an EMI choke between connector J1 and the USB connector.
USB8_P **USB8_N**	B74 B75	Include an EMI choke between connector J1 and the USB connector.
SATA1_TX_P **SATA1_TX_N**	A17 A18	Include 0.01μF AC coupling capacitors. Place near SATA connector.
SATA1_RX_P **SATA1_RX_N**	A19 A20	Include 0.01μF AC coupling capacitors. Place near SATA connector.
CAN_RX **CAN_TX**	A47 A48	Include a transceiver and filter between connector J1 and the CAN connector.

Table 19. Circuitry Recommended on the Carrier Board

Test and Debug

The maintenance serial port is extremely important in bring-up of a new carrier board design. Eurotech highly recommends including an external connection to SMC_UART_RX (J1 B57) and SMC_UART_TX (J1 B106) on your carrier board.

The IEEE1149.1 JTAG port, provided on connector J1, is available for programming the CPLD on the module, factory test, and software debugging. Otherwise, this port is not supported for application use. Eurotech highly recommends including an external connection to this JTAG port on your carrier board. To ensure correct operation of the JTAG interface, include a 10kΩ pull-up resistor to V3.3S on the TDO signal on the carrier board.

An additional ITP debug port, connector J3, provides full access to the XDP debugger port using a SFF style connector. Eurotech highly recommends allowing for access to this connector, in the event you are directed to use this port when working with Eurotech staff. Allow for the size of the mating connector and bend radius of the cable.

Connectors

Identifying Connectors

The following diagrams illustrate the location and numbering of the connectors on the Catalyst TC. When viewing the module from the component side, connector J1 and connector J2 lie under the module.

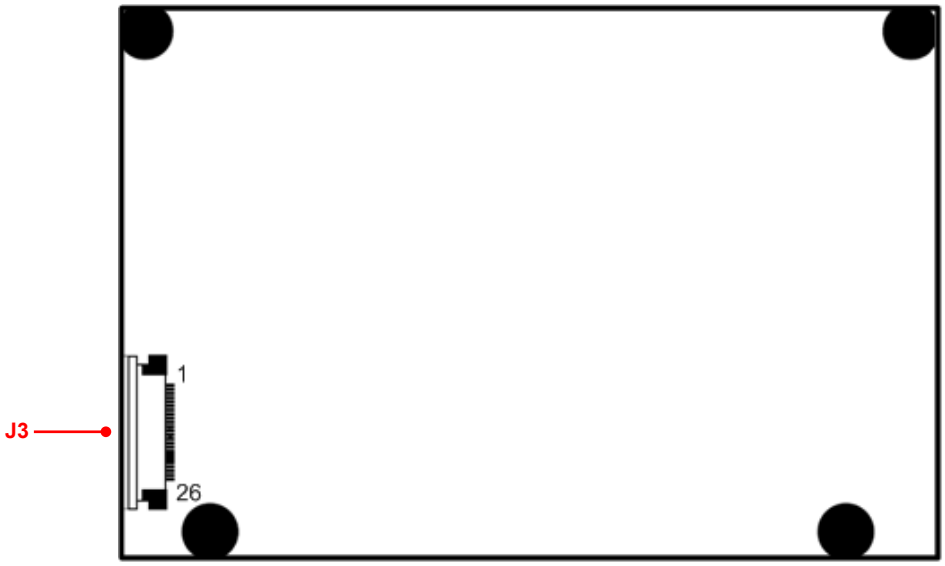


Figure 19. Connector Location, Top View

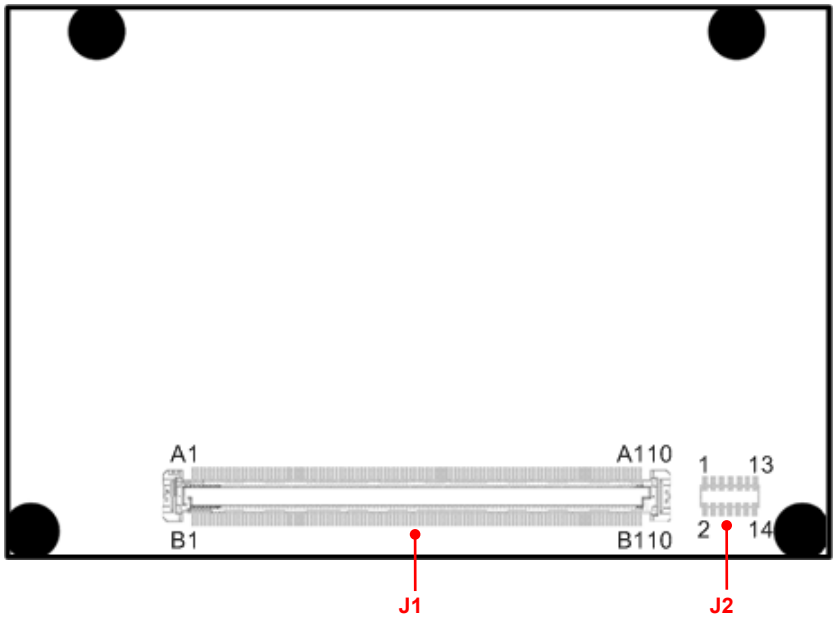


Figure 20. Connector Location, Bottom View

Signal Headers

The following tables describe the electrical signals available on the connectors of the module. Each section provides relevant details about the connector including part numbers, mating connectors, and connector pinout. The pinout table includes signal type, termination included on the module, the power state in which the signal is active, and a signal description.

J1: Docking Connector: Data

Board connector: 220-pin, stacking board-to-board receptacle, 0.5 mm, Tyco Electronics 3-6318490-6
Carrier board connector: Tyco Electronics 3-1827253-6, 5 mm stacking height
Tyco Electronics 3-6318491-6, 8 mm stacking height

The Catalyst TC connector J1 mates to the carrier board. Most data signals are provided on this docking connector.

Pin	Name	Type	On Module Termination	Power State	Description
A1	GND	P			Ground
A2	GPIO6	IO-LVTTL		S0,S3	Intel PCH EG20T GPIO1
A3	GPIO2	IO-CMOS		S0	Embedded controller GPIO
A4	HDA_SYNC	O-HDA		S0	Intel HD Audio frame sync
A5	HDA_RST#	O-HDA		S0	Intel HD Audio reset
A6	HDA_SDATAIN0	I-HDA		S0	Intel HD Audio serial data input 0
A7	HDA_SDATAIN1	I-HDA		S0	Intel HD Audio serial data input 1
A8	SLOT0_DATA4	IO-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 data 4
A9	SLOT0_DATA3	IO-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 data 3
A10	SLOT0_DATA1	IO-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 data 1
A11	GND	P			Ground
A12	SLOT0_LED	O-LVTTL		S0	SD/MMC 0 LED
A13	SLOT0_CLK	O-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 clock
A14	Reserved				
A15	SLOT0_DATA7	IO-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 data 7
A16	SLOT0_PWR#	O-3.3		S0	SD/MMC 0 power control
A17	SATA1_TX_P	O-SATA		S0	SATA1 transmit, positive signal
A18	SATA1_TX_N	O-SATA		S0	SATA1 transmit, negative signal
A19	SATA1_RX_P	I-SATA		S0	SATA1 receive, positive signal
A20	SATA1_RX_N	I-SATA		S0	SATA1 receive, negative signal
A21	GND	P			Ground
A22	MDI0_P	IO-A		S0,S3	Gigabit Ethernet, positive signal
A23	MDI0_N	IO-A		S0,S3	Gigabit Ethernet, negative signal
A24	LAN_LED0	O-3.3		S0,S3	Ethernet LED 0
A25	MDI2_P	IO-A		S0,S3	Gigabit Ethernet, positive signal
A26	MDI2_N	IO-A		S0,S3	Gigabit Ethernet, negative signal
A27	MDI3_P	IO-A		S0,S3	Gigabit Ethernet, positive signal
A28	MDI3_N	IO-A		S0,S3	Gigabit Ethernet, negative signal
A29	L_DDC_CLK	O-CMOS		S0, S3	LCD I^2C clock
A30	SDVO_CTLDATA	IO-CMOS/OD		S0	SDVO DDC I^2C data
A31	GND	P			Ground
A32	L_VDDEN	O-CMOS		S0	LCD power enable
A33	SMB_ALERT#	I-CMOS	PU 10kΩ V3.3S	S0	SMBus activity alert
A34	SPKR	O-CMOS		S0	Intel HD Audio speaker
A35	PM_CLKRUN#	IO-CMOS	PU 10kΩ V3.3S	S0	Initiates active clock output from LPC bus master
A36	CLK_LPC_FWH	O-CMOS	R22.6Ω	S0	LPC bus

Pin	Name	Type	On Module Termination	Power State	Description
A37	SPI_MISO	I-LVTTL	PD 10kΩ	S0	SPI data input
A38	SMB_CLK	O-CMOS/OD	PU 2.2kΩ V3.3S	S0	SMBus clock
A39	INT_SERIRQ	IO-CMOS	PU 10kΩ V3.3S	S0	LPC bus interrupt
A40	LPC_FRAME#	O-CMOS		S0	LPC bus frame sync
A41	GND	P			Ground
A42	SPI_MOSI	O-LVTTL		S0	SPI data output
A43	SPI_SCK	O-LVTTL	PD 10kΩ	S0	SPI clock signal
A44	SPI_SSN	IO-LVTTL	PD 10kΩ	S0	SPI chip select signal
A45	TC_I2C_SCL	O-OD	PU 10kΩ V3.3S	S0	I^2C clock
A46	TC_I2C_SDA	IO-OD	PU 10kΩ V3.3S	S0	I^2C data
A47	CAN_RX	I-LVTTL	PU 10kΩ V3.3S	S0	CAN Bus
A48	CAN_TX	O-LVTTL		S0	CAN Bus
A49	SP0_TX	O-LVTTL		S0,S3	Serial Port 0 Transmit Data
A50	SP0_RX	I-LVTTL	PU 10kΩ V3.3	S0,S3	Serial Port 0 Receive Data
A51	GND	P			Ground
A52	SP0_RTS	O-LVTTL		S0,S3	Serial Port 0 Request To Send
A53	SP0_RI	I-LVTTL	PU 10kΩ V3.3	S0,S3	Serial Port 0 Ring Indicator
A54	SP0_DTR	O-LVTTL		S0,S3	Serial Port 0 Data Terminal Ready
A55	SP0_DSR	I-LVTTL	PU 10kΩ V3.3	S0,S3	Serial Port 0 Data Set Ready
A56	SP0_DCD	I-LVTTL	PU 10kΩ V3.3	S0,S3	Serial Port 0 Carrier Detect
A57	HDA_DOCK_EN#	O-HDA		S0	Intel HD Audio enable
A58	HDA_DOCK_RST#	O-HDA		S0	Intel HD Audio reset
A59	FP_RESET#	I-3.3	PU 10kΩ V3.3S	S0	Front panel reset
A60	GND	P			Ground
A61	USB_OC5#	I-LVTTL	PU 10kΩ V3.3	S0,S3	USB5 over current
A62	USB6_P	IO		S0,S3	USB 6, positive signal
A63	USB6_N	IO		S0,S3	USB 6, negative signal
A64	GND	P			Ground
A65	USB4_P	IO		S0,S3	USB 4, positive signal
A66	USB4_N	IO		S0,S3	USB 4, negative signal
A67	GND	P			Ground
A68	USB2_P	IO		S0,S3	USB 2, positive signal
A69	USB2_N	IO		S0,S3	USB 2, negative signal
A70	GND	P			Ground
A71	USB0_P	IO		S0,S3	USB 0, positive signal
A72	USB0_N	IO		S0,S3	USB 0, negative signal
A73	GND	P			Ground
A74	LA_CLK_P	O-LVDS		S0	LVDS clock, positive signal
A75	LA_CLK_N	O-LVDS		S0	LVDS clock, negative signal
A76	GND	P			Ground
A77	LA_DATA2_P	O-LVDS		S0	LVDS data 2, positive signal
A78	LA_DATA2_N	O-LVDS		S0	LVDS data 2, negative signal
A79	USB_OC2#	I-3.3	PU 10kΩ V3.3_DELAY	S0,S3	USB 2 over current
A80	GND	P			Ground
A81	LA_DATA1_P	O-LVDS		S0	LVDS data 1, positive signal
A82	LA_DATA1_N	O-LVDS		S0	LVDS data 1, negative signal
A83	GND	P			Ground
A84	SDVO_STALL_P	I-SDVO		S0	SDVO stall signal, positive signal
A85	SDVO_STALL_N	I-SDVO		S0	SDVO stall signal, negative signal
A86	GND	P			Ground

Pin	Name	Type	On Module Termination	Power State	Description
A87	SDVO_BLUE_P	O-SDVO	C 0.1µF	S0	SDVO blue data, positive signal
A88	SDVO_BLUE_N	O-SDVO	C 0.1µF	S0	SDVO blue data, negative signal
A89	USB_OC3#	I-LVTTL	PU 10kΩ V3.3	S0,S3	USB 3 over current
A90	GND	P			Ground
A91	SDVO_INT_P	I-SDVO		S0	SDVO interrupt, positive signal
A92	SDVO_INT_N	I-SDVO		S0	SDVO interrupt, negative signal
A93	GND	P			Ground
A94	PCIE_RX_SLOT1_N	I-PCIe		S0	PCIe 1 Receive, negative signal
A95	PCIE_RX_SLOT1_P	I-PCIe		S0	PCIe 1 Receive, positive signal
A96	GND	P			Ground
A97	CLK_SLOT0_OE#	I-3.3	PU 10kΩ V3.3S	S0	PCIe 0 clock enable
A98	PCIE_TX_SLOT0_N	O-PCIe	C 0.1µF	S0	PCIe 0 Transmit, negative signal
A99	PCIE_TX_SLOT0_P	O-PCIe	C 0.1µF	S0	PCIe 0 Transmit, positive signal
A100	GND	P			Ground
A101	CLK_PCIE_SLOT0_P	O	R 33Ω	S0	PCIe 0 Clock, positive signal
A102	CLK_PCIE_SLOT0_N	O	R 33Ω	S0	PCIe 0 Clock, negative signal
A103	GND	P			Ground
A104	JTAG_TMS	O	PU 10kΩ V3.3S	S0	JTAG
A105	JTAG_TCK	I	PD 1kΩ	S0	JTAG
A106	JTAG_TDO	O		S0	JTAG
A107	JTAG_TDI	I	PU 10kΩ V3.3S	S0	JTAG
A108	GPIO1	IO-CMOS		S0	Embedded controller GPIO
A109	Reserved				
A110	GND	P			Ground
B1	GND	P			Ground
B2	LPCPD#	O-3.3	PU 10kΩ V3.3S	S0	(For details, contact Eurotech)
B3	H_INIT#	I-LVCMOS	PU 1kΩ 1.05V	S0	Soft reset for host processor
B4	HDA_BITCLK	O-HDA		S0	Intel HD Audio bit clock
B5	HDA_SDATAOUT	O-HDA		S0	Intel HD Audio data out
B6	SLOT0_CMD	IO-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 command
B7	SLOT0_DATA0	IO-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 data 0
B8	SLOT0_DATA6	IO-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 data 6
B9	SLOT0_DATA5	IO-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 data 5
B10	SLOT0_DATA2	IO-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 data 2
B11	GND	P			Ground
B12	SLOT0_WP	I-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 write protect
B13	SLOT0_CD#	I-LVTTL	PU 10kΩ V3.3S	S0	SD/MMC 0 card detection
B14	Reserved				
B15	Reserved				
B16	PCIE_TX_SLOT2_P	O-PCIe	C 0.1µF	S0	PCIE 2 transmit, positive signal
B17	PCIE_TX_SLOT2_N	O-PCIe	C 0.1µF	S0	PCIE 2 transmit, negative signal
B18	PCIE_RX_SLOT2_P	I-PCIe		S0	PCIE 2 receive, positive signal
B19	PCIE_RX_SLOT2_N	I-PCIe		S0	PCIE 2 receive, negative signal
B20	Reserved				
B21	GND	P			Ground
B22	MDI1_P	IO-A		S0, S3	Gigabit Ethernet, positive signal
B23	MDI1_N	IO-A		S0, S3	Gigabit Ethernet, negative signal
B24	LAN_LED2	O-3.3		S0, S3	Ethernet LED 2
B25	L_CTLB_DATA	IO-LVTTL		S0	Backlight I^2C data
B26	Reserved				

Pin	Name	Type	On Module Termination	Power State	Description
B27	LAN_LED1	O-3.3		S0, S3	Ethernet LED 1
B28	L_DDC_DATA	IO-CMOS		S0, S3	LCD DDC I^2C data
B29	L_CTLA_CLK	O-LVTTL		S0	Backlight I^2C clock
B30	SDVO_CTLCLK	O-CMOS/OD		S0	SDVO DDC I^2C clock
B31	GND	P			Ground
B32	L_BKLTEN	O-CMOS		S0	Turns power to the backlight on/off
B33	L_BKLTCTL	O-CMOS		S0, S3	Controls intensity of the backlight
B34	LPC_AD2	IO-CMOS	PU 10kΩ V3.3S	S0	LPC Bus address/data 2
B35	SMB_DATA	IO-CMOS/OD	PU 2.2kΩ V3.3S	S0	SMBus data
B36	LPC_AD0	IO-CMOS	PU 10kΩ V3.3S	S0	LPC Bus address/data 0
B37	CLK_LPC_SIO	O-CMOS	R 22.6Ω	S0	LPC Bus clock
B38	LPC_AD3	IO-CMOS	PU 10kΩ V3.3S	S0	LPC Bus address/data 3
B39	LPC_AD1	IO-CMOS	PU 10kΩ V3.3S	S0	LPC Bus address/data 1
B40	GPIO3	IO-LVTTL		S0, S3	Intel PCH EG20T GPIO2
B41	GND	P			Ground
B42	SP0_CTS	I-LVTTL	PU 10kΩ V3.3	S0, S3	Serial Port 0 Clear To Send
B43	SP1_TX	O-LVTTL		S0, S3	Serial Port 1 Transmit Data
B44	SP1_RX	I-LVTTL	PU 10kΩ V3.3	S0, S3	Serial Port 1 Receive Data
B45	SP2_TX	O-LVTTL		S0, S3	Serial Port 2 Transmit Data
B46	SP2_RX	I-LVTTL	PU 10kΩ V3.3	S0, S3	Serial Port 2 Receive Data
B47	SP3_TX	O-LVTTL		S0, S3	Serial Port 3 Transmit Data
B48	SP3_RX	I-LVTTL	PU 10kΩ V3.3	S0, S3	Serial Port 3 Receive Data
B49	USB8_P	IO		S0, S3	USB 8, positive signal
B50	USB8_N	IO		S0, S3	USB 8, negative signal
B51	GND	P			Ground
B52	GPIO4	IO-LVTTL		S0, S3	Intel PCH EG20T GPIO3
B53	USB_CLIENT	I-3.3	PU 100kΩ V3.3_DELAY	S0, S3	USB2 client detection
B54	GPIO5	IO-LVTTL		S0, S3	Intel PCH EG20T GPIO4
B55	PCIE_WAKE#	I-CMOS	PU 1kΩ 3.3V	S0, S3	Standard I/O device wake event
B56	RST#	O-3.3		S0, S3	System reset
B57	SMC_UART_RX	I-3.3		S0, S3, S5	Maintenance port Receive
B58	L_BKLTSEL0_GPIO#	O-LVTTL		S0, S3	Selects backlight control (PWM vs. I^2C)
B59	BTN_ONOFF#	I-5	PU 10kΩ V5A	S0, S3, S5	Power button input
B60	GND	P			Ground
B61	USB7_P	IO		S0, S3	USB 7, positive signal
B62	USB7_N	IO		S0, S3	USB 7, negative signal
B63	GND	P			Ground
B64	USB5_P	IO		S0, S3	USB 5, positive signal
B65	USB5_N	IO		S0, S3	USB 5, negative signal
B66	GND	P			Ground
B67	USB3_P	IO		S0, S3	USB 3, positive signal
B68	USB3_N	IO		S0, S3	USB 3, negative signal
B69	USB_OC0#	I-LVTTL	PU 10kΩ V3.3	S0, S3	USB 0 over current
B70	GND	P			Ground
B71	USB1_P	IO		S0, S3	USB 1, positive signal
B72	USB1_N	IO		S0, S3	USB 1, negative signal
B73	GND	P			Ground
B74	LA_DATA3_P	O-LVDS		S0	LVDS data 3, positive signal
B75	LA_DATA3_N	O-LVDS		S0	LVDS data 3, negative signal
B76	GND	P			Ground

Pin	Name	Type	On Module Termination	Power State	Description
B77	LA_DATA0_P	O-LVDS		S0	LVDS data 0, positive signal
B78	LA_DATA0_N	O-LVDS		S0	LVDS data 0, negative signal
B79	USB_OC4#	I-LVTTL	PU 10kΩ V3.3	S0, S3	USB 4 over current
B80	GND	P			Ground
B81	SDVO_RED_P	O-SDVO	C 0.1µF	S0	SDVO red data, positive signal
B82	SDVO_RED_N	O-SDVO	C 0.1µF	S0	SDVO red data, negative signal
B83	GND	P			Ground
B84	SDVO_TVCLKIN_P	I-SDVO	C 0.1µF	S0	SDVO ext. frequency reference
B85	SDVO_TVCLKIN_N	I-SDVO	C 0.1µF	S0	SDVO ext. frequency reference
B86	GND	P			Ground
B87	SDVO_GREEN_P	O-SDVO	C 0.1µF	S0	SDVO green data, positive signal
B88	SDVO_GREEN_N	O-SDVO	C 0.1µF	S0	SDVO green data, negative signal
B89	USB_OC1#	I-LVTTL	PU 10kΩ V3.3	S0, S3	USB 1 over current
B90	GND	P			Ground
B91	SDVO_CLK_P	O-SDVO		S0	SDVO clock, positive signal
B92	SDVO_CLK_N	O-SDVO		S0	SDVO clock, negative signal
B93	GND	P			Ground
B94	PCIE_RX_SLOT0_N	I-PCIe		S0	PCIe 0 receive, negative signal
B95	PCIE_RX_SLOT0_P	I-PCIe		S0	PCIe 0 receive, positive signal
B96	GND	P			Ground
B97	CLK_SLOT1_OE#	I-3.3	PU 10kΩ V3.3S	S0	PCIe 1 clock enable
B98	PCIE_TX_SLOT1_N	O-PCIe	C 0.1µF	S0	PCIe 1 transmit, negative signal
B99	PCIE_TX_SLOT1_P	O-PCIe	C 0.1µF	S0	PCIe 1 transmit, positive signal
B100	GND	P			Ground
B101	CLK_PCIE_SLOT1_P	O	R 33Ω	S0	PCIe 1 clock, positive signal
B102	CLK_PCIE_SLOT1_N	O	R 33Ω	S0	PCIe 1 clock, negative signal
B103	Cat_TC Detect	I-3.3		S0, S3, S5	Indicates Catalyst TC mode (See Carrier Board Configuration)
B104	PM_EN_S0#	O-3.3	PU 10kΩ V3.3A	S0, S3, S5	Power state indicator
B105	PM_EN_PWR	O-3.3		S0, S3, S5	Power state indicator
B106	SMC_UART_TX	O-3.3		S0, S3, S5	Maintenance port Transmit
B107	PM_EN_S3#	O-3.3	PU 10kΩ V3.3A	S0, S3, S5	Power state indicator
B108	CARRIER_I2C_SDA	IO-OD		S0, S3, S5	I^2C bus data
B109	CARRIER_I2C_SCL	O-OD		S0, S3, S5	I^2C bus clock
B110	GND	P			Ground

J2: Docking Connector: Power

Board connector: 2x7 socket, 1 mm, Samtec CLM-107-02-LM-D
Carrier board connector: Samtec MW-07-03-G-D-095-085, 5 mm stacking height
Samtec MW-07-03-G-D-226-065, 8 mm stacking height

The Catalyst TC receives the power input and controls for interfacing with an external power supply on this docking connector. For a description of the Catalyst TC power supply, see Power Requirements, page 24.

Pin	Name	Type	Power State	Description
1	V3.3	PI	S0, S3	3.3 V primary supply voltage
2	PM_CARRIER_PWRGD	I-3.3	S0, S3, S5	Indicator for input power voltages
3	V3.3	PI	S0, S3	3.3 V primary supply voltage
4	V_BATTERY	PI		RTC backup power
5	V3.3	PI	S0, S3	3.3 V primary supply voltage
6	V5A	PI	S0, S3, S5	5 V “always” power
7	V5S	PI	S0	5 V normal operating power
8	V3.3A	PI	S0, S3, S5	3.3 V “always” power
9	V5S	PI	S0	5 V normal operating power
10	GND	P		Ground
11	V3.3S	PI	S0	3.3 V normal operating power
12	GND	P		Ground
13	V3.3S	PI	S0	3.3 V normal operating power
14	GND	P		Ground

Warning:
Disconnect the power input before removing the Catalyst TC. Removing the module from a powered carrier board may result in damage to both the carrier board and to the module.

J3: ITP Debug Port

Board connector: 26-pin FFC/FPC connector, 0.5 mm, Molex 52435-2472

Connector J3 provides an In-Target Probe (ITP) debug port for the Catalyst TC. For additional details, see Test and Debug, page 40.

System Specifications

Power Supply

The Catalyst TC requires the power inputs and control signals listed in the following table. For a description of the power supply, see Power Supply Architecture, page 25.

Symbol	Parameter	Min	Typ.	Max	Units
System Power Inputs (note 3)					
V3.3	Primary supply voltage	3.135	3.3	3.465	V
$I_{V3.3}$	Input current in S0 (note 4)			1.5	A
V3.3A	"Always" power (note 5)	3.135	3.3	3.465	V
$I_{V3.3A}$	Pre-production only Input current in S0 (note 4)			1.5	A
	Production Input current in S0 (note 4)			0.125	A
V3.3S	Normal operating power	3.135	3.3	3.465	V
$I_{V3.3S}$				0.45	A
V5A	"Always" power	4.75	5.0	5.25	V
I_{V5A}				0.025	A
V5S	Normal operating power	4.75	5.0	5.25	V
I_{V5S}				0.60	A
V_BATTERY	RTC backup power (note 6)		3.3		V
$I_{V\_BATTERY}$	(note 7)			300	µA
				40	µA
PM_CARRIER_PWRGD					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
R_{PU}	Pull-up resistance (note 8)		10		kΩ
V_{PU}				3.3	V
PM_EN_PWR					
V_{OH}	High-level output voltage I_{OH} = -16 mA, V_{CC} = 3 V	2.4	3.3		V
V_{OL}	Low-level output voltage I_{OL} = 16 mA, V_{CC} = 3 V			0.4	V
PM_EN_S0#, PM_EN_S3# (note 9)					
V_{OH}	High-level output voltage I_{OH} = -4 mA, V_{DD}=3.3 V	V_{DD}-0.4	3.3		V
V_{OL}	Low-level output voltage I_{OL} = 4 mA, V_{DD}=3.3 V			0.4	V
BTN_ONOFF#					
V_{IH}	High-level input voltage	2.5	5		V
V_{IL}	Low-level input voltage			1.0	V
R_{PU}	Pull-up resistance (note 10)		10		kΩ
V_{PU}				5	V

Notes:

3. The maximum currents per voltage rail include peak currents and are not indicative of aggregate power consumption during normal system operation.
4. On modules built prior to revision 621125-5000RA3, V3.3A and V3.3 are diode OR'ed to power an on-module regulator. The maximum current specified is 1.5 A for both V3.3 and V3.3A. However, this value is the maximum current for the sum of the two supplies, which is the current required for the on-module regulator. The voltage on V3.3A and V3.3 will determine how this current requirement is shared between the V3.3 and V3.3A.
   On modules built for revision 621125-5000RA3 and above, V3.3A and V3.3 are not diode OR'ed. The maximum current specified is 1.5 A for V3.3 and 0.125 A for V3.3A.
5. If V3.3A goes below 3.08V, the embedded controller will reset and a reset header will be displayed on the maintenance port. The reset of embedded controller results in a complete restart of module circuitry including all on-module power regulation, resets, and interface power sequence signals.
6. V_BATTERY has 1 µF of bulk decoupling capacitance, load side of diode.
7. On modules built prior to revision 621125-5000RB, the RTC circuit required 300uA.
   On modules built for revision 621125-5000RB and above, the RTC requires 40uA.
8. PM_CARRIER_PWRGD includes a pull-up resistor to V3.3A.
   For detailed timing requirements, see Power State Signals, page 27.
9. Specifications per the NXP LPC2132 Product Datasheet, Rev. 04 – 16 October 2007, www.nxp.com.
10. BTN_ONOFF# includes a pull-up resistor to V5A.

Performance

The Catalyst TC meets the performance specifications listed in the following table. For additional details about the processor, see Core Processor, page 15.

Parameter	Min	Typ.	Max	Units
Processor operating frequency (note 11)	0.6	1.3	1.6	GHz
System bus clock			400	MHz

Notes:

11. For availability of the 600 MHz and 1.6 GHz module, contact your local Eurotech representative.

Electrical

This section provides electrical specifications for the Catalyst TC. For additional details about termination of individual signals, see the signal connectors in Signal Headers, page 42.

PCIe Clock Buffer

An on-module PCIe clock buffer provides a PCIe clock for PCIe slot 0 and PCIe slot 1. Two additional input signals, CLK_SLOTx_OE#, individually control each reference clock. For a description of the PCIe slots, see PCI Express Bus, page 17.

Symbol	Parameter	Min	Typ.	Max	Units
CLK_PCIE_SLOT0, CLK_PCIE_SLOT1 (note 12)					
F_{PCIEx_REFCLK}	Frequency		100		MHz
V_{HIGH}	Maximum output voltage			1150	mV
V_{LOW}	Minimum output voltage	-300			mV
CLK_SLOT0_OE#, CLK_SLOT1_OE#					
V_{IH}	High-level input voltage	2	3.3		V
V_{IL}	Low-level input voltage			0.8	V
R_{PU}	Pull-up resistance (note 13)		10		kΩ
V_{PU}				3.3	V

Notes:

12. The CLK_PCIE_SLOT0 and CLK_PCIE_SLOT1 signal pairs are low power differential outputs. Specifications per the IDT ICS9DBL411A Datasheet, 02/21/08 (#1250B), www.idt.com.
13. CLK_SLOT0_OE# and CLK_SLOT1_OE# include pull-up resistors to V3.3S.

Universal Serial Bus

The Catalyst TC provides nine Universal Serial Bus (USB) ports. For a description of these ports, see Universal Serial Bus, page 18.

Symbol	Parameter	Min	Typ.	Max	Units
USB_OCx#					
R_{PU}	Pull-up resistance (note 14)		10		kΩ
V_{PU}				3.3	V
USB_CLIENT (note 15)					
V_{IH}	High-level input voltage	1.35			V
V_{IL}	Low-level input voltage			0.8	V

Notes:

14. USB_OC0#, USB_OC1#, USB_OC3#, USB_OC4#, and USB_OC5# include pull-up resistors to V3.3. USB_OC2# includes a pull-up resistor to V3.3_DELAY.
15. Specifications per the ADG772 Datasheet, Rev A, 6/08, www.analog.com.

I²C Bus

The Catalyst TC provides external connections to two I²C buses with the Catalyst TC acting as the bus master for each bus. The Carrier I²C bus connects to the Catalyst TC embedded controller, while the TC I²C bus connects to the Intel PCH EG20T. For a description of these buses, see I²C Bus, page 19.

Symbol	Parameter	Min	Typ.	Max	Units
CARRIER_I2C_SDA, CARRIER_I2C_SCL (note 16)					
F_{SMB_CLK}	Bus clock	100		400	kHz
TC_I2C_SDA, TC_I2C_SCL					
F_{SMB_CLK}	Bus clock	100		400	kHz
R_{PU}	Pull-up resistance (note 17)		10		kΩ
V_{PU}				3.3	V

Notes:

16. CARRIER_I2C_SDA and CARRIER_I2C_SCL do not include termination on the module. Include 10kΩ pull-up resistors to V3.3A on the carrier board.
17. TC_I2C_SDA and TC_I2C_SCL include pull-up resistors to V3.3S.

SMBus

The Catalyst TC includes an external connection to the SMBus on connector J1. For a description of this bus, see System Management Bus, page 20.

Symbol	Parameter	Min	Typ.	Max	Units
SMB_CLK, SMB_DATA					
F_{SMB_CLK}	Bus clock	1		1000	kHz
R_{PU}	Pull-up resistance (note 18)		2.2		kΩ
V_{PU}				3.3	V
SMB_ALERT#					
R_{PU}	Pull-up resistance (note 18)		10		kΩ
V_{PU}				3.3	V

Note:

18. SMB_CLK, SMB_DATA, and SMB_ALERT# include pull-up resistors to V3.3S.

LVDS Display and Backlight

The Catalyst TC provides discrete signals and two serial buses to control an LCD and backlight. For a description of these signals, see LVDS Display, page 21 and Backlight, page 22.

Symbol	Parameter	Min	Typ.	Max	Units
L_VDDEN, L_BKLTEN, L_BKLTCTL (note 19)					
V_{OH}	High-level output voltage	2.4			V
V_{OL}	Low-level output voltage			0.4	V
L_BKLTSEL0_GPIO# (note 20)					
V_{OH}	High-level output voltage I_{OH} = -8 mA, V_{CC} = 3.3 V	V_{CC}-0.5			V
V_{OL}	Low-level output voltage I_{OL} = 8 mA, V_{CC} = 3.3 V	0		0.4	V
L_DDC_CLK, L_DDC_DATA, L_CTLB_DATA, L_CTLA_CLK (note 21)					
F_{CLK}	Bus clock			100	kHz

Notes:

19. Specifications per the Intel Atom Processor E6xx Series Datasheet, October 2010 (#324208-002US).
20. Specifications per the Intel Platform Controller Hub EG20T, October 2010 (#324211-002US).
21. L_DDC_CLK and L_DDC_DATA do not include termination on the module. Include 2.2kΩ pull-up resistors to V3.3S on the carrier board.
    L_CTLB_DATA and L_CTLA_CLK do not include termination on the module. Include 4.7kΩ pull-up resistors to V3.3S on the carrier board.

Reset Signals

The Catalyst TC includes three reset signals. For details, see Reset Signals, page 23.

Symbol	Parameter	Min	Typ.	Max	Units
RST#					
V_{OH}	High-level output voltage I_{OH} = -16 mA, V_{CC} = 3 V	2.4	3.3		V
V_{OL}	Low-level output voltage I_{OL} = 16 mA, V_{CC} = 3 V			0.4	V
FP_RESET# (note 22)					
V_{IH}	High-level input voltage	2.0	3.3		V
V_{IL}	Low-level input voltage			0.8	V
R_{PU}	Pull-up resistance		10		kΩ
V_{PU}				3.3	V
H_INIT#					
V_{IH}	High-level input voltage V_{REF} = 1.05 V	1.55			V
V_{IL}	Low-level input voltage V_{REF} = 1.05 V			0.55	V

Note:
22. The module includes debounce circuitry and a pull-up resistor to V3.3S. FP_RESET# will not be detected until after RST# is de-asserted.

General-purpose Inputs and Outputs

The Catalyst TC includes six GPIOs. The embedded controller provides two GPIOs; while the Intel PCH EG20T provides the remaining four GPIOs. For a description of these signals, see General-Purpose Input and Output, page 23.

Symbol	Parameter	Min	Typ.	Max	Units
GPIO1, GPIO2 (note 23)					
V_{IH}	High-level input voltage	1.7	3.3		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage I_{OH} = -0.1 mA, V_{CC} = 3.3 V	V_{CC}-0.2			V
V_{OL}	Low-level output voltage I_{OL} = 0.1 mA, V_{CC} = 3.3 V			0.2	V
GPIO3, GPIO4, GPIO5, GPIO6 (note 24)					
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage I_{OH} = -8 mA, V_{CC} = 3.3 V	V_{CC}-0.5			V
V_{OL}	Low-level output voltage I_{OL} = 8 mA, V_{CC} = 3.3 V			0.4	V

Note:
23. Specifications per the Altera MAX II Device Handbook, August 2009 (MII5V1-3.3), www.altera.com.
24. Specifications per the Intel Platform Controller Hub EG20T, October 2010 (#324211-002US).

Intel High Definition Audio

The Intel Atom processor supports the Intel HD Audio specification. For a description of the audio interface, see Intel High Definition Audio, page 24.

Symbol	Parameter	Min	Typ.	Max	Units
HDA (note 25)					
V_{CC}	Supply voltage		3.3		V
V_{IH}	High-level input voltage	0.65*V_{CC}			V
V_{IL}	Low-level input voltage			0.35*V_{CC}	V
V_{OH}	High-level output voltage I_{OH} = -500 µA	0.9*V_{CC}			V
V_{OL}	Low-level output voltage I_{OL} = 1500 µA			0.10*V_{CC}	V
F_{HDA_SDIx}	Data rate		24		Mbps

Note:
25. Specifications per the Intel High Definition Audio Specification Revision 1.0.

General

This section provides general specifications for the Catalyst TC.

Crystal Frequencies

Agencies certifying the Catalyst TC for compliance for radio-frequency emissions typically need to know the frequencies of on-board oscillators. The following table lists the frequencies of all crystals on the Catalyst TC.

Crystals	Device	Typ.	Units
X3	Embedded Controller	14.7456	MHz
X5	Clock Generator	25.000	MHz
X6	USB Hub	24.000	MHz
X7	Reserved	25.000	MHz
X1	RTC	32.768	kHz
X10	Ethernet Controller	25.000	MHz
OS2	USB	48.0	MHz
OS3	Serial Port	1.8432	MHz

In addition, the Catalyst TC generates the following on-board clocks: 14.318 MHz, 33 MHz, 75 MHz, 96 MHz, and 100 MHz.

Real-Time Clock

The Intel Atom processor includes a RTC function that retains the system date and time. For a description of this function, see Real-Time Clock, page 16.

Parameter	Typ.	Units
Accuracy per month @ 25°C	+/-55	sec

Environmental

The Catalyst TC is designed to meet the environmental specifications listed in the following table. Note the local ambient temperature of the module is defined by the temperatures at three key thermal design interface contact points. Temperatures at these points must not exceed the maximum temperature specified. For additional information about the thermal interface of the Catalyst TC, see Thermal Management, page 35.

Parameter	Min	Typ.	Max	Units
Commercial operating temperature	0		+70	°C
Industrial operating temperature (note 26)	-40		+85	°C
Storage temperature	-40		+85	°C
Relative humidity, non-condensing	5		95	%

Note:
26. For availability of industrial temperature range modules, contact your local Eurotech representative.

Appendix A – Reference Information

Product Information

Product notices, updated drivers, support material:
www.eurotech.com

Intel

Information about the Intel products, High Definition Audio specification, and LPC bus specification:
www.intel.com

Trusted Computing Group

Trusted Computer Group specification:
www.trustedcomputinggroup.org

PCI SIG

PCI Express specification:
www.pcisig.com

USB

Universal Serial Bus specification:
www.usb.org

I²C Bus

I²C bus specification:
www.nxp.com

SMBus

SMBus specification:
www.smbus.org

SDIO Card

SD Card Association and SDIO specification:
www.sdcard.org

MMC Card

MultiMediaCard specification:
www.jedec.org

SATA

Serial ATA specification:
www.sata-io.org

CAN

CAN specification:
www.semiconductors.bosch.de

ACPI Specification

ACPI specification:
www.acpi.info/spec.htm

Appendix B – Board Revision

This guide applies to the current revision of the module as given in the following section.

Identifying the Board Revision

The revision number of the printed wiring board is printed on the board. That number is 170125-500Rx. The “x” indicates the revision level of the PWB.

The board also includes a label providing additional revision information. The number beginning with 621 indicates the revision level of the PWB with a corresponding bill of materials; while the number beginning with 900 indicates the configuration.

Board Revision History

The following is an overview of the revisions to the Catalyst TC.

Revision A

Initial release

Revision 621125-5000RA3 and above

V3.3A and V3.3 are not diode OR’ed.

Revision 621125-5000RB and above

RTC current draw is reduced.

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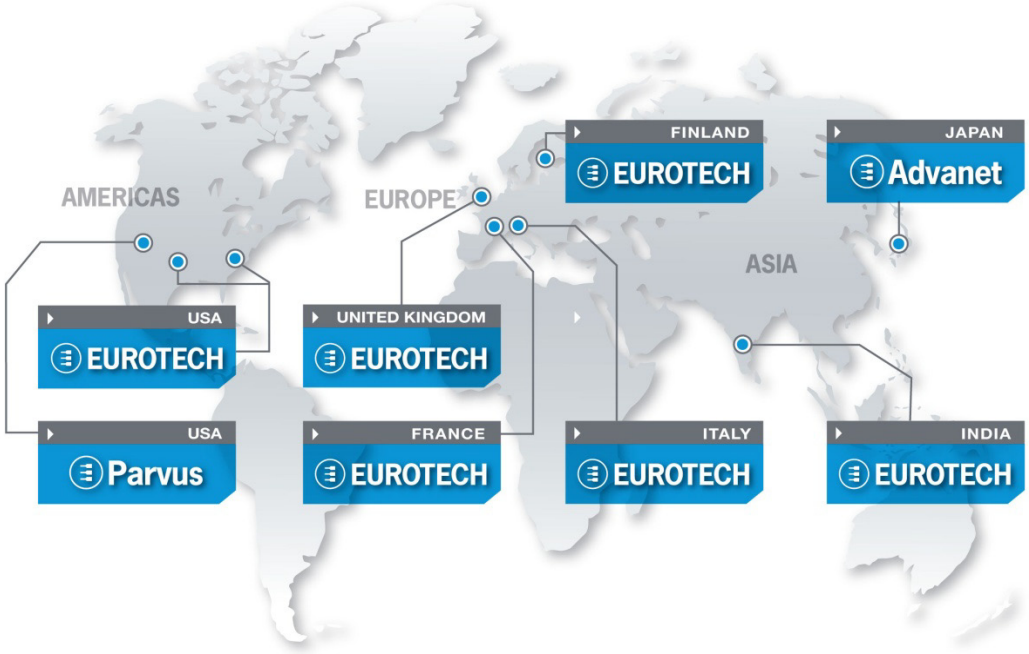

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