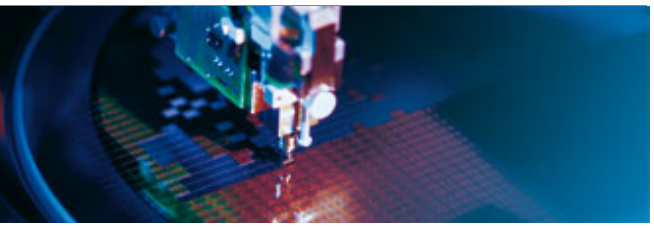
DESIGN-IN GUIDE



# CPU-301-16

**Single Board Computer/Computer on Module**

Rev 1 – August 2013 – 110127-40001

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# Document Revision History

| REVISION | DESCRIPTION | DATE |
|---|---|---|
| **1** | Initial release | August 2013 |

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# Important User Information

In order to lower the risk of personal injury, electric shock, fire, or equipment damage, users must observe the following precautions as well as good technical judgment, whenever this product is installed or used.

All reasonable efforts have been made to ensure the accuracy of this document; however, Eurotech assumes no liability resulting from any error/omission in this document or from the use of the information contained herein.

Eurotech reserves the right to revise this document and to change its contents at any time without obligation to notify any person of such revision or changes.

## Safety Notices and Warnings

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Eurotech assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Eurotech is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

### *Installation in Enclosures*

In the event that the product is placed within an enclosure, together with other heat generating equipment, ensure proper ventilation.

### *Do Not Operate in an Explosive Atmosphere*

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

### *Alerts that can be found throughout this manual*

The following alerts are used within this manual and indicate potentially dangerous situations.

**Danger, electrical shock hazard:**
Information regarding potential electrical shock hazards:

- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

**Warning:**
Information regarding potential hazards:

- Personal injury or death could occur. Also damage to the system, connected peripheral devices, or software could occur if the warnings are not carefully followed.
- Appropriate safety precautions should always be used, these should meet the requirements set out for the environment that the equipment will be deployed in.

**Information and/or Notes:**
These will highlight important features or instructions that should be observed.

### *Use an Appropriate Power Supply*

- Only start the product with a power supply that conforms to the voltage requirements as specified in Power Supply, page 55. In case of uncertainty about the required power supply, please contact your local Eurotech Technical Support Team.
- Avoid overcharging power-points.

### *Antistatic Precautions*

To avoid damage caused by ESD (Electro Static Discharge), always use appropriate antistatic precautions when handing any electronic equipment.

## Life Support Policy

Eurotech products are not authorized for use as critical components in life support devices or systems without the express written approval of Eurotech.

## Warranty

For Warranty terms and conditions users should contact their local Eurotech Sales Office.

See Eurotech Worldwide Presence page 59 for full contact details.

## WEEE

The information below is issued in compliance with the regulations as set out in the 2002/96/EC directive, subsequently superseded by 2003/108/EC. It refers to electrical and electronic equipment and the waste management of such products. When disposing of a device, including all of its components, subassemblies, and materials that are an integral part of the product, you should consider the WEEE directive.

This device is marketed after August 13, 2005 and you must separate all of its components when possible and dispose of them in accordance with local waste disposal legislations.

- Because of the substances present in the equipment, improper use or disposal of the refuse can cause damage to human health and to the environment.
- With reference to WEEE, it is compulsory not to dispose of the equipment with normal urban refuse and arrangements should be instigated for separate collection and disposal.
- Contact your local waste collection body for more detailed recycling information.
- In case of illicit disposal, sanctions will be levied on transgressors.

## RoHS

This device, including all its components, subassemblies and the consumable materials that are an integral part of the product, has been manufactured in compliance with the European directive 2002/95/EC known as the RoHS directive (Restrictions on the use of certain Hazardous Substances). This directive targets the reduction of certain hazardous substances previously used in electrical and electronic equipment (EEE).

## Technical Assistance

If you have any technical questions, cannot isolate a problem with your device, or have any enquiry about repair and returns policies, contact your local Eurotech Technical Support Team.

See Eurotech Worldwide Presence page 59 for full contact details.

### *Transportation*

When transporting any module or system, for any reason, it should be packed using anti-static material and placed in a sturdy box with enough packing material to adequately cushion it.

**Warning:**
Any product returned to Eurotech that is damaged due to inappropriate packaging will not be covered by the warranty.

# Conventions

The following table describes the conventions for signal names used in this document.

| Convention | Explanation |
|---|---|
| **GND** | Digital ground plane |
| **#** | Active low signal |
| **_P** | Positive signal in differential pair |
| **_N or _M** | Negative signal in differential pair |

The following table describes the abbreviations for direction and electrical characteristics of a signal used in this document.

| Type | Explanation |
|---|---|
| **I** | Signal is an input to the system |
| **O** | Signal is an output from the system |
| **IO** | Signal may be input or output |
| **P** | Power and ground |
| **2.5** | 2.5 V signal level |
| **3.3** | 3.3 V signal level |
| **5** | 5 V signal level |
| **A** | Analog signal |
| **HDMI** | Compliant with High-Definition Multimedia Interface Specification |
| **LVDS** | Low Voltage Differential Signalling |
| **MIPI** | Compliant with MIPI Specification |
| **NC** | No Connection |
| **OD** | Open-drain |
| **PCIe** | Compliant with PCI Express v2.0 Specification |
| **Reserved** | Use is reserved to Eurotech |
| **SATA** | Compliant with SATA-2 Specification |
| **USB** | Compliant with Universal Serial Bus 2.0 Specification |

Some signals include on-board termination. The following table describes the abbreviations that specify the signal termination.

| Termination | Explanation |
|---|---|
| **C** | Series capacitor |
| **PD** | Pull-down resistor |
| **PU** | Pull-up resistor to the specified voltage |
| **R** | Series resistor |

# Product Overview

The CPU-301-16 is a rugged, ultra-low power Single Board Computer/Computer on Module based on the Freescale™ i.MX 6 series of application processors. It is available in single-, dual-, and quad-core configurations allowing a scalable solution in a single form factor. Leveraging the processor's integrated 2D/3D graphics and high-definition video capabilities, the CPU-301-16 is optimized for multimedia applications and provides a rich user experience with greater energy efficiency.

To maximize its full functionality, the CPU-301-16 supports integration with an application-specific carrier board through two docking connectors. When coupled with a carrier board, you can implement several industry-standard interfaces allowing development across a broad spectrum of end-use applications. All configurations conform to the same footprint allowing you to easily migrate between modules based on your application needs with no changes to your carrier board. A select group of these interfaces are available through on-board connectors enabling standalone operation without a carrier board.

The CPU-301-16 is available with a variety of operating systems. Support is also available for Eurotech's Everyware™ Software Framework, which provides the MQTT plug-in enabling connection to Eurotech's Everyware™ Cloud.

## Block Diagram

The following diagram illustrates the system organization of the CPU-301-16. Signals are grouped on each connector according to functionality. For the actual signal names and pinout, see Signal Headers, page 46. Dotted lines indicate options.

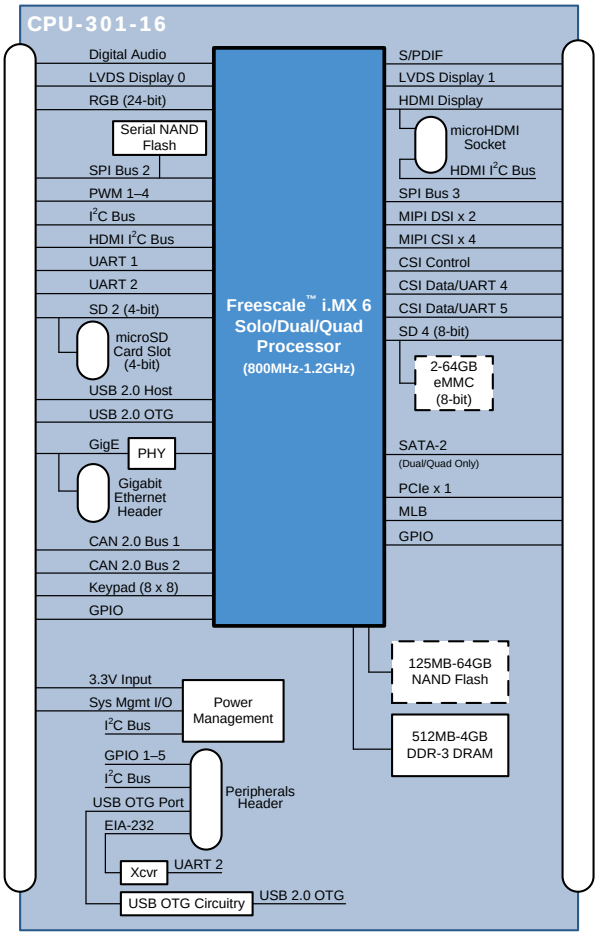



Figure 1. CPU-301-16 Block Diagram

# Features

## *Processor*

- Representative scalable multi-core configurations
  - o Freescale™ i.MX 6Solo
    Single-core ARM Cortex-A9 at 1.0GHz (max),128KB RAM, 512KB unified I/D L2 cache
  - o Freescale™ i.MX 6DualLite
    Dual-core ARM Cortex-A9 at 1.0GHz (max), 128KB RAM, 512KB unified I/D L2 cache shared
  - o Freescale™ i.MX 6Dual
    Dual-core ARM Cortex-A9 at 1.2GHz (max), 256KB RAM, 1MB unified I/D L2 cache shared
  - o Freescale™ i.MX 6Quad
    Quad-core ARM Cortex-A9 at 1.2GHz (max), 256KB RAM, 1MB unified I/D L2 cache shared

## *Memory*

- On-board DDR-3L DRAM
  - o Up to 2GB, 800MT/s (i.MX 6Solo)
  - o Up to 4 GB, 800 MT/s (i.MX 6Dual Lite)
  - o Up to 4GB, 1066 MT/s (i.MX 6Dual/6Quad)
- On-board RAW NAND flash device (options up to 64GB)
- Secure Digital (8-bit) supports
  - o On-board eMMC flash device (options up to 64GB)
  - o SD memory card on carrier board
- Secure Digital (4-bit) supports
  - o On-board microSD expansion slot (up to 64GB, for standalone use)
  - o SD memory card on carrier board
- Support for external SATA disk drive (i.MX 6Dual/6Quad)

## *Computer On Module Mode*

### Communications

- PCI Express port v2.0, one lane
- Universal Serial Bus
  - o USB 2.0 host port (High Speed)
  - o USB 2.0 OTG port (High Speed)
- Up to four serial ports
  - o One 8-wire, TTL-level
  - o One 4-wire, TTL-level
  - o Up to two 4-wire (shared with CMOS Camera)
- Gigabit Ethernet with physical layer transceiver
- Two Controller Area Network ports (CAN 2.0)
- Two $I^2C$ buses with $I^2C$ master device
- Two SPI buses
- Media Local Bus (Contact Eurotech for availability.)

### Graphics and Audio

- Support for up to two (i.MX 6Solo/6Dual Lite) or four (i.MX 6Dual/6Quad) simultaneous displays
  - o Digital (16-, 18-, or 24-bit RGB)
  - o Two LVDS (18- or 24-bit)
  - o HDMI v1.4
  - o MIPI DSI, two lanes
- Camera sensors
  - o CMOS Camera (8-bit)
  - o MIPI CSI, four lanes

- Audio CODEC interface
- Sony Philips Digital Interconnect Format (S/PDIF)

**Inputs and Outputs**

- 8 x 8 Keypad port
- Four Pulse Width Modulation (PWM) outputs
- Five general-purpose inputs and outputs

## *Standalone Single Board Computer Mode*

**Communications**

- USB 2.0 OTG port (High Speed)
- EIA-232 serial port, RX/TX only
- Gigabit Ethernet with physical layer transceiver
- $I^2C$ bus with $I^2C$ master device

**Graphics and Audio**

- HDMI v1.4

**Inputs and Outputs**

- Five general-purpose inputs and outputs

## *Power Supply*

- 3.3 V power input
- Ultra-low power dissipation
- Integrated power management

## *Mechanical*

- 67 mm x 85 mm dimensions

## *Environmental*

- Extended temperature option
- Enhanced vibration tolerance

# Design Checklist

Eurotech provides a host of services to ensure that your product is up and running from the first prototype release. We recommend the following process for every CPU-301-16 carrier board design:

## *Kickoff Stage*

During the Kickoff Stage, you will develop your block diagram and identify any customizations your application may require.

☐ **Gather your reference materials**

Eurotech provides several documents that include key information for designing a custom carrier board. Use the following resources and ask questions:

- CPU-301-16 Design-In Guide
- CPU-301-16 Development Kit User Manual

☐ **Define your requirements**

Define your system's requirement. Be sure to include requirements such as the product features, the input power, the type of transient protection on the power supply, connectivity to the CPU-301-16, and all I/O to your system.

☐ **Create a block diagram**

Create a block diagram of your proposed design. This step helps to formulate the best way to connect different devices to the CPU-301-16.

☐ **Identify customizations**

Identify any customizations that your application requires. Examples of customizations are custom configurations or supporting a device that is not included on Eurotech's standard carrier board.

☐ **Utilize the CPU-301-16 Development Kit**

Utilize the CPU-301-16 Development Kit for validating your proposed design. For example, if a specific display is to be used on the digital display interface, test that display by connecting it to the interface on the CPU-301-16 Development Kit. This testing also allows you to validate your OS image with all required drivers loaded.

☐ **Kickoff review**

Early in the development of your carrier board, meet with your Eurotech representative to review your block diagram and discuss customizations. Incorporate any changes into your design.

## *Preliminary Design Stage*

During the Preliminary Design Stage, you will finalize your block diagram, agree on customizations, and begin your preliminary schematic.

☐ **Follow the design requirements and recommendations**

Follow the design requirements and recommendations listed in this design-in guide. Use Eurotech's carrier board and standard Board Support Package as a starting point for your design. Using the same connectivity to the CPU-301-16 will minimize the time spent in developing your carrier board.

☐ **Preliminary design review**

Stay in contact with your Eurotech representative during your preliminary design. Together, finalize your block diagram and agree on customizations needed. Continue to ask questions as you move towards finalizing your design.

## *Critical Design Stage*

During the Critical Design Stage, you will finalize your schematic making sure that you have met all the electrical, thermal, and mechanical design requirements.

- **Implement power supply sequencing**

  Implement the exact power supply sequencing described in Power Sequences, page 36 of this design-in guide. The CPU-301-16 has very specific power-on sequence requirements in order to power-up and operate correctly. Power sequencing, as described in this section, is CRITICAL.

- **Provide a system-level reset**

  Use the system reset signal RESET_BTN# (J1 B84), described in Power Management Signals, page 36, to reset the CPU-301-16 and all devices on the carrier board.

- **Create a power budget**

  Create a power budget that takes into account the current requirement of the CPU-301-16, as specified in Power Supply, page 55, and of the devices that are used with the CPU-301-16. Design your power supply to handle the maximum current requirement.

- **Determine thermal management**

  Determine what type of thermal management is required for your design. Use your power budget and the information provided in Thermal Management, page 44 of this design-in guide to design a heat spreader, if necessary.

- **Follow the mechanical requirements**

  Follow the exact mechanical requirements given in Mechanical Design, page 42 for mounting holes placement, position of the board-to-board connectors, and stack height on your carrier board design.

- **Use advanced layout and high-speed routing techniques**

  Adhering to good design practices for high-speed PCB design is essential. You should have your schematic 95% complete, especially the high-speed signals and buses, power sequencing, and system reset, before you start board layout. Meet with your Eurotech representative to review your schematic before you begin layout. After your layout is complete, meet again to review your complete design.

- **Have a strategy to debug your design**

  Review your strategy to bring-up and to debug your design. Ensure that you have included the necessary support in your design. The debug serial port (SERIAL_RXD, J11 6 and SERIAL_TXD, J11 7) is extremely important in bring-up of a new design.

- **Critical design review**

  Do an in-depth review of your finished design, including final schematic and board layout, to ensure that you have met all the requirements described in this checklist and throughout this design-in guide. Again, ask your Eurotech representative questions.

## *Prototype Bring-up Stage*

Eurotech provides assistance in bringing-up your prototype at your site or ours. We have several tools that can assist the process.

- **Begin with the basics**

  Begin by checking basic functionality such as power, reset, and clocks. Minimize the number of devices required for bring-up. After you have verified this base level, enable each subsystem as needed. Adding one device at a time will help determine which subsystem, if any, is having problems.

- **Utilize the debug port**

  Utilize the debug port output, described in Debug Serial Port, page 44, to identify problems during bring-up. This port provides important debug information that enables you to monitor the operation of the CPU-301-16.

- **Use your CPU-301-16 Development Kit**

  Use your CPU-301-16 Development Kit to isolate problems. If a problem occurs during bring-up of your carrier board, try to duplicate the problem on the development kit.

- **Prototype bring-up review**

  Review your bring-up process and share lessons learned with your Eurotech representative.

### *Acceptance of Customizations*

Eurotech is committed to your design success. Using our support services throughout the development cycle ensures a complete and robust solution with which to move forward.

- **Customization Acceptance**

  Meet with your Eurotech representative to discuss acceptance of any customizations and to plan the steps toward production of your CPU-301-16 design.

# Development Kit

The CPU-301-16 Development Kit is designed to get the developer up and running quickly. The development kit includes the CPU-301-16, a standard development kit carrier board, display, and cables. To provide flexibility and allow development across a broad spectrum of end-use applications, the carrier board maximizes the CPU-301-16 functionality and implements many industry-standard interfaces. This configuration allows you to become familiar with the CPU-301-16 functionality prior to customization for your specific application. In addition, the standard development kit carrier board provides a reference for custom carrier board design.

For a complete description of the CPU-301-16 Development Kit, refer to the *CPU-301-16 Development Kit User Manual (Eurotech document 110127-5000).*

# Related Documents

This guide provides details about the various features of the CPU-301-16 and about how it creates a system that meets your application needs. It extends the information provided in the *CPU-301-16 Development Kit User Manual* and is intended for hardware design engineers. Design details are provided as guidelines for custom carrier board design.

The following documents are also important resources for the CPU-301-16.

| Document | |
|---|---|
| **CPU-301-16 Development Kit User Manual** | 110127-5000 |
| **CPU-301-16 Development Kit Quick Start** | 110127-5001 |

Table 1. Related Documents

Check the Eurotech support site (http://support.eurotech-inc.com/) for errata reports and for the latest releases of these documents.

# Software Specification

Eurotech provides an application-ready platform including operating system and board support package (BSP). This section gives a brief description of the software support available for the CPU-301-16.

## Operating System Support

The CPU-301-16 is compatible with the following operating systems:

- Windows® Embedded Compact 7
- Linux

For details about availability of other operating systems, contact your local Eurotech representative.

## Boot Devices

The CPU-301-16 has the capability to boot and install the operating system from four sources. The following are the boot device options:

- SD card
- RAW NAND flash device
- eMMC flash device
- SATA drive

The boot option is selected at power up based on the setting of the BOOT_CFG signals. For a detailed description of these signals, see Boot Mode Configuration, page 38.

## Board Support Package

Eurotech has constructed a standard board support package (BSP) that supports the feature set implemented on Eurotech's standard carrier board. Since most of the i.MX 6 processor I/O pads can be configured to work in more than one functional mode, this feature set was carefully selected to provide an optimal system solution. Eurotech's carrier board maximizes the full functionality of the CPU-301-16 and implements several commonly-used, industry-standard interfaces. Eurotech highly recommends utilizing the I/O mapping implemented on this carrier board along with the supporting BSP wherever possible in your application. If you do not require a specific function, those associated processor I/O can be used for general-purpose. However, any changes will require a custom BSP. Contact your local Eurotech representative to discuss any customizations.

## Everyware™ Software Framework

Everyware Software Framework (ESF) is an inclusive software framework that puts a middleware layer between the operating system and the OEM application. It provides industry-standard interfaces that shorten development time, simplify coding, and allow software to be ported from one Eurotech hardware platform to another. The CPU-301-16 supports ESF. If your application requires ESF, contact your local Eurotech representative.

Information about ESF is available at http://esf.eurotech.com.

# Hardware Specification

## Core Processor

The CPU-301-16 bases its architecture on the Freescale i.MX 6 series of application processors. It implements the single- (i.MX 6Solo), dual- (i.MX 6DualLite or i.MX 6Dual), or quad-core (i.MX 6Quad) processor providing a scalable solution in a single form factor. The processors are multimedia-focused and offer high-performance processing with 2D/3D graphics display and high-definition video capabilities. In addition, the processors support Freescale's Dynamic Voltage and Frequency Scaling (DVFS) to minimize power consumption while optimizing performance.

The processor provides a wide range of memory, communication, display, camera, user interface, discrete inputs/outputs and audio capabilities. Subsequent sections describe these features as it relates to the CPU-301-16 architecture.

## Memory

The CPU-301-16, standalone or combined with a carrier board, provides a variety of storage capabilities. The following sections describe the different types of memory supported and provide details about implementation.

### *Synchronous DRAM*

Double Data Rate Synchronous DRAM (DDR-3) is used on the CPU-301-16 for system main memory. Standard options of 512MB to 4GB are available. If your application requires a custom configuration, contact your local Eurotech representative.

The following table describes the on-board DDR-3L DRAM for each configuration.

| Processor | i.MX 6Solo | i.MX 6Dual Lite | i.MX 6Dual | i.MX 6Quad |
|---|---|---|---|---|
| **DDR-3L DRAM** | Up to 2GB<br>800MT/s | Up to 4 GB<br>800 MT/s | Up to 4GB<br>1066 MT/s | Up to 4GB<br>1066 MT/s |

Figure 2. Synchronous DRAM

### *Serial NAND Flash*

An on-board flash memory device stores the configuration data and MAC address. Standard configuration is 2 MB. The flash device connects to the processor using the SPI 2 bus.

### *eMMC Flash*

The CPU-301-16 supports an optional on-board eMMC flash memory device connected to the SD 4 interface. Configurations of up to 64GB are available. In addition to providing mass storage, this memory is a boot option. For additional details about the boot options, see Boot Mode Configuration, page 38.

**Notes:**
The eMMC flash memory device is mutually exclusive with SD 4 (J2, page 49) and the RAW NAND flash memory device.

## RAW NAND Flash

The CPU-301-16 supports an optional on-board RAW NAND flash memory device. Configurations up to 64GB are available. Contact your local Eurotech representative for availability. In addition to providing mass storage, this memory is a boot option. For additional details about the boot options, see Boot Mode Configuration, page 38.

**Notes:**
The RAW NAND flash memory device is mutually exclusive with SD 4 (J2, page 49) and the eMMC flash memory device.

## External Memory Interfaces

Four types of external memory interfaces provide mass storage options for the CPU-301-16. Using a carrier board, you can connect a SATA disk drive, USB mass storage device, SD memory card, and PCIe memory card to the CPU-301-16. Include support circuitry and connectors on your carrier board. For standalone use, an on-board microSD card slot is included allowing direct connection to a memory card.

The high-speed differential and single-ended signals associated with these external memory interfaces require strict routing constraints on the carrier board. Be sure to follow best high-speed design practices.

### SATA Disk Drive

The i.MX 6Dual processor and i.MX 6Quad processor configurations of the CPU-301-16 support a serial ATA (SATA) bus on connector J2, page 49 enabling connection of a high-capacity, removable storage SATA disk drive through a carrier board. This interface supports the Serial ATA II Specification with data transfer rates of up to 3.0 Gbps. In addition to providing mass storage, this memory is a boot option. For additional details about the boot options, see Boot Mode Configuration, page 38. The following diagram illustrates the SATA connectivity on the CPU-301-16.

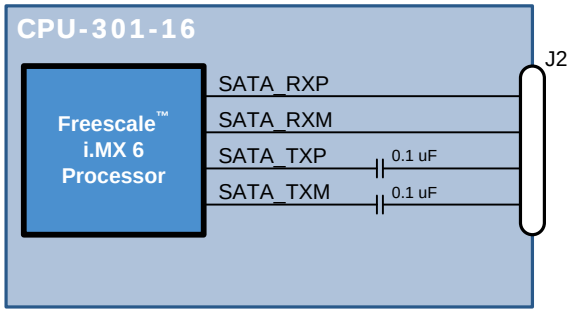



Figure 3. SATA Connectivity

Notice that the CPU-301-16 includes 0.1µF AC coupling capacitors on the transmit differential pair. On your carrier board, include 0.1µF AC coupling capacitors on the receive differential pair. Place the capacitors near the SATA connector on the carrier board. Also, the SATA signals route directly from the processor. Include ESD protection on your carrier board.

The following table lists the SATA signals.

| Connector J2 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|
| **A81** | SATA_RXM | I-SATA | | Receive negative |
| **A82** | SATA_RXP | I-SATA | | Receive positive |
| **A84** | SATA_TXM | O-SATA | C 0.1µF | Transmit negative |
| **A85** | SATA_TXP | O-SATA | C 0.1µF | Transmit positive |

Table 2. Serial ATA Signals

### USB Mass Storage Device

A USB mass storage device can connect to the USB host port provided on connector J1, page 46. Any USB device that has USB drivers installed on the CPU-301-16 can connect to this port through a carrier board. For a description of this port, see Universal Serial Bus, page 19.

### Secure Digital

The CPU-301-16 includes two Secure Digital (SD) interfaces for memory and I/O expansion. These interfaces are compliant with the following specifications:

- MultiMediaCard System Specification,v4.2/4.3/4.4
  (MMC command/response sets and Physical Layer including high-capacity cards HC MMC, > 2 GB)
- SD Memory Card Specifications, v3.0
  (SD command/response sets and Physical Layer including high-capacity SDHC cards, up to 32 GB)
- SDIO Card Specification, Part E1, v1.10
  (SDIO command/response sets and interrupt/read-wait mode)
- SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00

SD 2 supports 1- or 4-bit data transfers. It is available on docking connector J1, page 46 for use with a carrier board or on J3, page 52 for connection to a microSD card in standalone use. SD 4 supports 1-, 4-, or 8-bit data transfers. This interface connects to J2, page 49 for use with a carrier board or an on-board eMMC flash memory device. Both SD interfaces support 3.3 V levels only. The following diagram illustrates the connectivity of the SD interfaces on the CPU-301-16.

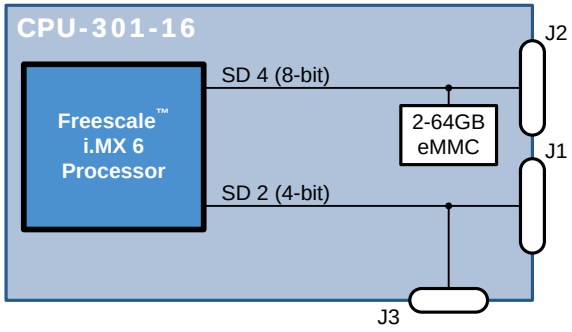



Figure 4. Secure Digital Interface Connectivity

The CPU-301-16 can boot from any device connected to SD 2 or SD 4. For additional details about the boot options, see Boot Mode Configuration, page 38.

The following table lists the signals for the SD interfaces.

| Connector J1 | Connector J2 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|---|
| **Secure Digital Interface 4** | | | | | |
| | **B42** | SD4_CMD | IO-3.3 | | Command |
| | **B43** | SD4_DAT0 | IO-3.3 | | Data 0 |
| | **B44** | SD4_DAT1 | IO-3.3 | | Data 1 |
| | **B45** | SD4_DAT2 | IO-3.3 | | Data 2 |
| | **B46** | SD4_DAT3 | IO-3.3 | | Data 3 |
| | **B47** | SD4_DAT4 | IO-3.3 | | Data 4 |
| | **B48** | SD4_DAT5 | IO-3.3 | | Data 5 |
| | **B49** | SD4_DAT6 | IO-3.3 | | Data 6 |
| | **B50** | SD4_DAT7 | IO-3.3 | | Data 7 |
| | **B52** | SD4_CLK | O-3.3 | R 33Ω | Clock |
| | **B53** | SD4_CD# | I-3.3 | | Card Detect |
| | **B54** | SD4_WP | I-3.3 | | Write Protect |
| | **B55** | SD4_PWR_EN# | O-3.3 | | Power enable |
| | **B56** | VDD_SD | PO | | SD power (note 1) |
| | **B57** | VDD_SD | PO | | SD power (note 1) |

| Connector J1 | Connector J2 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|---|
| **Secure Digital Interface 2** | | | | | |
| **B9** | | SD2_WP | I-3.3 | PU 47kΩ VDD_SD | Write Protect |
| **B10** | | SD2_CD# | I-3.3 | PU 47kΩ VDD_SD | Card Detect |
| **B12** | | SD2_CLK | O-3.3 | R 33Ω | Clock |
| **B13** | | SD2_CMD | IO-3.3 | PU 47kΩ VDD_SD | Command |
| **B14** | | SD2_DAT0 | IO-3.3 | | Data 0 |
| **B15** | | SD2_DAT1 | IO-3.3 | | Data 1 |
| **B16** | | SD2_DAT2 | IO-3.3 | | Data 2 |
| **B17** | | SD2_DAT3 | IO-3.3 | | Data 3 |
| **B27** | | GPIO4_IO3/GPIO_SD4_PWR_EN# | O-3.3 | | Power enable |

Notes:

1. Use VDD_SD (3.3 V) to power an SD slot on the carrier board.

Table 3. Secure Digital Signals

**Notes:**
SD 4 is mutually exclusive with the eMMC flash memory device and the RAW NAND flash memory device.

### PCI Express Memory Card

A PCI Express (PCIe) memory card can connect to the PCIe x1 port available on connector J2, page 49. For a description of the PCIe capability, see PCI Express, page 18.

# Communications

The CPU-301-16 supports several industry-standard channels for communication with peripheral and peer devices on the carrier board. These interfaces include PCI Express, USB, serial ports, Gigabit Ethernet, CAN, $I^2C$ bus, SPI bus, and MLB as described in the following sections.

The high-speed differential and single-ended signals associated with these external interfaces require strict routing constraints on the carrier board. Be sure to follow best high-speed design practices.

## *PCI Express*

The CPU-301-16 provides a PCI Express port v2.0, one lane (PCIe x 1) available on connector J2, page 49. In addition, Eurotech's standard BSP defines one processor GPIO signal as a reset output for an external PCIe device. This signal is included on connector J1, page 46. The following diagram illustrates the PCIe connectivity on the CPU-301-16.

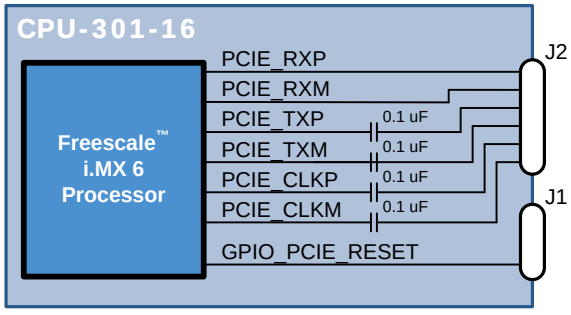



Figure 5. PCI Express Connectivity

You can use this interface to connect to peripherals integrated on a carrier board or to implement a PCIe slot allowing connectivity to add-on expansion cards. Notice that the CPU-301-16 includes 0.1µF AC coupling capacitors on the transmit and clock differential pair. On your carrier board, include 0.1µF AC coupling capacitors on the receive differential pair and 49.9 Ω termination resistors on the clock differential pair. Place the components near the PCIe connector on the carrier board.

The following table lists the PCIe signals.

| Connector J1 | Connector J2 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|---|
| | **A22** | PCIE_RXM | I_PCIe | | Receive negative |
| | **A23** | PCIE_RXP | I_PCIe | | Receive positive |
| | **A25** | PCIE_TXM | O-PCIe | C 0.1µF | Transmit negative |
| | **A26** | PCIE_TXP | O-PCIe | C 0.1µF | Transmit positive |
| | **A28** | PCIE_CLKM | O | C 0.1µF | Clock negative |
| | **A29** | PCIE_CLKP | O | C 0.1µF | Clock positive |
| **B57** | | GPIO5_IO15/GPIO_PCIE_RESET | O-3.3 | | External PCIe device reset |

Table 4. PCI Express Signals

## *Universal Serial Bus*

Supporting the USB 2.0 specification at High Speed (480 Mbps), the CPU-301-16 includes a Universal Serial Bus (USB) host port and USB On-The-Go (OTG) port.

### USB Host

The USB host signals are available on connector J1, page 46 with associated over-current detection input and power enable output. In addition, Eurotech's standard BSP defines four processor GPIO signals as reset and power enable outputs to support a USB hub implemented on the carrier board. The following diagram illustrates the USB 2.0 Host connectivity on the CPU-301-16.

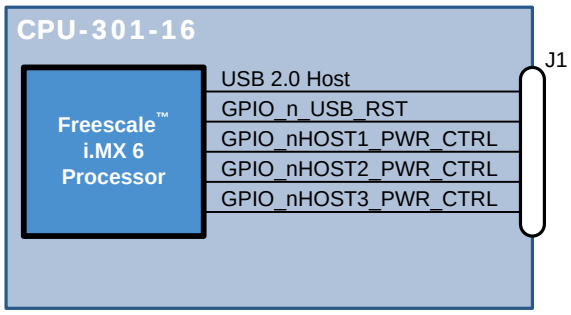



Figure 6. USB 2.0 Connectivity

Use this USB host port to connect external devices to the CPU-301-16 when used with a carrier board. In order to create a fully functioning USB host port, include the host power supply, current limiter circuit, EMI suppression filter, and over-voltage protection on your carrier board. The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The carrier board must supply the 5 V power required by client devices. Use a power switch with the over-current detection signal. USB mouse and keyboard are the most common client devices, but you can connect any USB device that has USB drivers installed on the I.MX 6.

The following table lists the USB 2.0 Host signals.

| Connector J1 | Signal Name | Type | Description |
|---|---|---|---|
| **A42** | USB_HOST_DN | IO-USB | Data negative |
| **A43** | USB_HOST_DP | IO-USB | Data positive |
| **A45** | USB_H_OC# | I-3.3 | Over current |
| **A46** | USB_H_PWR_EN | O-3.3 | Power enable |
| **A52** | GPIO5_IO1/GPOI_nUSB_RST | O-3.3 | External USB hub reset |
| **B50** | GPIO5_IO9/GPIO_nHOST1_PWR_CTRL | O-3.3 | External USB hub host 1 power enable |
| **B52** | GPIO5_IO10/GPIO_nHOST2_PWR_CTRL | O-3.3 | External USB hub host 2 power enable |
| **B53** | GPIO5_IO11/GPIO_nHOST3_PWR_CTRL | O-3.3 | External USB hub host 3 power enable |

Table 5. USB 2.0 Host Signals

### USB On-The_Go

The USB On-The-Go (OTG) port is capable of dynamically switching between a host and client allowing point-to-point connections between USB devices that have traditionally been peripheral-only. The USB OTG signals with associated ID input are available on connector J1, page 46. In addition to providing the USB OTG signals on J1, the CPU-301-16 includes an EMI suppression filter, current limiter circuit, voltage regulator, and detection circuit to provide a fully functioning USB OTG port on header J11, page 54. This capability allows direct connection to other USB OTG devices or to a personal computer in standalone use. The following diagram illustrates the USB 2.0 OTG connectivity on the CPU-301-16.

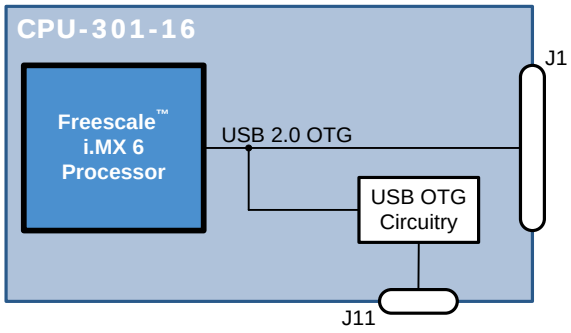



Figure 7. USB 2.0 OTG Connectivity

On your carrier board, use the signals provided on J1 to implement a USB OTG or USB client port. Include EMI suppression and ESD protection if you are not using a buffer.

The following table lists the USB OTG signals for connector J1. For the pinout of connector J11, see connector J11, page 54.

| Connector J1 | Signal Name | Type | Description |
|---|---|---|---|
| **B42** | USB_OTG_DN | IO-USB | Data negative |
| **B43** | USB_OTG_DP | IO-USB | Data positive |
| **B45** | USB_OTG_ID | I-3.3 | ID input |
| **B46** | VDD_USB_5V | PIO | Power input/output (5 V) |
| **B47** | VDD_USB_5V | PIO | Power input/output (5 V) |
| **B48** | VDD_USB_5V | PIO | Power input/output (5 V) |

Table 6. USB OTG Signals

## *Serial Ports*

The CPU-301-16 provides the signals for up to four serial ports. The following table describes the serial ports on the CPU-301-16.

| Serial Port | Connector | Description |
|---|---|---|
| **1** | J1, page 46 | Full-function, 3.3V levels |
| **2** | J1, page 46 | 4-wire, 3.3V levels |
| | J11, page 54 | RX/TX only,EIA-232 levels (note 2) |
| **4** | J2, page 49 | 4-wire, 3.3V levels (note 3) |
| **5** | J2, page 49 | 4-wire, 3.3V levels (note 3) |

Notes:

2. The RX/TX signals of Serial port 2 are provided at EIA-232 levels on J11 for direct connection to the board in standalone use.
3. Serial ports 4 and 5 share I/O pins with the CMOS Camera interface.

Table 7. Serial Ports

In addition to the serial port signals, Eurotech's standard BSP defines three processor GPIO signals as enable outputs to support external EIA-232/422/485 transceivers. These signals are available on connector J1, page 46.

The following diagram illustrates the serial port connectivity on the CPU-301-16.

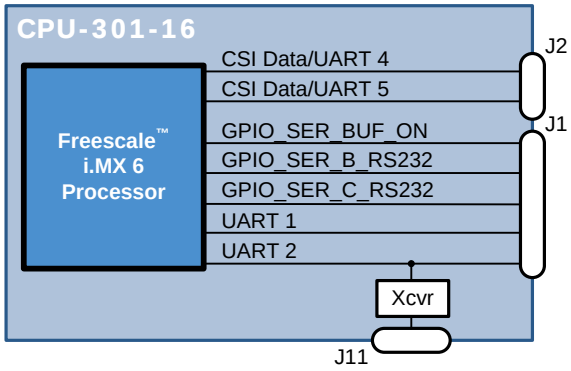



Figure 8. Serial Port Connectivity

Notice that the serial port signals route directly to the processor. If your application requires EIA-232/422/485, include transceivers on your carrier board. If you are not using transceivers, include series termination and ESD protection.

The following table lists the signals for the serial ports for connectors J1 and J2. For the pinout of connector J11, see connector J11, page 54.

| Connector J1 | Connector J2 | Signal Name | Type | Description |
|---|---|---|---|---|
| **Serial port 1 (UART 1)** | | | | |
| **A2** | | UART1_DCD | I-3.3 | Data Carrier Detect |
| **A3** | | UART1_DSR | I-3.3 | Data Set Ready |
| **A4** | | UART1_RXD | I-3.3 | Receive Data |
| **A5** | | UART1_RTS | O-3.3 | Request To Send |
| **A6** | | UART1_TXD | O-3.3 | Transmit Data |
| **A7** | | UART1_CTS | I-3.3 | Clear To Send |
| **A8** | | UART1_DTR | O-3.3 | Data Terminal Ready |
| **A9** | | UART1_RI | I-3.3 | Ring Indicator |
| **Serial port 2 (UART2)** | | | | |
| **B2** | | UART2_RXD | I-3.3 | Receive Data (note 2) |
| **B3** | | UART2_RTS | O-3.3 | Request To Send |
| **B4** | | UART2_TXD | O-3.3 | Transmit Data (note 2) |
| **B5** | | UART2_CTS | I-3.3 | Clear To Send |
| **External buffer control** | | | | |
| **B6** | | GPIO5_IO7/GPIO_SER_BUF_ON | O-3.3 | External EIA-232 buffer shutdown |
| **B18** | | GPIO3_IO1/GPIO_SER_B_RS232 | O-3.3 | External EIA-232 buffer enable |
| **B19** | | GPIO3_IO2/GPIO_SER_C_RS232 | O-3.3 | External EIA-232 buffer enable |
| **Serial port 4 (UART 4)** | | | | |
| | **A12** | UART4_TXD_CSI_DAT12 | O-3.3 | Transmit Data (CMOS Camera, Data 12) |
| | **A13** | UART4_RXD_CSI_DAT13 | I-3.3 | Receive Data (CMOS Camera, Data 13) |
| | **A16** | UART4_RTS_CSI_DAT16 | O-3.3 | Request To Send (CMOS Camera, Data 16) |
| | **A17** | UART4_CTS_CSI_DAT17 | I-3.3 | Clear To Send (CMOS Camera, Data 17) |
| **Serial port 5 (UART 5)** | | | | |
| | **A14** | UART5_TXD_CSI_DAT14 | O-3.3 | Transmit Data (CMOS Camera, Data 14) |
| | **A15** | UART5_RXD_CSI_DAT15 | I-3.3 | Receive Data (CMOS Camera, Data 15) |
| | **A18** | UART5_RTS_CSI_DAT18 | O-3.3 | Request To Send (CMOS Camera, Data 18) |
| | **A19** | UART5_CTS_CSI_DAT19 | I-3.3 | Clear To Send (CMOS Camera, Data 19) |

Table 8. Serial Port Signals

**Notes:**
The CMOS camera port shares processor I/O pins with Serial ports 4 and 5. Therefore, these functions are mutually exclusive.

## *Gigabit Ethernet*

The i.MX 6 series processor includes a Gigabit Ethernet Media Access Controller (MAC) that conforms to the IEEE 802.3 standard. This MAC device connects to an on-board Ethernet physical layer transceiver supporting a Media Dependent Interface (MDI) for 10Base-T, 100Base-TX, and 1000Base-T applications. In addition, the transceiver drives two programmable LED control signals. The Ethernet signals are available on connector J1, page 46 for use with a carrier board. In addition to including the MDI on J1, header J9, page 53 provides the signals for connection to the MDI in standalone use. The following diagram illustrates the Gigabit Ethernet connectivity on the CPU-301-16.

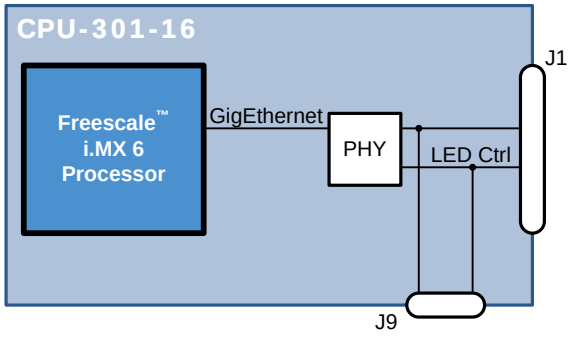



Figure 9. Gigabit Ethernet Connectivity

Include magnetics, termination, and an RJ-socket on your carrier board to complete the connection to your network. To turn on the LEDs, the transceiver pulls the signals ETH_LED1_C and ETH_LED2_C to a low logic-level. On your carrier board, do not include external pull down resistors on ETH_LED1_C and ETH_LED2_C. Ensure that you turn off the supply to the LEDs when ON_STATE is de-asserted low to prevent back power. For additional details about this signal, see Power Management Signals, page 36.

The following table lists the Gigabit Ethernet signals.

| Connector J1 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|
| **A94** | ETH_TXRX2P | IO-A | | MDI 2 positive signal |
| **A95** | ETH_TXRX2M | IO-A | | MDI 2 negative signal |
| **A97** | ETH_TXRX3P | IO-A | | MDI 3 positive signal |
| **A98** | ETH_TXRX3M | IO-A | | MDI 3 negative signal |
| **B91** | ETH_LED1_C | O | PU 10kΩ 2.5 V | LED 1, Cathode |
| **B92** | ETH_LED2_C | O | PU 10kΩ 2.5 V | LED 2, Cathode |
| **B94** | ETH_TXRX1P | IO-A | | MDI 1 positive signal |
| **B95** | ETH_TXRX1M | IO-A | | MDI 1 negative signal |
| **B97** | ETH_TXRX0P | IO-A | | MDI 0 positive signal |
| **B98** | ETH_TXRX0M | IO-A | | MDI 0 negative signal |

Table 9. Gigabit Ethernet Signals

## CAN 2.0B Bus

Supporting the CAN 2.0B Protocol Specification with bit rates up to 1 Mbps, the CPU-301-16 provides two Controller Area Network (CAN) buses. The two buses are available on connector J1, page 46. The following diagram illustrates the connectivity of CAN 2.0 buses on the CPU-301-16.

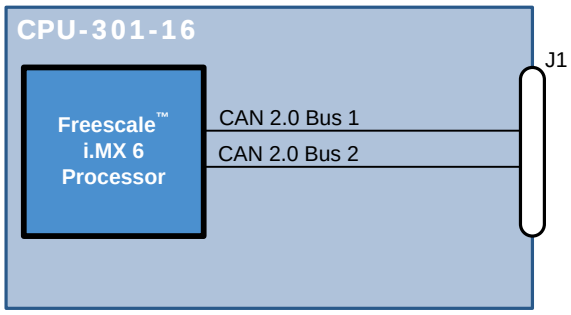



Figure 10. CAN 2.0 Bus Connectivity

Include a transceiver, common mode filter, and ESD protection on your carrier board. The CAN 2.0 signals are 3.3V tolerant. If your transceiver is specified for 5V, include a level translator also.

The following table lists the CAN 2.0 bus signals.

| Connector J1 | Signal Name | Type | Description |
|---|---|---|---|
| **A47** | TX_CAN1 | O-3.3 | CAN Bus 1 |
| **A48** | RX_CAN1 | I-3.3 | CAN Bus 1 |
| **A49** | TX_CAN2 | O-3.3 | CAN Bus 2 |
| **A50** | RX_CAN2 | I-3.3 | CAN Bus 2 |

Table 10. CAN 2.0 Bus Signals

## I²C Bus

I²C (Inter-IC) bus is a multi-master, “two-wire” synchronous serial bus for communications between integrated circuits (ICs) and for addressing peripherals in a system. The CPU-301-16 provides external connections to two I²C buses with the I.MX 6 series processor acting as the bus master for each bus. This section provides details about the general-purpose I²C bus. For details about the HDMI I²C bus, see HDMI Display, page 28.

### General-purpose I²C Bus

The general-purpose I²C bus (I2C3_SDA, I2C3_SCL) connects to the on-board Power Management Integrated Circuit (PMIC) and is available on connectors J1, page 46 and J11, page 54. The following diagram illustrates the connectivity of this I²C bus on the CPU-301-16.

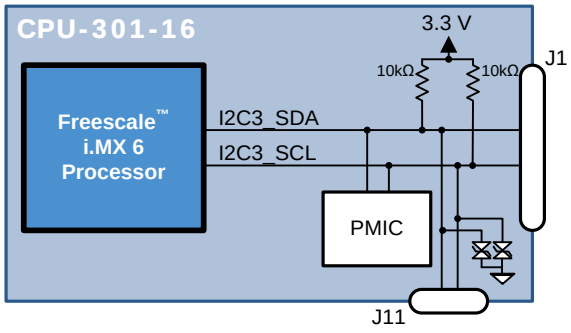



Figure 11. General-purpose I²C Bus Connectivity

Use the general-purpose I²C bus to communicate with external devices on your carrier board. Notice that the board includes 10kΩ pull-up resistors to 3.3 V and ESD protection on the data and clock signals for standalone use. When using a carrier board, do not rely on the ESD protection circuit on the CPU-301-16. Include ESD protection at the source on your carrier board for the signals on connector J1.

The following table lists the signals for the general-purpose I²C bus for connector J1. For the pinout of connector J11, see connector J11, page 54.

| Connector J1 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|
| **B7** | I2C3_SDA | IO-3.3 | PU 10kΩ V3.3 | I²C data for general-purpose use |
| **B8** | I2C3_SCL | O-3.3 | PU 10kΩ V3.3 | I²C data for general-purpose use |

Table 11. General-purpose I²C Bus Signals

## *SPI Bus*

The Serial Peripheral Interface (SPI) is a synchronous serial port that consists of a clock, transmit, receive, ground, and one or more device selects. Each device on the bus requires its own select line. Buses may be full or half duplex, clocking data one or both directions at the same time, respectively. The CPU-301-16 provides external connections to two SPI buses with the i.MX 6 series processor acting as the bus master for both buses. This section provides details about the general-purpose SPI bus. For details about the SPI bus intended for use with an external touch panel controller, see Touch Panel Control, page 28.

### General-purpose SPI Bus

The general-purpose SPI bus (SPI3) is available on connector J2, page 49. The following diagram illustrates the connectivity of this bus on the CPU-301-16.

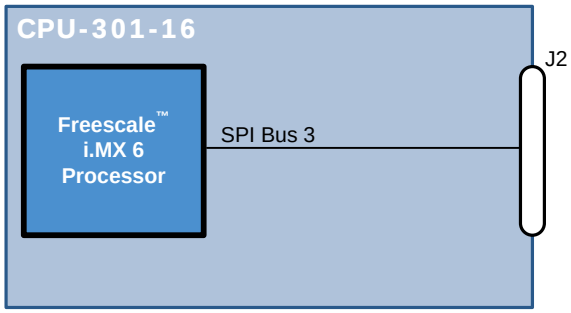



Figure 12. SPI Bus Connectivity

Notice that the SPI bus routes directly from the processor. Include series termination and ESD protection on your carrier board.

The following table lists the signals for the general-purpose SPI bus.

| Connector J2 | Signal Name | Type | Description |
|---|---|---|---|
| **A2** | SPI3_MISO | I-3.3 | Master input |
| **A3** | SPI3_MOSI | O-3.3 | Master output |
| **A4** | SPI3_RDY | I-3.3 | Ready |
| **A5** | SPI3_SCLK | O-3.3 | Serial clock |
| **A6** | SPI3_SS0 | O-3.3 | Chip select 0 |

Table 12. Serial Peripheral Interface Signals

## *Media Local Bus*

Contact Eurotech for availability of Media Local Bus.

# Graphics and Audio

The i.MX 6 series processor's high-performing unified graphics and video processing units along with its flexible display and camera support provide for a rich user experience in a wide variety of multimedia applications. The i.MX 6Solo/6Dual Lite processor supports up to two simultaneous display ports, while the i.MX 6Dual/6Quad processor supports up four simultaneous display ports:

- Digital (16-, 18-, or 24-bit RGB)
- Two LVDS (18- or 24-bit)
- HDMI v1.4 (available in standalone use and with a carrier board)
- MIPI DSI, two lanes

All processors provide inputs for the following camera sensors:

- CMOS Camera (8-bit)
- MIPI CSI, four lanes

In addition to its flexible display and camera capabilities, the audio interface, SPI bus, Pulse Width Modulation (PWM) outputs, and general-purpose inputs and outputs (GPIO) can be used to support an external audio codec, resistive touchscreen, and display backlights. This section summarizes the display, camera, and audio capabilities.

## *Digital Display*

To support display devices such as medium resolution LCDs, the CPU-301-16 provides a parallel digital display output on connector J1, page 46. This output includes red, green, and blue data, as well as horizontal sync, vertical sync, pixel clock, and data ready signals. In addition, Eurotech's standard BSP defines two processor GPIO signals as panel enable and external buffer enable outputs. The following diagram illustrates the digital display connectivity on the CPU-301-16.

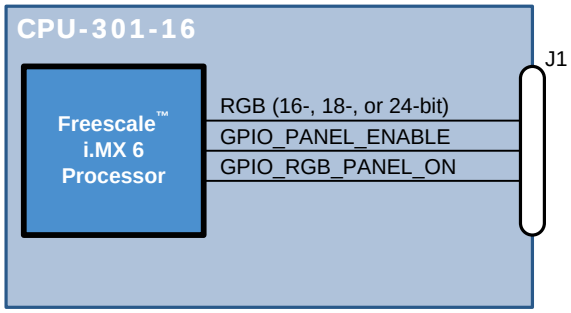



Figure 13. Digital Display Connectivity

To connect to a display, add buffers, termination, output filters and display power switch on your carrier board.

The following table lists the signals for the digital display.

| Connector J1 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|
| **A59** | GPIO3_IO3/GPIO_PANEL_ENABLE | O-3.3 | | Panel enable |
| **A62** | DISP_DAT23 | O-3.3 | | Data 23 |
| **A63** | DISP_DAT22 | O-3.3 | | Data 22 |
| **A64** | DISP_DAT21 | O-3.3 | | Data 21 |
| **A65** | DISP_DAT20 | O-3.3 | | Data 20 |
| **A66** | DISP_DAT19 | O-3.3 | | Data 19 |
| **A67** | DISP_DAT18 | O-3.3 | | Data 18 |
| **A68** | DISP_DAT17 | O-3.3 | | Data 17 |
| **A69** | DISP_DAT16 | O-3.3 | | Data 16 |
| **A71** | DISP_DAT15 | O-3.3 | | Data 15 |
| **A72** | DISP_DAT14 | O-3.3 | | Data 14 |
| **A73** | DISP_DAT13 | O-3.3 | | Data 13 |
| **A74** | DISP_DAT12 | O-3.3 | | Data 12 |
| **A75** | DISP_DAT11 | O-3.3 | | Data 11 |
| **A76** | DISP_DAT10 | O-3.3 | | Data 10 |
| **A77** | DISP_DAT9 | O-3.3 | | Data 9 |
| **A78** | DISP_DAT8 | O-3.3 | | Data 8 |
| **A79** | DISP_DAT7 | O-3.3 | | Data 7 |
| **A81** | DISP_DAT6 | O-3.3 | | Data 6 |
| **A82** | DISP_DAT5 | O-3.3 | | Data 5 |
| **A83** | DISP_DAT4 | O-3.3 | | Data 4 |
| **A84** | DISP_DAT3 | O-3.3 | | Data 3 |
| **A85** | DISP_DAT2 | O-3.3 | | Data 2 |
| **A86** | DISP_DAT1 | O-3.3 | | Data 1 |
| **A87** | DISP_DAT0 | O-3.3 | | Data 0 |
| **A88** | DISP_HSYNC | O-3.3 | | Horizontal sync |
| **A89** | DISP_DRDY | O-3.3 | | Data ready |
| **A91** | DISP_VSYNC | O-3.3 | | Vertical sync |
| **A92** | DISP_PIXCLK | O-3.3 | R 33Ω | Pixel clock |
| **B23** | GPIO1_IO3/GPIO_RGB_PANEL_ON | O-3.3 | | External buffer enable |

Table 13. Digital Display Signals

## *LVDS Display*

Low Voltage Differential Signaling (LVDS) provides a high-speed, low-power serial interface on a single pair of wires per channel addressing the design requirements of today's higher resolution displays. The CPU-301-16 provides two LVDS display outputs. The first LVDS display output (LVDS0) is available on connector J1, page 46, while the second output (LVDS1) is available on connector J2, page 49. Each output consists of four LVDS data pairs, as well as a LVDS pixel clock and supports 18- or 24-bit data. In addition, Eurotech's standard BSP defines one processor GPIO signal as a power enable output. This signal is available on J1. The following diagram illustrates the LVDS display connectivity on the CPU-301-16.

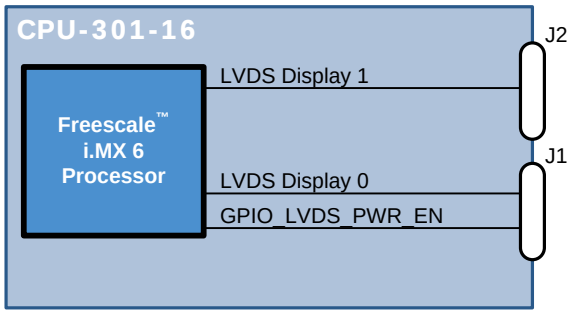



Figure 14. LVDS Display Connectivity

If your application requires transmission over a long display cable, include an LVDS buffer/repeater on your carrier board to boost the data and pixel clock signals. Include EMI Suppression and ESD protection if you are not using a buffer/repeater. Use controlled impedance cables that target 90 Ω ± 25%. Cables should not introduce major impedance discontinuities that cause signal reflections.

The following table lists the signals for the LVDS display.

| Connector J1 | Connector J2 | Signal Name | Type | Description |
|---|---|---|---|---|
| **LVDS Display 0** | | | | |
| **B61** | | LVDS0_TX0N | O-LVDS | Data 0 negative |
| **B62** | | LVDS0_TX0P | O-LVDS | Data 0 positive |
| **B64** | | LVDS0_TX1N | O-LVDS | Data 1 negative |
| **B65** | | LVDS0_TX1P | O-LVDS | Data 1 positive |
| **B67** | | LVDS0_TX2N | O-LVDS | Data 2 negative |
| **B68** | | LVDS0_TX2P | O-LVDS | Data 2 positive |
| **B71** | | LVDS0_TX3N | O-LVDS | Data 3 negative |
| **B72** | | LVDS0_TX3P | O-LVDS | Data 3 positive |
| **B74** | | LVDS0_CLKN | O-LVDS | Clock negative |
| **B75** | | LVDS0_CLKP | O-LVDS | Clock positive |
| **LVDS Display 1** | | | | |
| | B61 | LVDS1_TX0N | O-LVDS | Data 0 negative |
| | B62 | LVDS1_TX0P | O-LVDS | Data 0 positive |
| | B64 | LVDS1_TX1N | O-LVDS | Data 1 negative |
| | B65 | LVDS1_TX1P | O-LVDS | Data 1 positive |
| | B67 | LVDS1_TX2N | O-LVDS | Data 2 negative |
| | B68 | LVDS1_TX2P | O-LVDS | Data 2 positive |
| | B71 | LVDS1_TX3N | O-LVDS | Data 3 negative |
| | B72 | LVDS1_TX3P | O-LVDS | Data 3 positive |
| | B74 | LVDS1_CLKN | O-LVDS | Clock negative |
| | B75 | LVDS1_CLKP | O-LVDS | Clock positive |
| **LVDS Display Power Control** | | | | |
| **B56** | | GPIO5_IO14/GPIO_LVDS_PWR_EN | O-3.3 | Power enable |

Table 14. LVDS Display Signals

## *Backlight Control*

Backlights can easily become the greatest source of power consumption in a portable system. To reduce power consumption, most backlight inverters include control signals to dim and turn off the backlight. To support these features, the CPU-301-16 includes Pulse Width Modulation (PWM) outputs that can be used for backlight control. Each output has a resolution of 16-bit. In addition, Eurotech's standard BSP defines three processor GPIO signals as outputs used to turn power to the backlight on or off. These outputs are available on connector J1, page 46 and connector J2, page 49. The following diagram illustrates the backlight control signals on the CPU-301-16.

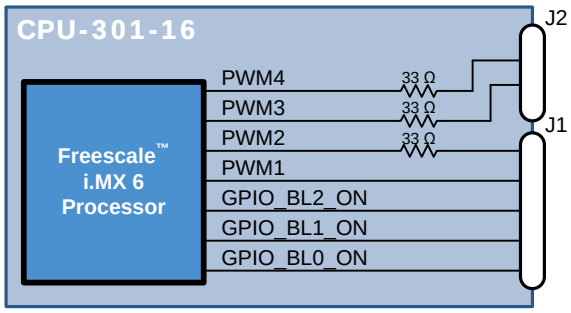



Figure 15. Backlight Control Connectivity

The following table lists the backlight control signals.

| Connector J1 | Connector J2 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|---|
| **A58** | | GPIO5_IO8/GPIO_BL0_ON | O-3.3 | | Backlight 0 on/off |
| **B20** | | GPIO1_IO1/GPIO_BL1_ON | O-3.3 | | Backlight 1 on/off |
| **B22** | | GPIO1_IO2/GPIO_BL2_ON | O-3.3 | | Backlight 2 on/off |
| **B78** | | PWM1 | O-A | | Pulse Width Modulator 1 |
| **B79** | | PWM2 | O-A | R 33Ω | Pulse Width Modulator 2 |
| | **B77** | PWM3 | O-A | R 33Ω | Pulse Width Modulator 3 |
| | **B78** | PWM4 | O-A | R 33Ω | Pulse Width Modulator 4 |

Table 15. Backlight Control Signals

## Touch Panel Control

The CPU-301-16 supports connectivity to an external touch panel controller using its SPI2 bus. In addition, Eurotech's standard BSP defines a processor GPIO signal as a touch panel controller interrupt. All signals are available on connector J1, page 46. The following diagram illustrates the touch panel control signals on the CPU-301-16.

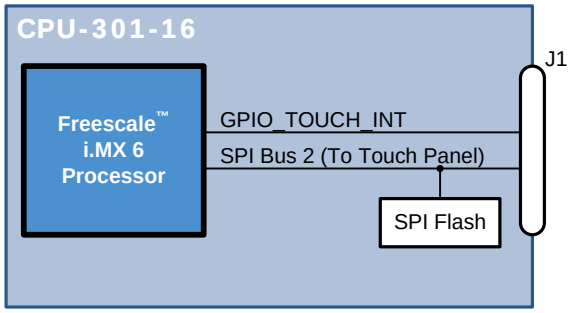



Figure 16. Touch Panel Connectivity

If your application does not require a touch panel, this SPI bus can be used for general-purpose.

The following table lists the touch panel control signals.

| Connector J1 | Signal Name | Type | Description |
|---|---|---|---|
| **A10** | EMI_LBA_SPI2_SS1 | O-3.3 | Chip select 1 (not used) |
| **A28** | SPI2_SS0 | O-3.3 | Chip select 0 |
| **A29** | SPI2_SCLK | O-3.3 | Serial clock |
| **A30** | SPI2_MISO | I-3.3 | Master input |
| **A32** | SPI2_MOSI | O-3.3 | Master output |
| **A53** | GPIO5_IO2/GPIO_TOUCH_INT | I-3.3 | Touch panel controller interrupt |

Table 16. Touch Panel Control Signals

## HDMI Display

As a digital replacement for older analog video standards, High-Definition Multimedia Interface (HDMI) vastly increases available bandwidth providing a sharper, richer quality output. The CPU-301-16 provides a HDMI 1.4 display port with transmitter port protection circuitry. This port is available on connector J2, page 49 for use with a carrier board and the microHDMI socket J4, page 53 for direct connection to a display in standalone use. The HDMI display port consists of three data pairs, as well as a clock, Consumer Electronics Control (CEC), and hot plug detect signals. For applications that require HDMI, the HDMI $I^2C$ bus (I2C2_SDA, I2C2_SCL) is dedicated to this port and supports the HDMI Display Data Channel (DDC) protocol. The following diagram illustrates the HDMI display connectivity on the CPU-301-16.

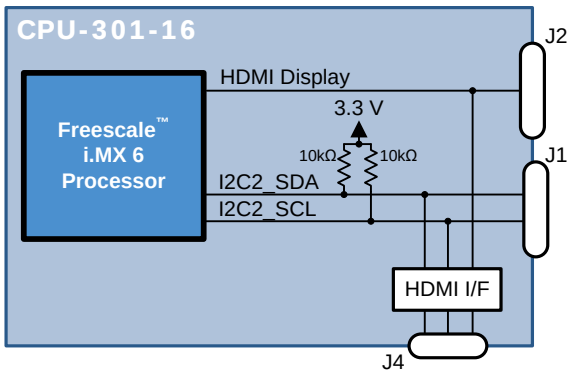



Figure 17. HDMI Display Connectivity

When connecting to an HDMI display through a carrier board, include ESD protection on all signals. A level shifter is also required on the carrier board for the single-ended control signals.

**Notes:**
HDMI.org licencing may apply.

If the HDMI functionality is not required in your application, the HDMI $I^2C$ bus can be used as a standard $I^2C$ bus. Notice that the board includes 10kΩ pull-up resistors to 3.3 V on the data and clock signals. Include ESD protection on your carrier board.

The following table lists the signals for the HDMI display.

| Connector J1 | Connector J2 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|---|
| **A18** | | I2C2_SDA | IO-3.3 | PU 10kΩ V3.3 | $I^2C$ data dedicated to HDMI |
| **A19** | | I2C2_SCL | O-3.3 | PU 10kΩ V3.3 | $I^2C$ clock dedicated to HDMI |
| | **A95** | HDMI_CEC | O-3.3 | | Consumer Electronics Control |
| | **A96** | HDMI_HPD | I-HDMI | PU 47kΩ 2.5V | Hot Plug Detect |
| | **A98** | HDMI_D2M | O-HDMI | | Data 2 negative |
| | **A99** | HDMI_D2P | O-HDMI | | Data 2 positive |
| | **A101** | HDMI_CLKP | O-HDMI | | Clock positive |
| | **A102** | HDMI_CLKM | O-HDMI | | Clock negative |
| | **A104** | HDMI_D0M | O-HDMI | | Data 0 negative |
| | **A105** | HDMI_D0P | O-HDMI | | Data 0 positive |
| | **A107** | HDMI_D1M | O-HDMI | | Data 1 negative |
| | **A108** | HDMI_D1P | O-HDMI | | Data 1 positive |

Table 17. HDMI Display Signals

## *MIPI Display Serial Interface*

The Mobile Industry Processor Interface (MIPI) Display Serial Interface (DSI) specification addresses the distinctive requirements of mobile devices by defining a protocol between the host processor and display in handheld devices. The host processor sends data and commands to the display and reads status from the display using a single pair of wires per lane. The MIPI display output, provided by the CPU-301-16, consists of two data lanes, as well as a clock pair. This output is available on connector J2, page 49. In addition, Eurotech's standard BSP defines two processor GPIO signals as reset and power enable outputs. The following diagram illustrates the MIPI DSI on the CPU-301-16.

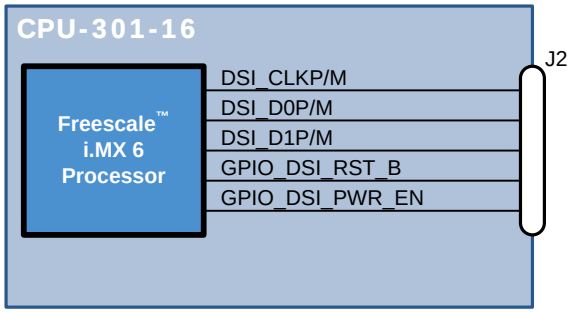



Figure 18. MIPI Display Serial Interface Connectivity

Notice that the MIPI DSI signals route directly from the processor. Include EMI suppression and ESD protection on your carrier board.

The following table lists the MIPI DSI signals.

| Connector J2 | Signal Name | Type | Description |
|---|---|---|---|
| **A32** | DSI_CLK0M | O-MIPI | Clock negative |
| **A33** | DSI_CLK0P | O-MIPI | Clock positive |
| **A35** | DSI_D0M | O-MIPI | Data 0 negative |
| **A36** | DSI_D0P | O-MIPI | Data 0 positive |
| **A38** | DSI_D1M | O-MIPI | Data 1 negative |
| **A39** | DSI_D1P | O-MIPI | Data 1 positive |
| **A42** | GPIO7_IO1/GPIO_DSI_RST_B | O-3.3 | Reset |
| **B30** | GPIO7_IO3/GPIO_DSI_PWR_EN | O-3.3 | Power enable |

Table 18. MIPI Display Serial Interface Signals

## *CMOS Camera*

To support input from a digital camera, the CPU-301-16 provides a parallel CMOS camera port on connector J2, page 49. This port includes 8-bit data, horizontal sync, vertical sync, pixel clock, and data enable signals. In addition, Eurotech's standard BSP defines two processor GPIO signals as reset and PWM outputs. These outputs are available on connector J1, page 46. The following diagram illustrates the CMOS camera connectivity on the CPU-301-16.

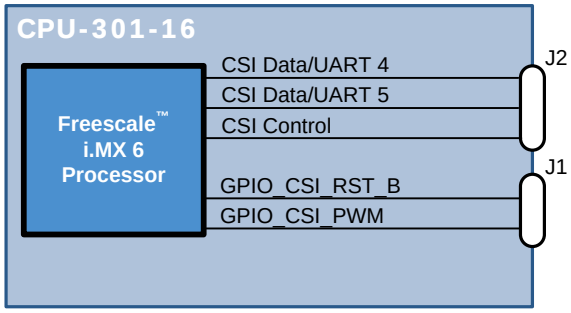



Figure 19. CMOS Camera Connectivity

Notice that the CMOS camera signals route directly to the processor. Include ESD protection on your carrier board.

The following table lists the CMOS camera signals.

| Connector J1 | Connector J2 | Signal Name | Type | Description |
|---|---|---|---|---|
| | **A12** | UART4_TXD_CSI_DAT12 | O-3.3 | Data 12 (UART 4 Transmit Data) |
| | **A13** | UART4_RXD_CSI_DAT13 | O-3.3 | Data 13 (UART 4 Receive Data) |
| | **A14** | UART5_TXD_CSI_DAT14 | O-3.3 | Data 14 (UART 5 Transmit Data) |
| | **A15** | UART5_RXD_CSI_DAT15 | O-3.3 | Data 15 (UART 5 Receive Data) |
| | **A16** | UART4_RTS_CSI_DAT16 | O-3.3 | Data 16 (UART 4 Request To Send) |
| | **A17** | UART4_CTS_CSI_DAT17 | O-3.3 | Data 17 (UART 4 Clear To Send) |
| | **A18** | UART5_RTS_CSI_DAT18 | O-3.3 | Data 18 (UART 5 Request To Send) |
| | **A19** | UART5_CTS_CSI_DAT19 | O-3.3 | Data 19 (UART 5 Clear To Send) |
| | **B12** | CSI_DATA_EN | O-3.3 | Data enable |
| | **B13** | CSI_HSYNC | O-3.3 | Horizontal sync |
| | **B14** | CSI_VSYNC | O-3.3 | Vertical sync |
| | **B15** | CSI_PIXCLK | O-3.3 | Pixel clock |
| **B32** | | CCM_CLKO | O | Clock source for audio and CMOS camera |
| **B54** | | GPIO5_IO12/GPIO_CSI_RST_B | O-3.3 | Reset |
| **B55** | | GPIO5_IO13/GPIO_CSI_PWM | O-3.3 | PWM |

Table 19. CMOS Camera Signals

**Notes:**
The CMOS camera port shares processor I/O pins with Serial ports 4 and 5. Therefore, these functions are mutually exclusive.

## MIPI Camera Serial Interface

The growing demand for higher image resolutions has been meet with design limitations on the older parallel interface between the host processor and camera. The Mobile Industry Processor Interface (MIPI) Camera Serial Interface (CSI) specification addresses these issues by providing a scalable, high-speed, low-power interface on a single pair of wires per lane. The CPU-301-16 includes a two lane MIPI CSI-2 on connector J2, page 49. The following diagram illustrates the MIPI CSI on the CPU-301-16.

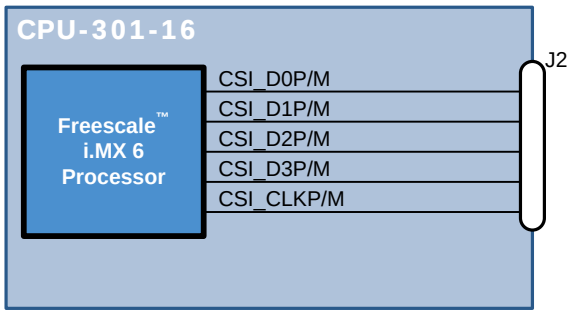



Figure 20. MIPI Camera Serial Interface Connectivity

Notice that the MIPI CSI signals route directly to the processor. Include EMI suppression and ESD protection on your carrier board. The following table lists the MIPI CSI signals.

| Connector J2 | Signal Name | Type | Description |
|---|---|---|---|
| **B81** | CSI_D0P | O-MIPI | Data 0 positive |
| **B82** | CSI_D0M | O-MIPI | Data 0 negative |
| **B84** | CSI_D1P | O-MIPI | Data 1 positive |
| **B85** | CSI_D1M | O-MIPI | Data 1 negative |
| **B87** | CSI_CLK0P | O-MIPI | Clock positive |
| **B88** | CSI_CLK0M | O-MIPI | Clock negative |
| **B91** | CSI_D2P | O-MIPI | Data 2 positive |
| **B92** | CSI_D2M | O-MIPI | Data 2 negative |
| **B94** | CSI_D3P | O-MIPI | Data 3 positive |
| **B95** | CSI_D3M | O-MIPI | Data 3 negative |

Table 20. MIPI CSI Signals

## Digital Audio

The digital audio interface enables connectivity between the CPU-301-16 and external peripherals such as audio and voice codecs. It supports a serial audio data format with rates up to 1.4 Mbps. This full-duplex synchronous interface includes transmit and receive channels with each channel providing data, bit clock, and sync signals. In addition, Eurotech's standard BSP defines two processor GPIO signals as a power enable output and headphone detect input to support an external audio codec. The digital audio interface is available on connector J1, page 46. The following diagram illustrates the digital audio interface on the CPU-301-16.

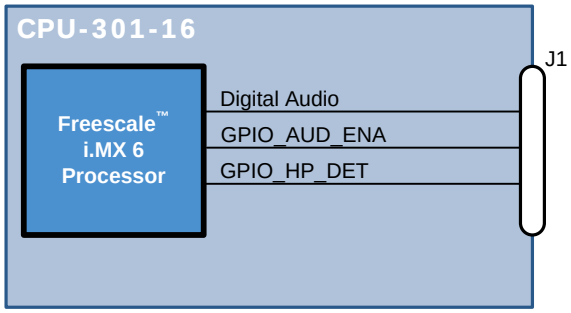



Figure 21. Digital Audio Connectivity

Include audio codecs along with amplifiers and switches on your carrier board.

The following table lists the digital audio signals.

| Connector J1 | Signal Name | Type | Description |
|---|---|---|---|
| **A12** | AUD_RXC | I-3.3 | ADC bit clock |
| **A13** | AUD_RXFS | I-3.3 | ADC sync |
| **A14** | AUD_RXD | I-3.3 | ADC data |
| **A15** | AUD_TXC | O-3.3 | DAC bit clock |
| **A16** | AUD_TFS | O-3.3 | DAC sync |
| **A17** | AUD_TXD | O-3.3 | DAC data |
| **B24** | GPIO1_IO4/GPIO_AUD_ENA | O-3.3 | External audio codec power enable |
| **B25** | GPIO4_IO1/GPIO_HP_DET | I-3.3 | Headphone detect input |
| **B32** | CCM_CLKO | O | Clock source for audio and CMOS camera |

Table 21. Digital Audio Signals

### *S/PDIF*

Developed jointly by the Sony and Phillips Corporations, S/PDIF is a digital audio interface commonly used in consumer audio equipment. The CPU-301-16 supports transmitter and receiver functionality and provides this interface on connector J2, page 49. The following diagram illustrates the S/PDIF connectivity on the CPU-301-16.

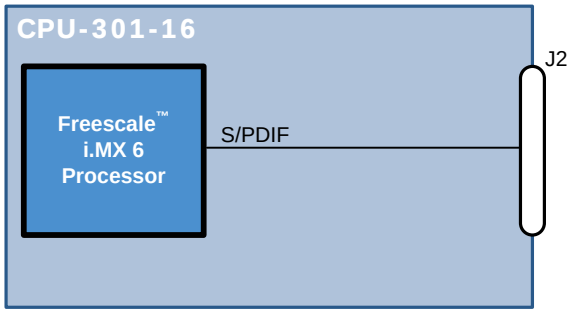



Figure 22. S/PDIF Connectivity

The following table lists the S/PDIF signals.

| Connector J2 | Signal Name | Type | Description |
|---|---|---|---|
| **A47** | SPDIF_IN | I-2.5 | Data in |
| **A48** | SPDIF_OUT | O-3.3 | Data out |
| **A49** | SPDIF_SRCLK | O-3.3 | Receive clock |
| **A50** | SPDIF_PLOCK | O-3.3 | Lock |
| **A52** | SPDIF_EXTCLK | O-2.5 | External clock |

Table 22. S/PDIF Signals

# Inputs and Output

Several signals on the CPU-301-16 support I/O expansion, system control, and general-purpose input and output. The following sections describe these discrete I/O.

### *User-defined Button and LEDS*

For use with a carrier board, Eurotech's standard BSP defines three processor GPIO signals as a user-defined button input and user-controlled LED outputs: GPIO6_IO3/GPIO_BUTTON (J1 B30), GPIO5_IO16/GPIO_LED_RED (J1 B58), and GPIO7_IO2/GPIO_LED_GRN (J1 B59). These GPIO can be used to drive high impedance loads only. Do not drive LEDs directly with these signals.

## Keypad/GPIO

The CPU-301-16 provides sixteen signals that can be used to support an 8x8 keypad or as general-purpose inputs and outputs (GPIO). These keypad/GPIO signals are available on connector J1, page 46, as shown in the following diagram.

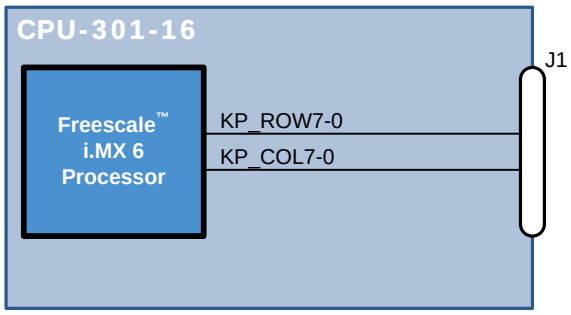



Figure 23. Keypad/GPIO Connectivity

Notice that the keypad/GPIO signals route directly from the processor. Include series termination and ESD protection on your carrier board. The following table describes these signals.

| Connector J1 | Signal Name | Type | Description |
|---|---|---|---|
| **A33** | KP_COL0 | IO-3.3 | Column 0 |
| **A34** | KP_COL1 | IO-3.3 | Column 1 |
| **A35** | KP_COL2 | IO-3.3 | Column 2 |
| **A36** | KP_COL3 | IO-3.3 | Column 3 |
| **A37** | KP_COL4 | IO-3.3 | Column 4 |
| **A38** | KP_COL5 | IO-3.3 | Column 5 |
| **A39** | KP_COL6 | IO-3.3 | Column 6 |
| **A40** | KP_COL7 | IO-3.3 | Column 7 |
| **B33** | KP_ROW0 | IO-3.3 | Row 0 |
| **B34** | KP_ROW1 | IO-3.3 | Row 1 |
| **B35** | KP_ROW2 | IO-3.3 | Row 2 |
| **B36** | KP_ROW3 | IO-3.3 | Row 3 |
| **B37** | KP_ROW4 | IO-3.3 | Row 4 |
| **B38** | KP_ROW5 | IO-3.3 | Row 5 |
| **B39** | KP_ROW6 | IO-3.3 | Row 6 |
| **B40** | KP_ROW7 | IO-3.3 | Row 7 |

Table 23. Keypad/GPIO Signals

## General User I/O

The CPU-301-16 provides five signals that are defined as general user inputs and outputs (GPIO) with interrupt capabilities. These GPIO are available on connector J1, page 46 for use with a carrier board and on connector J11, page 54 for standalone use. The following diagram illustrates the connectivity of these GPIO on the CPU-301-16.

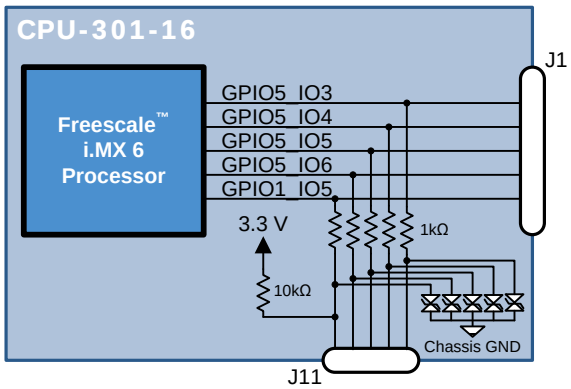



Figure 24. General User I/O Connectivity

Notice that the GPIO signals include series termination and ESD protection on connector J11 for standalone use. When using a carrier board, do not rely on the ESD protection circuit on the CPU-301-16. Include series termination and ESD protection at the source on your carrier board for the signals on connector J1.

The following table lists the GPIO for connector J1. For the pinout of connector J11, see connector J11, page 54.

| Connector J1 | Signal Name | Type | Description |
|---|---|---|---|
| **A54** | GPIO5_IO3 | IO-3.3 | General user I/O |
| **A55** | GPIO5_IO4 | IO-3.3 | General user I/O |
| **A56** | GPIO5_IO5 | IO-3.3 | General user I/O |
| **A57** | GPIO5_IO6 | IO-3.3 | General user I/O |
| **B85** | GPIO1_IO5/SLEEP_EVENT | IO-3.3 | General user I/O<br>(See Power Management Signals, page 36.) |

Table 24. General User I/O

**Notes:**
In addition to the general user inputs and outputs, there are twenty-eight GPIO that are used by Eurotech's standard Board Support Package (BSP) to support a pre-defined set of commonly used interfaces. These interfaces are implemented on the standard Eurotech carrier board. The sections in this document describe how each GPIO is defined based on this standard BSP. These GPIO can be configured differently for your specific end-use based on your custom BSP.

## *Accelerometer*

Eurotech's standard BSP defines two processor GPIO signals as programmable interrupts from an external accelerometer to the processor: GPIO6_IO1/GPIO_ACCEL_INT1 (J1 B28) and GPIO6_IO2/GPIO_ACCEL_INT2 (J1 B29).

## *Tamper*

The output signal TAMPER (J1 B83) is an indicator for enclosure tampering.

## *Watchdog Timeout*

The output signal WDOG_TIMEOUT (J1 B89) is activated when the processor's internal watchdog timer expires. Contact Eurotech for availability of this function.

## *Real-Time Clock*

The CPU-301-16 includes a secure Real-Time Clock (RTC) function that retains the system date and time when power is provided to the board. If your application requires this feature, include a long-life, lithium coin battery on your carrier board to supply backup power to the CPU-301-16.

# Power Supply

Power management is especially critical in today's handheld and portable systems. Applications are not only demanding higher performance but also requiring lower power dissipation. To meet these on-going requirements, the CPU-301-16 combines the integrated power management of the i.MX 6 series processor with an on-board Power Management Integrated Circuit (PMIC). This section provides information about power and power management on the CPU-301-16.

Embedded system designers using the CPU-301-16 should have a clear understanding of how the system design allocates power usage. Create a power budget that takes into account the types of devices that are used with the CPU-301-16.

## *Power Supply Architecture*

The following diagram illustrates the power supply architecture of the CPU-301-16. For power specifications, see Power Supply, page 55.

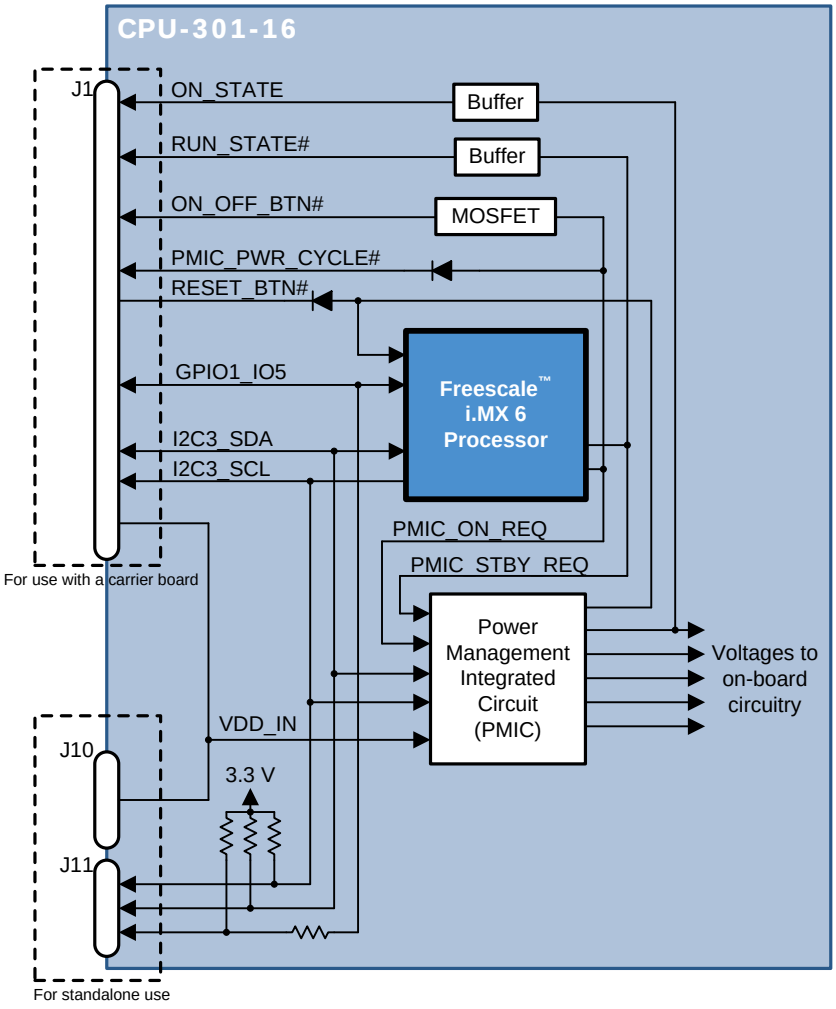



Figure 25. Power Supply Architecture

The CPU-301-16 receives input power from header J10 (for standalone use) or connector J1 (for use with a carrier board). An on-board PMIC generates all voltages required by the on-board circuitry. It is the responsibility of the designers to provide input power protection as required by their application. This is especially important if the power supply wires will be subject to EMI/RFI or ESD. In addition, VDD_IN should be a power plane on your carrier board. Be sure to include sufficient bulk decoupling and local decoupling.

## Power Management Signals

In addition to the input power, connector J1, page 46 includes six power management signals that can be used for proper reset, power synchronization, and power control on a carrier board. These signals are described in the following table.

| Signal | J1 Pin | Type | Description |
|---|---|---|---|
| **ON_STATE** | B87 | Output | When asserted high, output indicates all on-board power supplies have been enabled. Use this output to turn on power for peripheral devices on the carrier board. |
| **RUN_STATE#** | B86 | Output | Transitions low when the processor requests sleep mode and remains low until the processor issues a wake request. |
| **PMIC_PWR_CYCLE#** | B49 | Input | Pull this input low to force the CPU-301-16 into a Power Reset sequence. Include a pull-up resistor on the carrier board. |
| **ON_OFF_BTN#** | B88 | Input | When the CPU-301-16 is turned off by software, pull this input low to turn on the CPU-301-16 without requiring a power cycle.<br><br>As an option for Android-like systems, the input can be used as an on/off button. This option requires customization. Contact your local Eurotech representative for additional information. |
| **RESET_BTN#** | B84 | Input | Pull this input low to force the CPU-301-16 to reset without going through a Power Reset sequence. Include a pull-up resistor on the carrier board. |
| **GPIO1_IO5/SLEEP_EVENT** | B85 | Input | This signal is defined in the standard BSP as an external sleep/wake control. |

Table 25. Power Control and Reset Signals

The output signals are not buffered on the CPU-301-16; therefore, include additional buffering on the carrier board to drive multiple loads. For electrical specifications, see Power Supply, page 55.

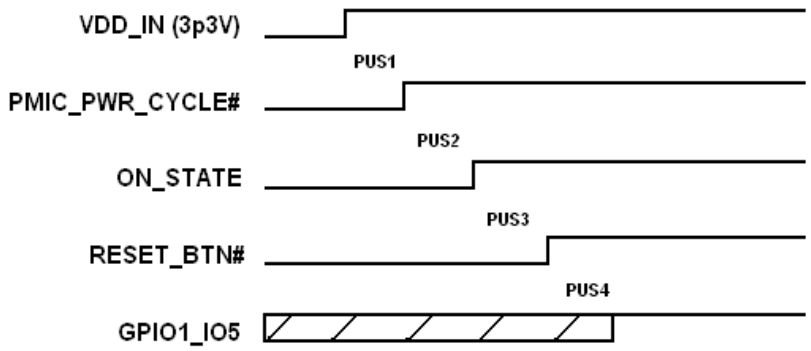
## Power Sequences

This section describes the relationship of the power management signals on the CPU-301-16.

**Notes:**
Implement the exact power supply sequencing as described in this section. The CPU-301-16 has very specific power-on sequence requirements in order to power-up and operate correctly. Power sequencing is CRITICAL for correct operation of the CPU-301-16.

### Power-on

The following diagram shows the default power-on sequence. The CPU-301-16 boots when VDD_IN is applied. The carrier board should turn on power for peripheral devices after ON_STATE is asserted high to avoid back power.

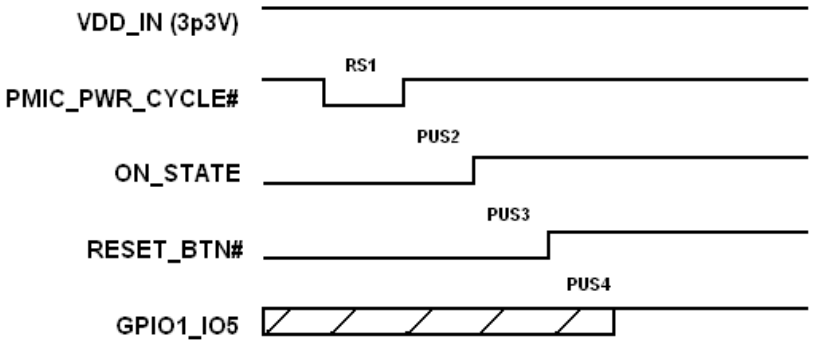



Notes:
4. Timing for PUS1, PUS2, PUS3, and PUS4 is to be determined.

Figure 26. Power-on Sequence

### Power Reset

The following diagram shows the power reset sequence. Pulling PMIC_PWR_CYCLE# low at any time, forces the PMIC to reinitialize the power for the CPU-301-16 including the processor.




Notes:

5. Timing for RS1, PUS2, PUS3, and PUS4 is to be determined.

Figure 27. Power Reset Sequence

### Entering Sleep Mode

The following diagram shows the CPU-301-16 entering sleep mode. Pulling GPIO1_IO5 low, forces the processor to request that the PMIC enter sleep mode by asserting RUN_STATE# high. The PMIC reconfigures the power rails for sleep and de-asserts ON_STATE. To conserve power further, turn off power for peripheral devices on the carrier board when ON_STATE is de-asserted low.


Notes:

6. Timing for ESS1 and ESS2 is to be determined.

Figure 28. Entering Sleep Mode Sequence

### Exiting Sleep Mode

The following diagram shows the CPU-301-16 exiting sleep mode. Pulling GPIO1_IO5 high, forces the processor to request that the PMIC exit sleep mode by asserting RUN_STATE# low. The PMIC reconfigures the power rails for operation and asserts ON_STATE high. Turn on power for peripheral devices on the carrier board when ON_STATE is asserted.


Notes:

7. Timing for WS1 and WS2 is to be determined.

Figure 29. Exiting Sleep Mode Sequence

# Boot Mode Configuration

The i.MX 6 series of processors provide a flexible method for selecting the boot mode and boot device. This section provides details about how this capability is implemented on the CPU-301-16.

## *Boot Mode Signals*

The i.MX 6 series of processors provide for three boot mode options. At power-up, the processor samples the signals BOOT_MODE0 (J1 B81) and BOOT_MODE1 (J1 B82) to determine which option is selected. The following table describes the boot mode options.

| BOOT_MODE[1:0] (note 8) | Jumper Setting (note 9) J7 | J8 | Boot Type | Comments |
|---|---|---|---|---|
| **00** | NC | 1-2 | Boot From Fuses | Contact Eurotech if your application requires this option. |
| **01** | NC | NC | Serial Downloader | Default setting for factory testing |
| **10** | 1-2 | 1-2 | Internal Boot | Recommended setting |
| **11** | 1-2 | NC | Reserved | |

Notes:

8. Signals include on-board pull-up/pull-down resistors. Do not include any termination on your carrier board.
9. Two on-board jumpers are used to set BOOT_MODE[1:0]. NC indicates that the jumper is not installed, while 1-2 indicates that the jumper is installed.

Table 26. Boot Mode Options

For factory testing, the default setting on the CPU-301-16 is Serial Downloader. This option uses a FreeScale tool to load software to a selected boot device through the USB OTG port. For your application, Eurotech recommends that you use the Internal Boot setting and include circuitry on your carrier board to select your boot device as described in the following section.

## *Boot Configuration Signals*

For the Internal Boot mode previously described, you can select a specific boot device using the processor's BOOT_CFG signals. These signals are special I/O that serve a dual-function. At power-up, these signals determine the boot device of the CPU-301-16. After boot, these signals assume the alternate function specified by the BSP. Use care on your carrier board to ensure that these signals are not driven high or pulled low by the device associated with the alternate function during power up or rest.

The following table lists the boot configuration signals.

| Boot Configuration Signal Name | Eurotech's BSP Signal Name | J1 Pin | Note |
|---|---|---|---|
| **BOOT_CFG1_0** | DISP_DAT9 | A77 | |
| **BOOT_CFG1_1** | DISP_DAT8 | A78 | |
| **BOOT_CFG1_2** | DISP_DAT7 | A79 | |
| **BOOT_CFG1_3** | DISP_DAT6 | A81 | |
| **BOOT_CFG1_4** | DISP_DAT5 | A82 | |
| **BOOT_CFG1_5** | DISP_DAT4 | A83 | |
| **BOOT_CFG1_6** | DISP_DAT3 | A84 | |
| **BOOT_CFG1_7** | DISP_DAT2 | A85 | |
| **BOOT_CFG2_0** | DISP_DAT1 | A86 | |
| **BOOT_CFG2_1** | DISP_DAT0 | A87 | |
| **BOOT_CFG2_2** | DISP_DRDY | A89 | |
| **BOOT_CFG2_3** | DISP_HSYNC | A88 | |
| **BOOT_CFG2_4** | DISP_VSYNC | A91 | |
| **BOOT_CFG2_5** | GPIO_PANEL_ENABLE | A59 | |
| **BOOT_CFG2_6** | GPIO_SER_B_RS232 | B18 | |
| **BOOT_CFG2_7** | GPIO_SER_C_RS232 | B19 | |
| **BOOT_CFG3_2** | DISP_DAT13 | A73 | System CLK configuration pin |
| **BOOT_CFG3_3** | DISP_DAT14 | A72 | |

| Boot Configuration Signal Name | Eurotech's BSP Signal Name | J1 Pin | Note |
|---|---|---|---|
| **BOOT_CFG3_4** | DISP_DAT15 | A71 | System DDR configuration pin |
| **BOOT_CFG3_5** | DISP_DAT16 | A69 | System DDR configuration pin |
| **BOOT_CFG3_6** | DISP_DAT17 | A68 | System test Configuration pin |
| **BOOT_CFG3_7** | DISP_DAT18 | A67 | |
| **BOOT_CFG4_7** | UART1_RI | A9 | |

Table 27. Boot Configuration Signals

Include circuitry on your carrier board to configure these signals. The following diagrams give example circuitry that can be used on you carrier board.

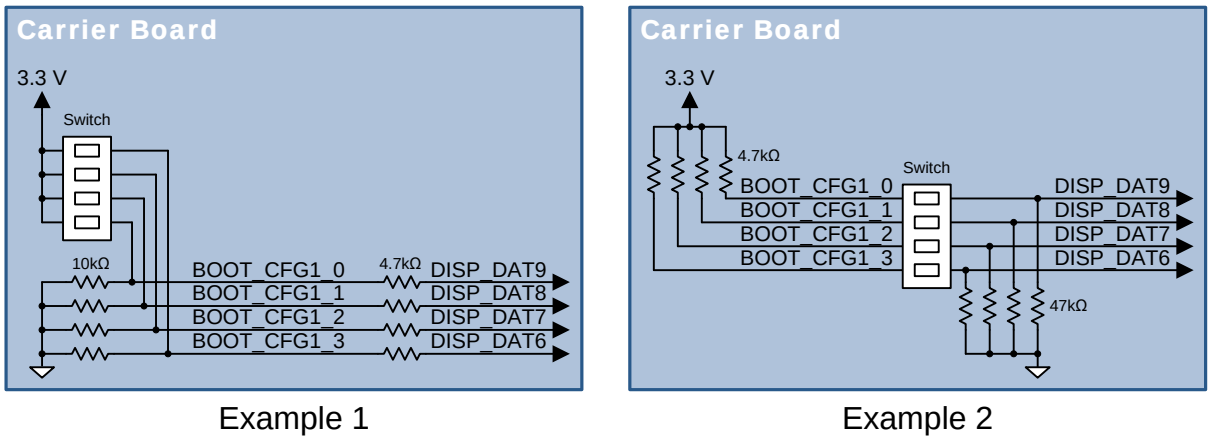



Figure 30. Example Boot Configuration Circuitry

The boot device is determined by the configuration of the BOOT_CFG signals as described in the tables in the following section.

## *Boot Devices*

Based on the setting of the BOOT_CFG signals, the CPU-301-16 has the capability to boot and install the operating system from the following sources:

- SD card on SD 2
- SD card on SD 4
- eMMC flash memory device on SD 4
- RAW NAND flash memory device
- SATA drive on carrier board

The following tables describe the BOOT_CFG settings for each option. In the table, a “0”, indicates a low logic-level, a “1” indicates a high logic-level, and a “x” indicates a “don’t care”.

### SATA Drive

| Boot Configuration Signal Name | SSD/Hard Drive | TX Spread Spectrum | | RX Spread Spectrum | | SATA Speed | | SATA Type | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | No | Yes | No | Yes | Gen2 (3.0Gbps) | Gen1 (1.5Gbps) | i | m | x | Reserved |
| **BOOT_CFG1_4** | 0 | | | | | | | | | | |
| **BOOT_CFG1_5** | 1 | | | | | | | | | | |
| **BOOT_CFG1_6** | 0 | | | | | | | | | | |
| **BOOT_CFG1_7** | 0 | | | | | | | | | | |
| **BOOT_CFG2_0** | | | | | | | | 0 | 1 | 0 | 1 |
| **BOOT_CFG2_1** | | | | | | | | 0 | 0 | 1 | 1 |
| **BOOT_CFG2_2** | | | | | | 0 | 1 | | | | |
| **BOOT_CFG2_3** | | | | 0 | 1 | | | | | | |
| **BOOT_CFG2_4** | | 0 | 1 | | | | | | | | |

Table 28. Boot Configuration Settings for SATA Drive

### SD Card

| Boot Configuration Signal Name | SD/eSD/SDXC | Boot Mode | | Speed | | | PWR Cycle through SD_RST (SD3) | | From Pad CLK Loopback | Bit | | 1 Calibration Step Delay | Slot | | Default - Pull-up/down when PWR Cycle Enable | Default - Pad Setting (Manufacture Setting) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Normal (25M) | Fast (50M) | Normal (25M) | SDR50 (100M) | SDR104 (200M) | No | Yes | | 1 | 4 | | 2 | 4 | | |
| **BOOT_CFG1_0** | | | | | | | | | 0 | | | | | | | |
| **BOOT_CFG1_1** | | | | | | | 0 | 1 | | | | | | | | |
| **BOOT_CFG1_2** | | | | x | 0 | 1 | | | | | | | | | | |
| **BOOT_CFG1_3** | | | | 0 | 1 | 1 | | | | | | | | | | |
| **BOOT_CFG1_4** | x | 0 | 1 | | | | | | | | | | | | | |
| **BOOT_CFG1_5** | 0 | | | | | | | | | | | | | | | |
| **BOOT_CFG1_6** | 1 | | | | | | | | | | | | | | | |
| **BOOT_CFG1_7** | 0 | | | | | | | | | | | | | | | |
| **BOOT_CFG2_0** | | | | | | | | | | | | | | | | 0 |
| **BOOT_CFG2_1** | | | | | | | | | | | | | | | 0 | |
| **BOOT_CFG2_3** | | | | | | | | | | | | | 1 | 1 | | |
| **BOOT_CFG2_4** | | | | | | | | | | | | | 0 | 1 | | |
| **BOOT_CFG2_5** | | | | | | | | | | 0 | 1 | | | | | |
| **BOOT_CFG2_6** | | | | | | | | | | | | 0 | | | | |
| **BOOT_CFG2_7** | | | | | | | | | | | | 0 | | | | |

Table 29. Boot Configuration Settings for SD Card

### eMMC Flash Memory Device

| Boot Configuration Signal Name | MMC/eMMC | Boot Mode: Normal | Boot Mode: Fast | Boot Speed: High | Boot Speed: Normal | PWR Cycle through SD_RST (SD3 and SD4 only): No | PWR Cycle through SD_RST (SD3 and SD4 only): Yes | 8 Bit | 4 Slot | Boot ROM Default - DII Override | Enabled - Boot Acknowledge | Default - Pad Setting (Manufacture Setting) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **BOOT_CFG1_1** | | | | | | 0 | 1 | | | | | |
| **BOOT_CFG1_2** | | | | x | x | | | | | | | |
| **BOOT_CFG1_3** | | | | 0 | 1 | | | | | | | |
| **BOOT_CFG1_4** | x | 0 | 1 | | | | | | | | | |
| **BOOT_CFG1_5** | 1 | | | | | | | | | | | |
| **BOOT_CFG1_6** | 1 | | | | | | | | | | | |
| **BOOT_CFG1_7** | 0 | | | | | | | | | | | |
| **BOOT_CFG2_0** | | | | | | | | | | | | 0 |
| **BOOT_CFG2_1** | | | | | | | | | | | 0 | |
| **BOOT_CFG2_2** | | | | | | | | | | 0 | | |
| **BOOT_CFG2_3** | | | | | | | | | 1 | | | |
| **BOOT_CFG2_4** | | | | | | | | | 1 | | | |
| **BOOT_CFG2_5** | | | | | | | | 0 | | | | |
| **BOOT_CFG2_6** | | | | | | | | 1 | | | | |
| **BOOT_CFG2_7** | | | | | | | | 0 | | | | |

Table 30. Boot Configuration Settings for eMMC Flash Memory Device

### RAW NAND Flash Memory Device

| Boot Configuration Signal Name | NAND | Raw NAND - BT Toggle Mode | Default - Override Pad Setting | 1 - Number of Devices | 3 - Address Cycle | 16 - Toggle Mode 33MHz Preamble Delay, Read Latency (unit = GPMICLK Cycles) | 2 - Boot Search Count | Pages in Block: 128 | Pages in Block: 64 | Pages in Block: 32 | Pages in Block: 256 | 12 - Reset Time (ms) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **BOOT_CFG1_0** | | | | | 0 | | | | | | | |
| **BOOT_CFG1_1** | | | | | 0 | | | | | | | |
| **BOOT_CFG1_2** | | | | 0 | | | | | | | | |
| **BOOT_CFG1_3** | | | | 0 | | | | | | | | |
| **BOOT_CFG1_4** | x | | 0 | | | | | | | | | |
| **BOOT_CFG1_5** | x | 0 | | | | | | | | | | |
| **BOOT_CFG1_6** | x | | | | | | | | | | | |
| **BOOT_CFG1_7** | 1 | | | | | | | | | | | |
| **BOOT_CFG2_0** | | | | | | | | | | | | 0 |
| **BOOT_CFG2_1** | | | | | | | | 0 | 1 | 0 | 1 | |
| **BOOT_CFG2_2** | | | | | | | | 0 | 0 | 1 | 1 | |
| **BOOT_CFG2_3** | | | | | | | 0 | | | | | |
| **BOOT_CFG2_4** | | | | | | | 0 | | | | | |
| **BOOT_CFG2_5** | | | | | | 0 | | | | | | |
| **BOOT_CFG2_6** | | | | | | 0 | | | | | | |
| **BOOT_CFG2_7** | | | | | | 0 | | | | | | |

Table 31. Boot Configuration Settings for RAW NAND Flash Memory Device

# Mechanical Specifications

This section describes mechanical and thermal design guidelines for the CPU-301-16.

## Mechanical Design

### *Mechanical Drawing*

The following mechanical drawings specify the dimensions of the CPU-301-16, as well as locations of key components on the board. All dimensions are in millimeters.

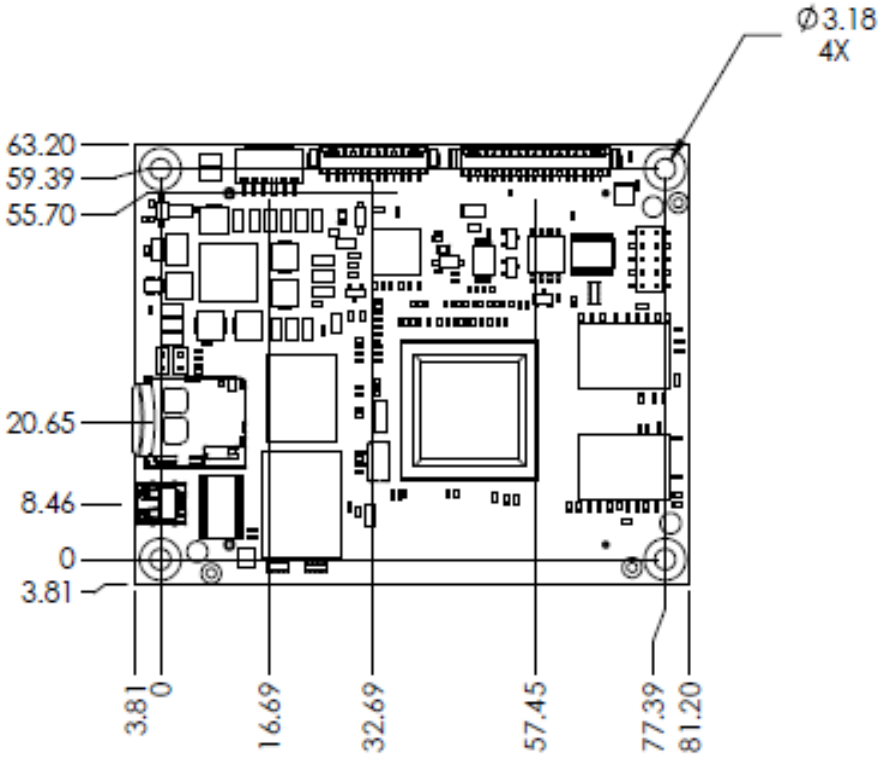



Figure 31. CPU-301-16, Top View

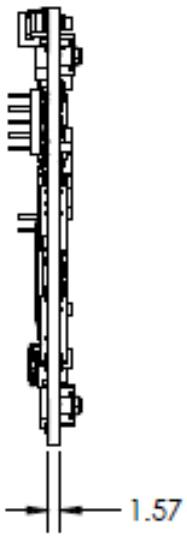



Figure 32. CPU-301-16, Side View

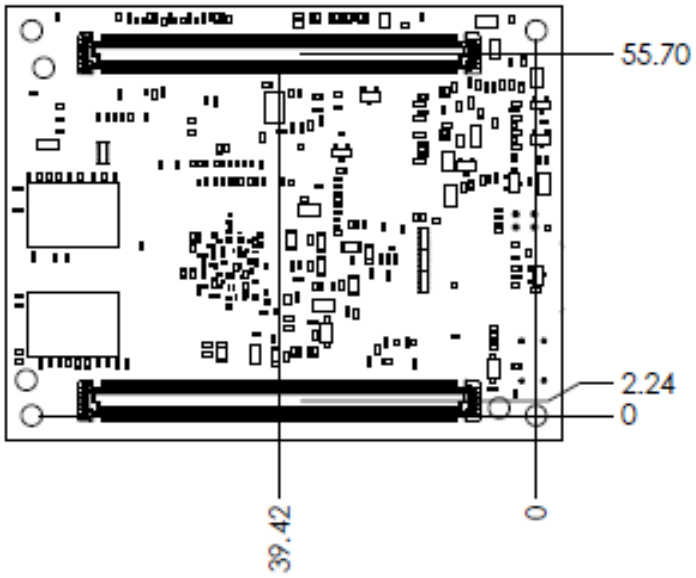
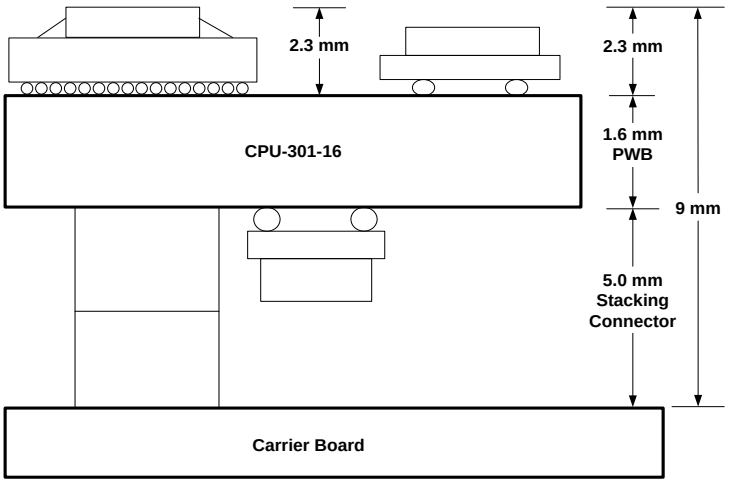



Figure 33. CPU-301-16, Bottom View

## *Total Stack Height*

Selection of low profile stacking connectors and components minimizes the total stack height of the CPU-301-16 and carrier board. The CPU-301-16 uses stacking board-to-board connectors to mate with a carrier board. The mating connectors on the carrier board can be either 5 mm or 8 mm stacking height. When 5 mm stacking board-to-board connectors are used, the total board height combined with the connector clearance results in a total stack height of 9 mm. You may place components under the CPU-301-16 on a custom carrier board. However, the design must allow adequate heat dissipation.

The following diagram illustrates the total stack height using 5 mm stacking connectors on the carrier board.




Notes:

10. Total stack height is specified for use with a carrier board with standalone-use connectors (J3, J4, J6, J7, J8, J9, J10, and J11) depopulated.

Figure 34. Total Stack Height

### *Mounting*

Four holes located at each corner enable mounting on the carrier board. The ground plane connects electrically to three of the four the mounting holes through 0Ω resistors. Mounting hole 4 is not connected to the ground plane. For the location of the mounting holes, see Identifying Connectors, page 45.

Per IPC-A-610D section 4.2.3, secure the board to standoffs using a flat washer against the board with a split washer on top between the flat washer and the screw head or nut. Do not use toothed star washers, as they cut into the plating and laminations of the board over time and will not produce an attachment that will withstand vibration and thermal cycling.

### *Insertion and Removal*

The CPU-301-16 connects to the carrier board through two high-density, stacking board-to-board connectors. When fully connected, these fine pitch connectors provide reliable and durable connection. However, care is required when removing or installing the module onto the carrier board. Observe industry-standard electronic handling procedures when handling the CPU-301-16. Eurotech recommends using a grounded wrist strap and heel strap. The connectors expose signals on the system bus that do not have ESD protection.

## Thermal Management

In some applications such as high ambient temperature or extended multicore activity, the CPU-301-16 may require convective cooling or heat spreading to dissipate the heat generated by the i.MX 6 processor. Contact your local Eurotech representative to discuss your thermal management requirements.

## Test and Debug

### *Debug Serial Port*

One of the serial ports can be configured as a debug port which is useful for debugging. Eurotech recommends reserving a serial port for this purpose. In case all serial ports are used, you can share the debug port with a low priority port such that the port can be configured for its intended use after debug is complete.

### *JTAG Port*

The JTAG port, provided on connector J1 and J6, is available for factory test and software debugging. Otherwise, this port is not supported for application use. Eurotech highly recommends allowing access to header J6 in your system or including an external connection to this JTAG port on your carrier board.

The following table lists the JTAG signals for connector J1. For the pinout of connector J6, see connector J6, page 53.

| Connector J1 | Signal Name | Type | On-board Termination | Description |
|---|---|---|---|---|
| **A22** | JTAG_TRST# | I-3.3 | PU 10kΩ V3.3 | Test Reset |
| **A23** | JTAG_RST# | I-SNVS | PU 10kΩ V3.3 | Reset |
| **A24** | JTAG_TMS | I-3.3 | PU 10kΩ V3.3 | Test Mode Select |
| **A25** | JTAG_TDI | I-3.3 | PU 10kΩ V3.3 | Test Data In |
| **A26** | JTAG_TDO | O-3.3 | | Test Data Out |
| **A27** | JTAG_TCK | I-3.3 | PU 10kΩ V3.3 | Test Clock |

Table 32. JTAG Signals

To ensure correct operation of the JTAG interface, include a 10kΩ pull-up resistor to 3.3 V on the TDO signal on the carrier board.

# Connectors

## Identifying Connectors

The following diagrams illustrate the location and numbering of the connectors on the CPU-301-16. When viewing the board from the component side, connector J1 and connector J2 lie under the board.

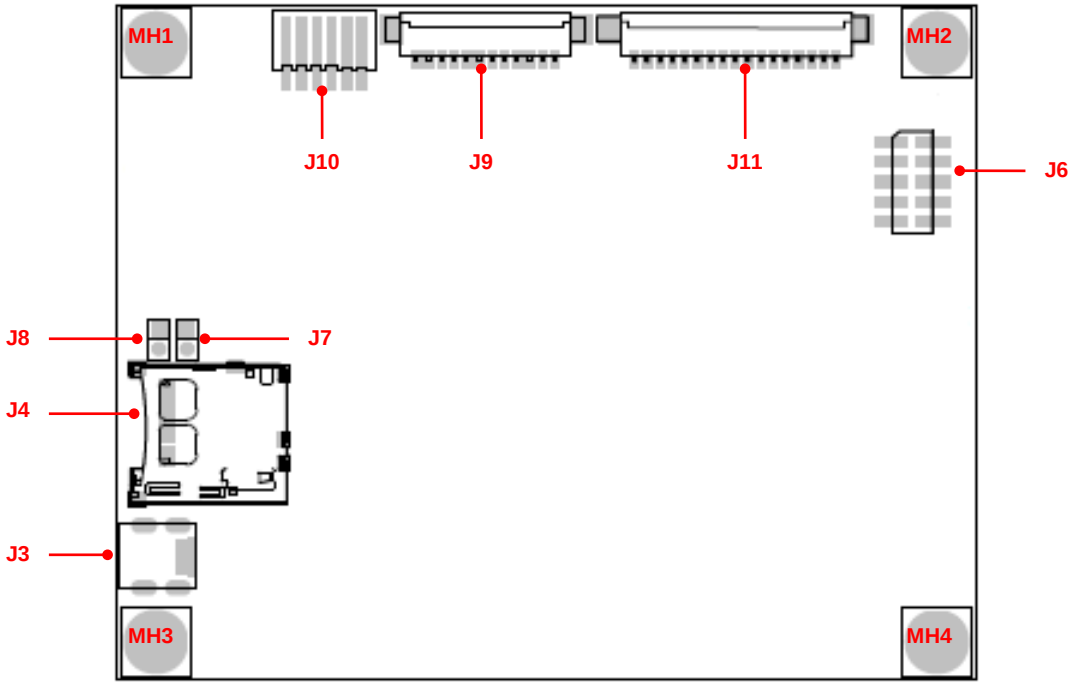



Figure 35. Connector Location, Top View

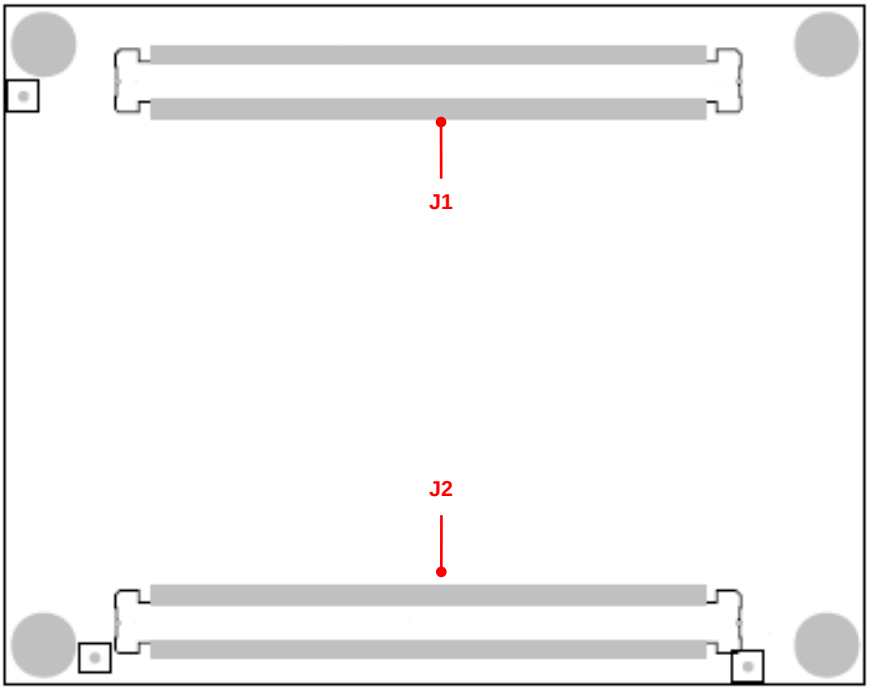



Figure 36. Connector Location, Bottom View

# Signal Headers

The following tables describe the electrical signals available on the connectors of the CPU-301-16. Each section provides relevant details about the connector including part numbers, mating connectors, and connector pinout. The pinout table includes signal type and a signal description. For electrical specifications, see System Specifications, page 55.

**Note:**
In addition to being available on the docking connectors, the following signals are provided on the on-board connectors (J3, J4, J9, J10, and J11) for use when the CPU-301-16 is used in standalone mode:

- Power
- SD
- HDMI Display
- Ethernet
- USB OTG
- Serial 2
- General-purpose $I^2C$ bus
- GPIO

For details, see the pinout tables in this section.

## *J1: Docking Connector: Serial, Audio, $I^2C$ Buses, SD, JTAG, SPI, Keypad, USB Host, USB OTG, CAN, GPIO, LVDS Display, Digital Display, PWM, Control, Gigabit Ethernet, and Power*

Board connector: 220-pin, stacking board-to-board receptacle, 0.5 mm, Tyco Electronics 3-6318490-6
Carrier board connector: Tyco Electronics 3-1827253-6, 5 mm stacking height
Tyco Electronics 3-6318491-6, 8 mm stacking height

Connector J1 mates to the carrier board. Input power and data signals are provided on this docking connector.

| Pin | Name | Type | Description |
|---|---|---|---|
| **A1** | GND | P | Ground |
| **A2** | UART1_DCD | I-3.3 | Serial 1, Data Carrier Detect |
| **A3** | UART1_DSR | I-3.3 | Serial 1, Data Set Ready |
| **A4** | UART1_RXD | I-3.3 | Serial 1, Receive Data |
| **A5** | UART1_RTS | O-3.3 | Serial 1, Request To Send |
| **A6** | UART1_TXD | O-3.3 | Serial 1, Transmit Data |
| **A7** | UART1_CTS | I-3.3 | Serial 1, Clear To Send |
| **A8** | UART1_DTR | O-3.3 | Serial 1, Data Terminal Ready |
| **A9** | UART1_RI | I-3.3 | Serial 1, Ring Indicator |
| **A10** | EIM_LBA_SPI2_SS1 | O-3.3 | |
| **A11** | GND | P | Ground |
| **A12** | AUD_RXC | I-3.3 | Digital audio, ADC bit clock |
| **A13** | AUD_RXFS | I-3.3 | Digital audio, ADC sync |
| **A14** | AUD_RXD | I-3.3 | Digital audio, ADC data |
| **A15** | AUD_TXC | O-3.3 | Digital audio, DAC bit clock |
| **A16** | AUD_TFS | O-3.3 | Digital audio, DAC sync |
| **A17** | AUD_TXD | O-3.3 | Digital audio, DAC data |
| **A18** | I2C2_SDA | IO-3.3 | $I^2C$ data dedicated to HDMI |
| **A19** | I2C2_SCL | O-3.3 | $I^2C$ clock dedicated to HDMI |
| **A20** | NC | | |
| **A21** | GND | P | Ground |
| **A22** | JTAG_TRST# | I-3.3 | JTAG, Test Reset |
| **A23** | JTAG_RST# | I-SNVS | JTAG, Reset |
| **A24** | JTAG_TMS | I-3.3 | JTAG, Test Mode Select |
| **A25** | JTAG_TDI | I-3.3 | JTAG, Test Data In |
| **A26** | JTAG_TDO | O-3.3 | JTAG, Test Data Out |
| **A27** | JTAG_TCK | I-3.3 | JTAG, Test Clock |
| **A28** | SPI2_SS0 | O-3.3 | SPI 2, Chip select 0 |
| **A29** | SPI2_SCLK | O-3.3 | SPI 2, Serial clock |
| **A30** | SPI2_MISO | I-3.3 | SPI 2, Master input |
| **A31** | GND | P | Ground |
| **A32** | SPI2_MOSI | O-3.3 | SPI 2, Master output |

| Pin | Name | Type | Description |
|---|---|---|---|
| **A33** | KP_COL0 | IO-3.3 | Keypad, Column 0 |
| **A34** | KP_COL1 | IO-3.3 | Keypad, Column 1 |
| **A35** | KP_COL2 | IO-3.3 | Keypad, Column 2 |
| **A36** | KP_COL3 | IO-3.3 | Keypad, Column 3 |
| **A37** | KP_COL4 | IO-3.3 | Keypad, Column 4 |
| **A38** | KP_COL5 | IO-3.3 | Keypad, Column 5 |
| **A39** | KP_COL6 | IO-3.3 | Keypad, Column 6 |
| **A40** | KP_COL7 | IO-3.3 | Keypad, Column 7 |
| **A41** | GND | P | Ground |
| **A42** | USB_HOST_DN | IO-USB | USB host, Data negative |
| **A43** | USB_HOST_DP | IO-USB | USB host, Data positive |
| **A44** | GND | P | Ground |
| **A45** | USB_H_OC# | I-3.3 | USB host, Over current |
| **A46** | USB_H_PWR_EN | O-3.3 | USB host, Power enable |
| **A47** | TX_CAN1 | O-3.3 | CAN Bus 1 |
| **A48** | RX_CAN1 | I-3.3 | CAN Bus 1 |
| **A49** | TX_CAN2 | O-3.3 | CAN Bus 2 |
| **A50** | RX_CAN2 | I-3.3 | CAN Bus 2 |
| **A51** | GND | P | Ground |
| **A52** | GPIO5_IO1/GPIO_nUSB_RST | IO-3.3 | External USB Hub reset |
| **A53** | GPIO5_IO2/GPIO_TOUCH_INT | IO-3.3 | Touch panel controller interrupt |
| **A54** | GPIO5_IO3 | IO-3.3 | See General User I/O, page 33. |
| **A55** | GPIO5_IO4 | IO-3.3 | See General User I/O, page 33. |
| **A56** | GPIO5_IO5 | IO-3.3 | See General User I/O, page 33. |
| **A57** | GPIO5_IO6 | IO-3.3 | See General User I/O, page 33. |
| **A58** | GPIO5_IO8/GPIO_BL0_ON | IO-3.3 | Backlight 0 on/off |
| **A59** | GPIO3_IO3/GPIO_PANEL_ENABLE | IO-3.3 | Digital display, Panel enable |
| **A60** | GND | P | Ground |
| **A61** | NC | | |
| **A62** | DISP_DAT23 | O-3.3 | Digital display, Data 23 (Red 7) |
| **A63** | DISP_DAT22 | O-3.3 | Digital display, Data 22 (Red 6) |
| **A64** | DISP_DAT21 | O-3.3 | Digital display, Data 21 (Red 5) |
| **A65** | DISP_DAT20 | O-3.3 | Digital display, Data 20 (Red 4) |
| **A66** | DISP_DAT19 | O-3.3 | Digital display, Data 19 (Red 3) |
| **A67** | DISP_DAT18 | O-3.3 | Digital display, Data 18 (Red 2) |
| **A68** | DISP_DAT17 | O-3.3 | Digital display, Data 17 (Red 1) |
| **A69** | DISP_DAT16 | O-3.3 | Digital display, Data 16 (Red 0) |
| **A70** | GND | P | Ground |
| **A71** | DISP_DAT15 | O-3.3 | Digital display, Data 15 (Green 7) |
| **A72** | DISP_DAT14 | O-3.3 | Digital display, Data 14 (Green 6) |
| **A73** | DISP_DAT13 | O-3.3 | Digital display, Data 13 (Green 5) |
| **A74** | DISP_DAT12 | O-3.3 | Digital display, Data 12 (Green 4) |
| **A75** | DISP_DAT11 | O-3.3 | Digital display, Data 11 (Green 3) |
| **A76** | DISP_DAT10 | O-3.3 | Digital display, Data 10 (Green 2) |
| **A77** | DISP_DAT9 | O-3.3 | Digital display, Data 9 (Green 1) |
| **A78** | DISP_DAT8 | O-3.3 | Digital display, Data 8 (Green 0) |
| **A79** | DISP_DAT7 | O-3.3 | Digital display, Data 7 (Blue 7) |
| **A80** | GND | P | Ground |
| **A81** | DISP_DAT6 | O-3.3 | Digital display, Data 6 (Blue 6) |
| **A82** | DISP_DAT5 | O-3.3 | Digital display, Data 5 (Blue 5) |
| **A83** | DISP_DAT4 | O-3.3 | Digital display, Data 4 (Blue 4) |
| **A84** | DISP_DAT3 | O-3.3 | Digital display, Data 3 (Blue 3) |
| **A85** | DISP_DAT2 | O-3.3 | Digital display, Data 2 (Blue 2) |
| **A86** | DISP_DAT1 | O-3.3 | Digital display, Data 1 (Blue 1) |
| **A87** | DISP_DAT0 | O-3.3 | Digital display, Data 0 (Blue 0) |
| **A88** | DISP_HSYNC | O-3.3 | Digital display, Horizontal sync |
| **A89** | DISP_DRDY | O-3.3 | Digital display, Data ready |
| **A90** | GND | P | Ground |
| **A91** | DISP_VSYNC | O-3.3 | Digital display, Vertical sync |
| **A92** | DISP_PIXCLK | O-3.3 | Digital display, Pixel clock |
| **A93** | GND | P | Ground |
| **A94** | ETH_TXRX2P | IO-A | Ethernet, MDI 2 positive signal |
| **A95** | ETH_TXRX2M | IO-A | Ethernet, MDI 2 negative signal |
| **A96** | GND | P | Ground |
| **A97** | ETH_TXRX3P | IO-A | Ethernet, MDI 3 positive signal |
| **A98** | ETH_TXRX3M | IO-A | Ethernet, MDI 3 negative signal |
| **A99** | GND | P | Ground |
| **A100** | GND | P | Ground |
| **A101** | GND | P | Ground |
| **A102** | GND | P | Ground |
| **A103** | VDD_IN | PI | Power input (3.3 V nominal) |
| **A104** | VDD_IN | PI | Power input (3.3 V nominal) |
| **A105** | VDD_IN | PI | Power input (3.3 V nominal) |
| **A106** | VDD_IN | PI | Power input (3.3 V nominal) |

| Pin | Name | Type | Description |
|---|---|---|---|
| **A107** | VDD_IN | PI | Power input (3.3 V nominal) |
| **A108** | VDD_IN | PI | Power input (3.3 V nominal) |
| **A109** | VDD_IN | PI | Power input (3.3 V nominal) |
| **A110** | GND | P | Ground |
| **B1** | GND | P | Ground |
| **B2** | UART2_RXD | I-3.3 | Serial 2, Receive Data (note 2) |
| **B3** | UART2_RTS | O-3.3 | Serial 2, Request To Send |
| **B4** | UART2_TXD | O-3.3 | Serial 2, Transmit Data (note 2) |
| **B5** | UART2_CTS | I-3.3 | Serial 2, Clear To Send |
| **B6** | GPIO5_IO7/GPIO_SER_BUF_ON | IO-3.3 | External EIA-232 buffer shutdown |
| **B7** | I2C3_SDA | IO-3.3 | $I^2C$ data for general-purpose use |
| **B8** | I2C3_SCL | O-3.3 | $I^2C$ clock for general-purpose use |
| **B9** | SD2_WP | I-3.3 | SD 2, Write Protect |
| **B10** | SD2_CD# | I-3.3 | SD 2, Card Detect |
| **B11** | GND | P | Ground |
| **B12** | SD2_CLK | O-3.3 | SD 2, Clock |
| **B13** | SD2_CMD | IO-3.3 | SD 2, Command |
| **B14** | SD2_DAT0 | IO-3.3 | SD 2, Data 0 |
| **B15** | SD2_DAT1 | IO-3.3 | SD 2, Data 1 |
| **B16** | SD2_DAT2 | IO-3.3 | SD 2, Data 2 |
| **B17** | SD2_DAT3 | IO-3.3 | SD 2, Data 3 |
| **B18** | GPIO3_IO1/GPIO_SER_B_RS232 | O-3.3 | External EIA-232 buffer enable |
| **B19** | GPIO3_IO2/GPIO_SER_C_RS232 | O-3.3 | External EIA-232 buffer enable |
| **B20** | GPIO1_IO1/GPIO_BL1_ON | IO-3.3 | Backlight 1 on/off |
| **B21** | GND | P | Ground |
| **B22** | GPIO1_IO2/GPIO_BL2_ON | IO-3.3 | Backlight 2 on/off |
| **B23** | GPIO1_IO3/GPIO_RGB_PANEL_ON | IO-3.3 | Digital display, External buffer enable |
| **B24** | GPIO1_IO4/GPIO_AUD_ENA | IO-2.5 | Digital audio, External audio codec power enable |
| **B25** | GPIO4_IO1GPIO_HP_DET | I-3.3 | Digital audio, Headphone detect |
| **B26** | GPIO4_IO2 | IO-3.3 | See General User I/O, page 33. |
| **B27** | GPIO4_IO3/GPIO_SD4_PWR_EN# | IO-3.3 | SD 2, Power enable |
| **B28** | GPIO6_IO1/GPIO_ACCEL_INT1 | I-3.3 | Programmable accelerometer interrupt |
| **B29** | GPIO6_IO2/GPIO_ACCEL_INT2 | I-3.3 | Programmable accelerometer interrupt |
| **B30** | GPIO6_IO3/GPIO_BUTTON | IO-3.3 | User-defined button input |
| **B31** | GND | P | Ground |
| **B32** | CCM_CLKO | O | Clock source for Audio and CMOS Camera |
| **B33** | KP_ROW0 | IO-3.3 | Keypad, Row 0 |
| **B34** | KP_ROW1 | IO-3.3 | Keypad, Row 1 |
| **B35** | KP_ROW2 | IO-3.3 | Keypad, Row 2 |
| **B36** | KP_ROW3 | IO-3.3 | Keypad, Row 3 |
| **B37** | KP_ROW4 | IO-3.3 | Keypad, Row 4 |
| **B38** | KP_ROW5 | IO-3.3 | Keypad, Row 5 |
| **B39** | KP_ROW6 | IO-3.3 | Keypad, Row 6 |
| **B40** | KP_ROW7 | IO-3.3 | Keypad, Row 7 |
| **B41** | GND | P | Ground |
| **B42** | USB_OTG_DN | IO-USB | USB OTG, Data negative |
| **B43** | USB_OTG_DP | IO-USB | USB OTG, Data positive |
| **B44** | GND | P | Ground |
| **B45** | USB_OTG_ID | I-3.3 | USB OTG, ID input |
| **B46** | VDD_USB_5V | PIO | USB OTG, Power input/output (5 V) |
| **B47** | VDD_USB_5V | PIO | USB OTG, Power input/output (5 V) |
| **B48** | VDD_USB_5V | PIO | USB OTG, Power input/output (5 V) |
| **B49** | PMIC_PWR_CYCLE# | I | See Power Management Signals, page 36. |
| **B50** | GPIO5_IO9/GPIO_nHOST1_PWR_CTRL | IO-3.3 | External USB hub host 1 power enable |
| **B51** | GND | P | Ground |
| **B52** | GPIO5_IO10/GPIO_nHOST2_PWR_CTRL | IO-3.3 | External USB hub host 2 power enable |
| **B53** | GPIO5_IO11/GPIO_nHOST3_PWR_CTRL | IO-3.3 | External USB hub host 3 power enable |
| **B54** | GPIO5_IO12/GPIO_CSI_RST_B | IO-3.3 | CMOS Camera, Reset |
| **B55** | GPIO5_IO13/GPIO_CSI_PWM | IO-3.3 | CMOS Camera, PWM |
| **B56** | GPIO5_IO14/GPIO_LVDS_PWR_EN | O-3.3 | LVDS display, Power enable |
| **B57** | GPIO5_IO15/GPIO_PCIE_RESET | IO-3.3 | External PCIe device reset |
| **B58** | GPIO5_IO16/GPIO_LED_RED | IO-3.3 | User-controlled LED output |
| **B59** | GPIO7_IO2/GPIO_LED_GRN | IO-3.3 | User-controlled LED output |
| **B60** | GND | P | Ground |
| **B61** | LVDS0_TX0N | O-LVDS | LVDS 0, Data 0 negative |
| **B62** | LVDS0_TX0P | O-LVDS | LVDS 0, Data 0 positive |
| **B63** | GND | P | Ground |
| **B64** | LVDS0_TX1N | O-LVDS | LVDS 0, Data 1 negative |
| **B65** | LVDS0_TX1P | O-LVDS | LVDS 0, Data 1 positive |
| **B66** | GND | P | Ground |
| **B67** | LVDS0_TX2N | O-LVDS | LVDS 0, Data 2 negative |
| **B68** | LVDS0_TX2P | O-LVDS | LVDS 0, Data 2 positive |
| **B69** | GND | P | Ground |
| **B70** | GND | P | Ground |

| Pin | Name | Type | Description |
|---|---|---|---|
| **B71** | LVDS0_TX3N | O-LVDS | LVDS 0, Data 3 negative |
| **B72** | LVDS0_TX3P | O-LVDS | LVDS 0, Data 3 positive |
| **B73** | GND | P | Ground |
| **B74** | LVDS0_CLKN | O-LVDS | LVDS 0, Clock negative |
| **B75** | LVDS0_CLKP | O-LVDS | LVDS 0, Clock positive |
| **B76** | GND | P | Ground |
| **B77** | GND | P | Ground |
| **B78** | PWM1 | O-A | Pulse Width Modulator 1 |
| **B79** | PWM2 | O-A | Pulse Width Modulator 2 |
| **B80** | GND | P | Ground |
| **B81** | BOOT_MODE0 | O-SNVS | Boot mode master configuration |
| **B82** | BOOT_MODE1 | O-SNVS | Boot mode master configuration |
| **B83** | TAMPER | O-SNVS | Indicator for enclosure tampering |
| **B84** | RESET_BTN# | I | See Power Management Signals, page 36. |
| **B85** | GPIO1_IO5/SLEEP_EVENT | IO-3.3 | See Power Management Signals, page 36. |
| **B86** | RUN_STATE# | O | See Power Management Signals, page 36. |
| **B87** | ON_STATE | O | See Power Management Signals, page 36. |
| **B88** | ON_OFF_BTN# | I | See Power Management Signals, page 36. |
| **B89** | WDOG_TIMEOUT | O-3.3 | Watchdog timeout |
| **B90** | GND | P | Ground |
| **B91** | ETH_LED1_C | O | Ethernet LED 1, Cathode |
| **B92** | ETH_LED2_C | O | Ethernet LED 2, Cathode |
| **B93** | GND | P | Ground |
| **B94** | ETH_TXRX1P | IO-A | Ethernet, MDI 1 positive signal |
| **B95** | ETH_TXRX1M | IO-A | Ethernet, MDI 1 negative signal |
| **B96** | GND | P | Ground |
| **B97** | ETH_TXRX0P | IO-A | Ethernet, MDI 0 positive signal |
| **B98** | ETH_TXRX0M | IO-A | Ethernet, MDI 0 negative signal |
| **B99** | GND | P | Ground |
| **B100** | GND | P | Ground |
| **B101** | GND | P | Ground |
| **B102** | GND | P | Ground |
| **B103** | VDD_IN | PI | Power input (3.3 V nominal) |
| **B104** | VDD_IN | PI | Power input (3.3 V nominal) |
| **B105** | VDD_IN | PI | Power input (3.3 V nominal) |
| **B106** | VDD_IN | PI | Power input (3.3 V nominal) |
| **B107** | VDD_IN | PI | Power input (3.3 V nominal) |
| **B108** | VDD_IN | PI | Power input (3.3 V nominal) |
| **B109** | VDD_IN | PI | Power input (3.3 V nominal) |
| **B110** | GND | P | Ground |

## *J2: Docking Connector: PCIe, SPI, CMOS Camera, MIPI CSI, MIPI DSI, GPIO, MLB Bus, SD, S/PDIF, LVDS Display, HDMI Display, SATA*

Board connector: 220-pin, stacking board-to-board receptacle, 0.5 mm, Tyco Electronics 3-6318490-6
Carrier board connector: Tyco Electronics 3-1827253-6, 5 mm stacking height
Tyco Electronics 3-6318491-6, 8 mm stacking height

Connector J2 mates to the carrier board. Data signals are provided on this docking connector.

| Pin | Name | Type | Description |
|---|---|---|---|
| **A1** | GND | P | Ground |
| **A2** | SPI3_MISO | I-3.3 | SPI 3, Master input |
| **A3** | SPI3_MOSI | O-3.3 | SPI 3, Master output |
| **A4** | SPI3_RDY | I-3.3 | SPI 3, Ready |
| **A5** | SPI3_SCLK | O-3.3 | SPI 3, Serial clock |
| **A6** | SPI3_SS0 | O-3.3 | SPI 3, Chip select 0 |
| **A7** | NC | | |
| **A8** | NC | | |
| **A9** | NC | | |
| **A10** | NC | | |
| **A11** | GND | P | Ground |
| **A12** | UART4_TXD_CSI_DAT12 | O/O-3.3 | Serial 4, Transmit Data / CMOS Camera, Data 12 |
| **A13** | UART4_RXD_CSI_DAT13 | I/O-3.3 | Serial 4, Receive Data / CMOS Camera, Data 13 |
| **A14** | UART5_TXD_CSI_DAT14 | O/O-3.3 | Serial 5, Transmit Data / CMOS Camera, Data 14 |
| **A15** | UART5_RXD_CSI_DAT15 | I/O-3.3 | Serial 5, Receive Data / CMOS Camera, Data 15 |

| Pin | Name | Type | Description |
|---|---|---|---|
| **A16** | UART4_RTS_CSI_DAT16 | O/O-3.3 | Serial 4, Request To Send / CMOS Camera, Data 16 |
| **A17** | UART4_CTS_CSI_DAT17 | I/O-3.3 | Serial 4, Clear To Send / CMOS Camera, Data 17 |
| **A18** | UART5_RTS_CSI_DAT18 | O/O-3.3 | Serial 5, Request To Send / CMOS Camera, Data 18 |
| **A19** | UART5_CTS_CSI_DAT19 | I/O-3.3 | Serial 5, Clear To Send / CMOS Camera, Data 19 |
| **A20** | NC | | |
| **A21** | GND | P | Ground |
| **A22** | PCIE_RXM | I_PCIe | PCIe, Receive negative |
| **A23** | PCIE_RXP | I_PCIe | PCIe, Receive positive |
| **A24** | GND | P | Ground |
| **A25** | PCIE_TXM | O-PCIe | PCIe, Transmit negative |
| **A26** | PCIE_TXP | O-PCIe | PCIe, Transmit positive |
| **A27** | GND | P | Ground |
| **A28** | PCIE_CLKM | O | PCIe, Clock negative |
| **A29** | PCIE_CLKP | O | PCIe, Clock positive |
| **A30** | GND | P | Ground |
| **A31** | GND | P | Ground |
| **A32** | DSI_CLK0M | O-MIPI | MIPI DSI, Clock negative |
| **A33** | DSI_CLK0P | O-MIPI | MIPI DSI, Clock positive |
| **A34** | GND | P | Ground |
| **A35** | DSI_D0M | O-MIPI | MIPI DSI, Data 0 negative |
| **A36** | DSI_D0P | O-MIPI | MIPI DSI, Data 0 positive |
| **A37** | GND | P | Ground |
| **A38** | DSI_D1M | O-MIPI | MIPI DSI, Data 1 negative |
| **A39** | DSI_D1P | O-MIPI | MIPI DSI, Data 1 positive |
| **A40** | GND | P | Ground |
| **A41** | GND | P | Ground |
| **A42** | GPIO7_IO1/GPIO_DSI_RST_B | IO-3.3 | MIPI DSI, Reset |
| **A43** | NC | | |
| **A44** | NC | | |
| **A45** | NC | | |
| **A46** | NC | | |
| **A47** | SPDIF_IN | I-2.5 | S/PDIF, Data in |
| **A48** | SPDIF_OUT | O-3.3 | S/PDIF, Data out |
| **A49** | SPDIF_SRCLK | O-3.3 | S/PDIF, Receive clock |
| **A50** | SPDIF_PLOCK | O-3.3 | S/PDIF, Lock |
| **A51** | GND | P | Ground |
| **A52** | SPDIF_EXTCLK | O-2.5 | S/PDIF, External clock |
| **A53** | NC | | |
| **A54** | NC | | |
| **A55** | NC | | |
| **A56** | NC | | |
| **A57** | NC | | |
| **A58** | NC | | |
| **A59** | NC | | |
| **A60** | GND | P | Ground |
| **A61** | NC | | |
| **A62** | NC | | |
| **A63** | NC | | |
| **A64** | NC | | |
| **A65** | NC | | |
| **A66** | NC | | |
| **A67** | NC | | |
| **A68** | NC | | |
| **A69** | NC | | |
| **A70** | GND | P | Ground |
| **A71** | NC | | |
| **A72** | NC | | |
| **A73** | NC | | |
| **A74** | NC | | |
| **A75** | NC | | |
| **A76** | NC | | |
| **A77** | NC | | |
| **A78** | NC | | |
| **A79** | NC | | |
| **A80** | GND | P | Ground |
| **A81** | SATA_RXM | I-SATA | SATA, Receive negative |
| **A82** | SATA_RXP | I-SATA | SATA, Receive positive |
| **A83** | GND | P | Ground |
| **A84** | SATA_TXM | O-SATA | SATA, Transmit negative |
| **A85** | SATA_TXP | O-SATA | SATA, Transmit positive |

| Pin | Name | Type | Description |
|---|---|---|---|
| **A86** | GND | P | Ground |
| **A87** | NC | | |
| **A88** | NC | | |
| **A89** | NC | | |
| **A90** | GND | P | Ground |
| **A91** | NC | | |
| **A92** | NC | | |
| **A93** | NC | | |
| **A94** | NC | | |
| **A95** | HDMI_CEC | O-3.3 | HDMI Display,<br>Consumer Electronics Control |
| **A96** | HDMI_HPD | I-HDMI | HDMI Display, Hot Plug Detect |
| **A97** | GND | P | Ground |
| **A98** | HDMI_D2M | O-HDMI | HDMI Display, Data 2 negative |
| **A99** | HDMI_D2P | O-HDMI | HDMI Display, Data 2 positive |
| **A100** | GND | P | Ground |
| **A101** | HDMI_CLKP | O-HDMI | HDMI Display, Clock positive |
| **A102** | HDMI_CLKM | O-HDMI | HDMI Display, Clock negative |
| **A103** | GND | P | Ground |
| **A104** | HDMI_D0M | O-HDMI | HDMI Display, Data 0 negative |
| **A105** | HDMI_D0P | O-HDMI | HDMI Display, Data 0 positive |
| **A106** | GND | P | Ground |
| **A107** | HDMI_D1M | O-HDMI | HDMI Display, Data 1 negative |
| **A108** | HDMI_D1P | O-HDMI | HDMI Display, Data 1 positive |
| **A109** | GND | P | Ground |
| **A110** | GND | P | Ground |
| **B1** | GND | P | Ground |
| **B2** | NC | | |
| **B3** | NC | | |
| **B4** | NC | | |
| **B5** | NC | | |
| **B6** | NC | | |
| **B7** | NC | | |
| **B8** | NC | | |
| **B9** | NC | | |
| **B10** | NC | | |
| **B11** | GND | P | Ground |
| **B12** | CSI_DATA_EN | O-3.3 | CMOS Camera, Data enable |
| **B13** | CSI_HSYNC | O-3.3 | CMOS Camera, Horizontal sync |
| **B14** | CSI_VSYNC | O-3.3 | CMOS Camera, Vertical sync |
| **B15** | CSI_PIXCLK | O-3.3 | CMOS Camera, Pixel clock |
| **B16** | NC | | |
| **B17** | NC | | |
| **B18** | NC | | |
| **B19** | NC | | |
| **B20** | NC | | |
| **B21** | GND | P | Ground |
| **B22** | NC | | |
| **B23** | NC | | |
| **B24** | NC | | |
| **B25** | NC | | |
| **B26** | NC | | |
| **B27** | NC | | |
| **B28** | NC | | |
| **B29** | NC | | |
| **B30** | GPIO7_IO3/GPIO_DSI_PWR_EN | IO-3.3 | MIPI DSI, Power enable |
| **B31** | GND | P | Ground |
| **B32** | GND | P | Ground |
| **B33** | MLB_DN | I-MLB | MLB Bus, Data negative |
| **B34** | MLB_DP | I-MLB | MLB Bus, Data positive |
| **B35** | GND | P | Ground |
| **B36** | MLB_SN | I-MLB | MLB Bus, Signal negative |
| **B37** | MLB_SP | I-MLB | MLB Bus Signal positive |
| **B38** | GND | P | Ground |
| **B39** | MLB_CN | I-MLB | MLB Bus, Clock negative |
| **B40** | MLB_CP | I-MLB | MLB Bus, Clock positive |
| **B41** | GND | P | Ground |
| **B42** | SD4_CMD | IO-3.3 | SD 4, Command |
| **B43** | SD4_DAT0 | IO-3.3 | SD 4, Data 0 |
| **B44** | SD4_DAT1 | IO-3.3 | SD 4, Data 1 |
| **B45** | SD4_DAT2 | IO-3.3 | SD 4, Data 2 |
| **B46** | SD4_DAT3 | IO-3.3 | SD 4, Data 3 |
| **B47** | SD4_DAT4 | IO-3.3 | SD 4, Data 4 |
| **B48** | SD4_DAT5 | IO-3.3 | SD 4, Data 5 |

| Pin | Name | Type | Description |
|---|---|---|---|
| **B49** | SD4_DAT6 | IO-3.3 | SD 4, Data 6 |
| **B50** | SD4_DAT7 | IO-3.3 | SD 4, Data 7 |
| **B51** | GND | P | Ground |
| **B52** | SD4_CLK | O-3.3 | SD 4, Clock |
| **B53** | SD4_CD# | I-3.3 | SD 4, Card Detect |
| **B54** | SD4_WP | I-3.3 | SD 4, Write Protect |
| **B55** | SD4_PWR_EN# | O-3.3 | SD4, Power enable |
| **B56** | VDD_SD | PO | SD4, Power out (3.3 V) |
| **B57** | VDD_SD | PO | SD4, Power out (3.3 V) |
| **B58** | NC | | |
| **B59** | NC | | |
| **B60** | GND | P | Ground |
| **B61** | LVDS1_TX0N | O-LVDS | LVDS 1, Data 0 negative |
| **B62** | LVDS1_TX0P | O-LVDS | LVDS 1, Data 0 positive |
| **B63** | GND | P | Ground |
| **B64** | LVDS1_TX1N | O-LVDS | LVDS 1, Data 1 negative |
| **B65** | LVDS1_TX1P | O-LVDS | LVDS 1, Data 1 positive |
| **B66** | GND | P | Ground |
| **B67** | LVDS1_TX2N | O-LVDS | LVDS 1, Data 2 negative |
| **B68** | LVDS1_TX2P | O-LVDS | LVDS 1, Data 2 positive |
| **B69** | GND | P | Ground |
| **B70** | GND | P | Ground |
| **B71** | LVDS1_TX3N | O-LVDS | LVDS 1, Data 3 negative |
| **B72** | LVDS1_TX3P | O-LVDS | LVDS 1, Data 3 positive |
| **B73** | GND | P | Ground |
| **B74** | LVDS1_CLKN | O-LVDS | LVDS 1, Clock negative |
| **B75** | LVDS1_CLKP | O-LVDS | LVDS 1, Clock positive |
| **B76** | GND | P | Ground |
| **B77** | PWM3 | O-A | Pulse Width Modulator 3 |
| **B78** | PWM4 | O-A | Pulse Width Modulator 4 |
| **B79** | GND | P | Ground |
| **B80** | GND | P | Ground |
| **B81** | CSI_D0P | O-MIPI | MIPI CSI, Data 0 positive |
| **B82** | CSI_D0M | O-MIPI | MIPI CSI, Data 0 negative |
| **B83** | GND | P | Ground |
| **B84** | CSI_D1P | O-MIPI | MIPI CSI, Data 1 positive |
| **B85** | CSI_D1M | O-MIPI | MIPI CSI, Data 1 negative |
| **B86** | GND | P | Ground |
| **B87** | CSI_CLK0P | O-MIPI | MIPI CSI, Clock positive |
| **B88** | CSI_CLK0M | O-MIPI | MIPI CSI, Clock negative |
| **B89** | GND | P | Ground |
| **B90** | GND | P | Ground |
| **B91** | CSI_D2P | O-MIPI | MIPI CSI, Data 2 positive |
| **B92** | CSI_D2M | O-MIPI | MIPI CSI, Data 2 negative |
| **B93** | GND | P | Ground |
| **B94** | CSI_D3P | O-MIPI | MIPI CSI, Data 3 positive |
| **B95** | CSI_D3M | O-MIPI | MIPI CSI, Data 3 negative |
| **B96** | GND | P | Ground |
| **B97** | NC | | |
| **B98** | NC | | |
| **B99** | NC | | |
| **B100** | GND | P | Ground |
| **B101** | NC | | |
| **B102** | NC | | |
| **B103** | NC | | |
| **B104** | NC | | |
| **B105** | NC | | |
| **B106** | NC | | |
| **B107** | NC | | |
| **B108** | NC | | |
| **B109** | NC | | |
| **B110** | GND | P | Ground |

## *J3: microSD Card*

Board connector: microSD card socket, Molex 502570-0893
Mating connector: microSD card

The CPU-301-16 includes a microSD card socket (4-bit) for standalone use. Power to this socket is software-controlled. These SD signals are also available on J1. For further details, see Secure Digital, page 17.

### J4: HDMI Display

Board connector: HDMI Micro socket, Molex 46765-2001
Mating connector: HDMI Micro cable assembly, Molex 68786 series

The CPU-301-16 includes an HDMI Micro socket providing a standard HDMI connection for standalone use. These HDMI signals are also available on J2. For further details, see HDMI Display, page 27.

### J6: JTAG

Board connector: 2x5 terminal strip, 2 mm, Samtec TMM-105-06-S-D

The JTAG port, provided on connector J6, is available for factory test and software debugging. Otherwise, this port is not supported for application use.

### J9: Gigabit Ethernet

Board connector: 1x12 header, 1.25mm, Molex 53261-1271
Mating connector: wire-to-board crimp housing, Molex 51021-1200

Header J9 provides a connection to the on-board Ethernet physical layer transceiver MDI for standalone use. This interface is also available on J1. For further details, see Gigabit Ethernet, page 21.

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | ETH_LED1_A | O | Ethernet LED 1, Anode |
| 2 | ETH_LED1_C | O | Ethernet LED 1, Cathode |
| 3 | ETH_LED2_C | O | Ethernet LED 2, Cathode |
| 4 | ETH_TXRX0P | IO-A | Ethernet, MDI 0 positive signal |
| 5 | ETH_TXRX0M | IO-A | Ethernet, MDI 0 negative signal |
| 6 | ETH_TXRX1P | IO-A | Ethernet, MDI 1 positive signal |
| 7 | ETH_TXRX1M | IO-A | Ethernet, MDI 1 negative signal |
| 8 | ETH_TXRX2P | IO-A | Ethernet, MDI 2 positive signal |
| 9 | ETH_TXRX2M | IO-A | Ethernet, MDI 2 negative signal |
| 10 | ETH_TXRX3P | IO-A | Ethernet, MDI 3 positive signal |
| 11 | ETH_TXRX3M | IO-A | Ethernet, MDI 3 negative signal |

### J10: Power

Board connector: 1x6 shrouded header, 1.5 mm, Molex 87438-0643
Mating connector: wire-to-board crimp housing, Molex 87439-0601

The CPU-301-16 receives input power from header J10 (for standalone use) or connector J1 (for use with a carrier board). For a description of the power supply, see Power Supply Architecture, page 35.

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | VDD_IN | PI | Power input (3.3 V nominal) |
| 2 | VDD_IN | PI | Power input (3.3 V nominal) |
| 3 | VDD_IN | PI | Power input (3.3 V nominal) |
| 4 | GND | P | Ground |
| 5 | GND | P | Ground |
| 6 | GND | P | Ground |

**Warning:**
Disconnect the power input before removing the CPU-301-16 form a carrier board. Removing the board from a powered carrier board may result in damage to both the carrier board and to the CPU-301-16.

## *J11: Peripherals*

Board connector: 1x17 header, 1.25 mm, Molex 53261-1771
Mating connector: wire-to-board crimp housing, Molex

Header J11 provides connections to the USB OTG port, Serial 2 port (EIA-232 levels), general-purpose $I^2C$ bus, and five GPIO for standalone use. These signals are also available on J1.

| Pin | Name | Type | On-board Termination | Description |
|---|---|---|---|---|
| **1** | VDD_USB_5V | PIO | | USB OTG, Power input/output (5 V) |
| **2** | C_USB_OTG_DP | IO-USB | | USB OTG, Data (note 11) |
| **3** | C_USB_OTG_DN | IO-USB | | |
| **4** | GND | P | | Ground |
| **5** | OTG_ID | I | PU 10kΩ V3.3 | USB OTG, ID input (note 12) |
| **6** | SERIAL_RXD | I-EIA232 | | Receive Data (note 13) |
| **7** | SERIAL_TXD | O-EIA232 | | Transmit Data (note 13) |
| **8** | GND | P | | Ground |
| **9** | I2C3_SCL | O | PU 10kΩ V3.3 | $I^2C$ clock for general-purpose use |
| **10** | I2C3_SDA | IO | PU 10kΩ V3.3 | $I^2C$ data for general-purpose use |
| **11** | GND | P | | Ground |
| **12** | GPIO5 | IO-3.3 | PU 10kΩ V3.3 | See Power Management Signals, page 36. (note 14) |
| **13** | GPIO4 | IO-3.3 | | See General User I/O, page 33. (note 15) |
| **14** | GPIO3 | IO-3.3 | | See General User I/O, page 33. (note 16) |
| **15** | GPIO2 | IO-3.3 | | See General User I/O, page 33. (note 17) |
| **16** | GPIO1 | IO-3.3 | | See General User I/O, page 33. (note 18) |
| **17** | GND | P | | Ground |

Notes:

11. C_USB_OTG_DP/C_USB_OTG_DN are connected to USB_OTG_DP (J1 B43)/USB_OTG_DN (J1 B42) through an EMI suppression filter.
12. OTG_ID is connected to USB_OTG_ID (J1 B45) through a 1kΩ series resistor.
13. SERIAL_RXD/SERIAL_TXD are UART2_RXD (J1 B2)/UART2_TXD (J1 B4) buffered at EIA232 levels.
14. GPIO5 is connected to GPIO1_IO5 (J1 B85) through a 1kΩ series resistor.
15. GPIO4 is connected to GPIO5_IO6 (J1 A57) through a 1kΩ series resistor.
16. GPIO3 is connected to GPIO5_IO5 (J1 A56) through a 1kΩ series resistor.
17. GPIO2 is connected to GPIO5_IO4 (J1 A55) through a 1kΩ series resistor.
18. GPIO1 is connected to GPIO5_IO3 (J1 A54) through a 1kΩ series resistor.

# System Specifications

## Power Supply

The CPU-301-16 is designed to meet the power supply specifications listed in the following table. For a description of the power supply, see Power Supply Architecture, page 35.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| **Power Input** | | | | | |
| **VDD_IN** | Input supply voltage | 3.135 | 3.3 | 3.465 | V |
| **$I_{VDD\_IN}$** | Input current | | 0.7 | 1.5 | A |
| **ON_STATE, RUN_STATE# (note 19)** | | | | | |
| **$V_{OH}$** | High-level output voltage<br>$I_{OH}$ = -16 mA, VCC = 3 V | 2.4 | 2.75 | | V |
| **$V_{OL}$** | Low-level output voltage<br>$I_{OL}$ = 16 mA, VCC = 3 V | | 0.16 | 0.4 | V |
| **PMIC_PWR_CYCLE#** | | | | | |
| **$V_H$** | High-level voltage | | Pull up to 3.0V | | V |
| **$V_{IL}$** | Low-level input voltage | | 0.1 | | V |
| **ON_OFF_BTN#** | | | | | |
| **$V_H$** | High-level voltage | | Pull up to 3.0V | | V |
| **$V_{IL}$** | Low-level input voltage | | 0.1 | | V |
| **RESET_BTN# (note 20)** | | | | | |
| **$V_{IH}$** | High-level voltage | | Pull up to 3.0V | | V |
| **$V_{IL}$** | Low-level input voltage | | 0.1 | | V |

Notes:

19. Specifications per the Fairchild NC7WZ17 Product Datasheet, Rev. 1.0.6, January 2012, www.fairchildsemi.com.
20. Specifications per the Freescale Semiconductor PF0100 Product Datasheet, Rev. 3.0, 10/2012, Document order number MMPF0100, www.freescale.com.

## Electrical

This section provides electrical specifications for the CPU-301-16. For additional details about voltage rail and termination of individual signals, see the sections included in Hardware Specification, page 15.

### *Inputs and Outputs*

The following table defines the electrical specifications for signals listed as inputs (I-3.3 or I-2.5) and outputs (O-3.3 or O-2.5) in the pinout tables for J1, page 46 and J2, page 49.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| **Input (note 21, 22)** | | | | | |
| **$V_{IH}$** | High-level input voltage | 0.7 x OVDD | | OVDD | V |
| **$V_{IL}$** | Low-level input voltage | 0 | | 0.3 x OVDD | V |
| **Output (note 21, 22)** | | | | | |
| **$V_{OH}$** | High-level output voltage<br>$I_{OH}$ = -1 mA | OVDD – 0.15 | | | V |
| **$V_{OL}$** | Low-level output voltage<br>$I_{OL}$ = 1 mA | | | 0.15 | V |
| **$R_{DRV}$** | Output driver impedance Single-ended | | 50 | | Ω |
| | Output driver impedance Differential | | 100 | | Ω |

Notes:

21. OVDD = 3.3 V or 2.5 V. For signal type, see Signal Headers, page 46.
22. Specifications per the Freescale Semiconductor i.MX 6Dual/Quad Applications Processor Data Sheet, Rev. 1, 11/2012, Document Number: IMX6DQCEC, www.freescale.com.

### *Ethernet LED*

The Ethernet physical layer transceiver located on the CPU-301-16 drives two programmable LED control signals as specified in the following table. For a description of the Gigabit Ethernet, see Gigabit Ethernet, page 21.

| Symbol | Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| **ETH_LEDx_C** | | | | | |
| $I_{LED}$ | Output drive current (note 23) | | 8 | | mA |
| $R_{PU}$ | Pull-up resistance | | 10 | | kΩ |
| $V_{PU}$ | | | | 2.5 | V |

Notes:

23. Specifications per the Micrel KSZ9031RNX Data Sheet, Rev. 1.0, October 2012, M9999-103112-1.0, www.micrel.com.

### *Crystal Frequencies*

Agencies certifying the CPU-301-16 for compliance for radio-frequency emissions typically need to know the frequencies of on-board oscillators and the maximum on-board signal rate. The maximum on-board signal rate is 533MHz, while the following table lists the frequencies of all crystals on the CPU-301-16.

| Crystals | Device | Typ. | Units |
|---|---|---|---|
| **X1** | Processor, high frequency (XTAL) | 24.000 | MHz |
| **X2** | Processor, low frequency (RTC_XTAL) | 32.768 | KHz |
| **X3** | Gigabit Ethernet | 25.000 | MHz |

# Environmental

The CPU-301-16 is designed to meet the environmental specifications listed in the following table.

| Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|
| **Commercial operating temperature** | 0 | | +70 | °C |
| **Extended operating temperature (note 24)** | -40 | | +85 | °C |
| **Storage temperature** | -40 | | +85 | °C |

Notes:

24. For availability of industrial temperature range boards, contact your local Eurotech representative.

# Appendix A – Reference Information

**Product Information**

Product notices, updated drivers, support material:
www.eurotech.com

**Processor**

i.MX 6 Solo/6Dual/6Quad Applications Processors and Power Management Integrated Circuit data sheets:
www.freescale.com

**SATA**

Serial ATA specification:
www.sata-io.org

**USB**

Universal Serial Bus specification:
www.usb.org

**SDIO Card**

SD Card Association and SDIO specification:
www.sdcard.org

**PCI SIG**

PCI Express specification:
www.pcisig.com

**MDI**

Gigabit Ethernet Physical Layer Transceiver and Media Dependent Interface:
www.micrel.com

**CAN**

CAN specification:
www.semiconductors.bosch.de

**$I^2C$ Bus**

$I^2C$ bus specification:
www.nxp.com

**HDMI**

HDMI specification:
www.hdmi.org

**MIPI**

MIPI DSI and MIPI CSI specification:
www.mipi.org

# Appendix B – Board Revision

This guide applies to the current revision of the board as given in the following section.

## Identifying the Board Revision

The revision number of the printed wiring board is printed on the board. That number is 170127-400Rx. The “x” indicates the revision level of the PWB.

The board also includes a label providing additional revision information. The number beginning with 621 indicates bill of materials used to build the board; while the number beginning with 900 indicates the configuration.

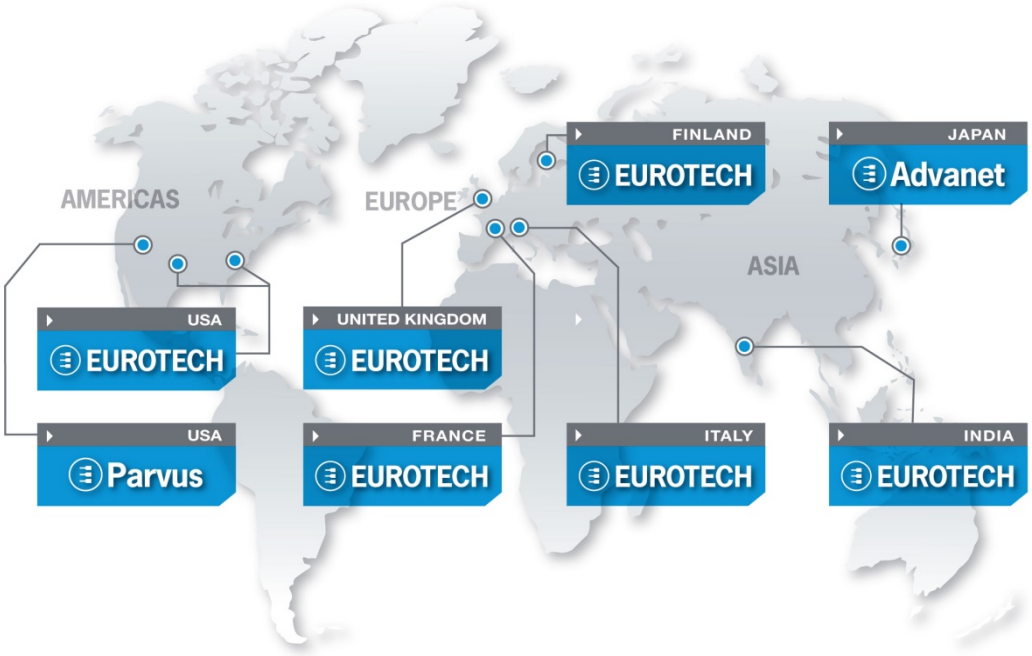
## Board Revision History

The following is an overview of the revisions to the CPU-301-16.

### *Revision 1*

Initial release

# Eurotech Worldwide Presence

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