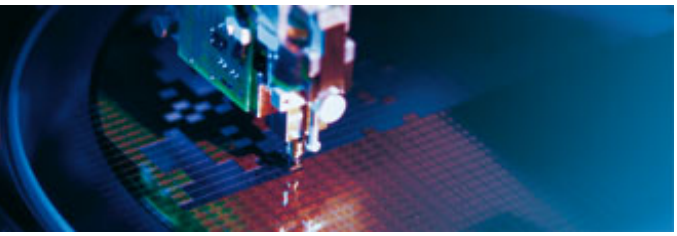
USER MANUAL



TurboXb Module

Application-ready Module

Rev B – September 2012 – 110130-0000B

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Revision History

Issue no.	*PWB*	*Date*	*Comments*
0		Nov-2007	Preliminary draft
A		Nov-2010	Initial release
B		Sept-2012	Corrected diagram in section 3.1.1. Updated contact page.

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1 Introduction

1.1 Overview

The TurboXb is a full-featured, application-ready module using the PXA270 XScale RISC microprocessor. It integrates with an application-specific solution board for a total production solution.

The cover image shows a revision A TurboXb module. However, this manual applies to the latest revision of the TurboXb, as listed in the revision history, section 7.2.

1.2 Features

1.2.1 Processor

- PXA270 32-bit XScale Processor
- Clock rates from 104 to 520 MHz
- Voltage and frequency scaling

1.2.2 Power Supply

- 3.3 V main power input
- VCORE power generation

1.2.3 Memory

- 64 MB synchronous DRAM and 32 MB Flash memory
  (Other memory configurations are available as volume production options.)
- Expansion Bus

1.2.4 Communications

- USB 1.1 Host port (low 1.5 Mbps and full 12 Mbps speeds) and full speed Function port
- Three Serial ports (3.3 V logic-level)
- 10/100 Mbps Ethernet
- Secure Digital (SD) and Multimedia Card (MMC) interface
- Two Synchronous Serial Ports (SSP)
- I^2C bus with I^2C master device

1.2.5 User Interface and Display

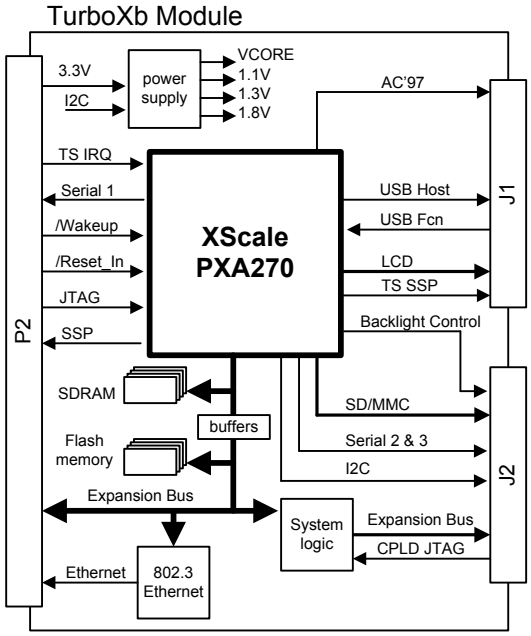
- Flat Panel interface
- Backlight control signals for Intensity and On/Off
- Analog Touch Panel support

1.2.6 Audio Interface

- AC '97 Codec interface

1.3 Block Diagram

The following diagram illustrates the system organization of the TurboXb. Arrows indicate the direction of control and not necessarily signal flow.



2 Getting Started

2.1 Development System

TurboXb Development Systems are designed to get the developer up and running quickly.

To use the system, simply plug the power supply into the receptacle on the system.

If the screen does not display anything after five to ten seconds, check the *Frequently Asked Questions*, below. Most operating systems cold boot within twenty seconds.

2.1.1 System Components

A typical BitsyX Development System is shown at right. The TurboXb Development System conforms to the same format. It consists of the following components:

- TurboXb application-ready module
- Solution Board
- Flat panel display and cable
- Backlight inverter and cable
- Touch panel and cable
- 100-240 VAC power adapter
- Plexiglas mounting
- Developer's Cable Kit including
  - Serial Port DB9 adapter (Eurotech cable #610111-80001)
  - DB9F/F null modem cable
  - USB A-B cable
- Operating system of your choice
- User's Guide (this document and operating system guide)

Please make sure you have received ***all*** the components before you begin your development.

2.2 Frequently Asked Questions

The following are some of the most commonly asked questions about development systems:

Q: When I plug in power, my screen is white and nothing comes up on it.

A: Check the connector seating. The flat panel connector may have come loose in shipping. Press it firmly into the panel and reapply power to your system.

Q: When I plug in power, the LED doesn't turn on.

A: Your system may still be booting. The LED is software-controlled and is not necessarily turned on at boot.

Q: Do I have to turn off the system before I insert a CompactFlash card?

A: No. The TurboXb supports hot-swapping of CompactFlash cards. Consult the operating system documentation for details.

Q: Do I need to observe any ESD precautions when working with the system?

A: Yes. Where possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the board or touching any components on the board.

Q: What do I need to start developing my application for the system?

A: You will need a flash ATA card (32 MiB or larger, 128 MiB recommended) and the cables supplied with your system to interface your development station to the system. For further direction, consult the user guide for the installed operating system.

Q: Who can I call if I need help developing my application?

A: Eurotech provides technical support to get your development system running. For customers who establish a business relationship with Eurotech, we provide support to develop applications and drivers.

Q: Is there online support?

A: Yes. Information about the TurboXb hardware and software is available on the Eurotech support site at http://support.eurotech-inc.com/. See section 2.3 for further details.

Q: Can I upgrade the version of the operating system?

A: Yes. Eurotech provides regular operating system updates on its developers' web site. For operating systems not maintained by Eurotech, contact the operating system vendor.

Q: I would like to interface to a different display panel. How can I do this?

A: Eurotech may have already interfaced to the panel you are interested in. Consult Eurotech for availability.

2.3 Errata, Addenda and Further Information

Errata and addenda to this manual are posted on the Eurotech support forums along with the latest release of the manual. Consult the support forums any time you need further information or feel information in this manual is in error. You may access the forums from the Eurotech support site,

http://support.eurotech-inc.com/

In addition to manuals, the support forums include downloads, troubleshooting guides, operating system updates, and answers to hundreds of questions about developing applications for Eurotech products. You may also post questions you have about Eurotech products on the forums.

3 Hardware Reference

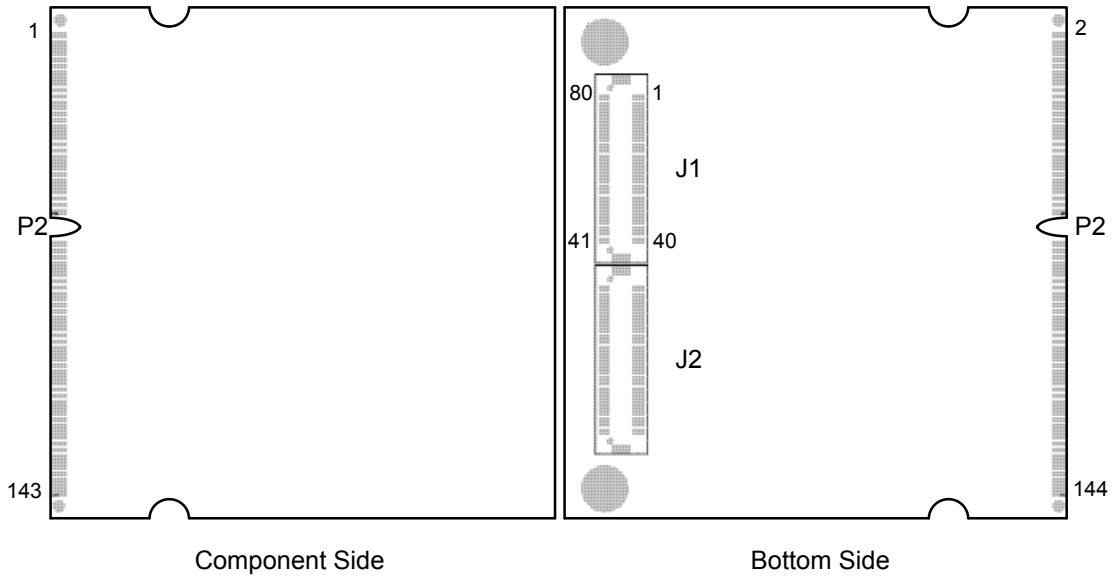
This section gives a description, including location and pinouts, of the connectors on the TurboXb.

3.1 Identifying Connectors

This section describes the location and numbering of the connectors on the board.

3.1.1 Locating Connectors

The following diagram illustrates the location of key components on the TurboXb. When viewing the module from the component side, connector J1 and connector J2 lie under the module. The "component side" of the TurboXb module is the one on which the processor and most large chips are populated. For precision measurements of the location of the connectors on the system, refer to section 6.1.1.



3.1.2 Determining Pin Numbers

Connectors J1, J2 and P2 do not follow the standard pin numbering of most double-row headers. The card-edge connector P2 places odd pins on the component side and even pins on the bottom side. Connectors J1 and J2 place pins 1 to 40 on one side and 41 to 80 on the other. The diagram in section 3.1.1 indicates how pins are numbered on these connectors.

To locate pin 1 of a connector, try the following:

1. Look for a visible number or marking on the board that indicates connector pin numbering. Pin numbers are indicated on the solder mask.
2. Download the mechanical drawing of the TurboXb module from the Eurotech support site (section 2.3). The indicated pad on each connector is pin 1.

3.2 Signal Headers

The following tables describe the electrical signals available on the connectors of the TurboXb. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions, and references to related chapters.

Legend:

n/c	Not connected
GND	digital ground plane
(3.2)	Reference section for signals

Signal Types:

I	signal is an input to the system
O	signal is an output from the system
IO	signal may be input or output
P	power and ground
A	analog signal
OC	open-collector
OD	open-drain

3.2.1 P2: Docking Header: System Bus, Ethernet, SSP, Serial 1 & CPU JTAG

Board Connector: Card-edge connector

The TurboXb module is installed in a SODIMM socket on a solution board.

Pin	Name	PXA270 GPIO	Type	Termination On Module (note 1)	Description
1	ETHER_RX-		I		Ethernet Receive -
2	/RESET_IN		OD	pull up, 10kΩ	Hardware Reset
3	ETHER_RX+		I		Ethernet Receive +
4	/WAKEUP	1	I	pull up, 33kΩ	Wakeup
5	ETHER_TX-		O		Ethernet Transmit -
6	/FAST_CS		O		Fast Chip Select
7	ETHER_TX+		O		Ethernet Transmit +
8	/SLOW_CS		O		Slow Chip Select
9	GND		P		ground
10	GPIO15	15	IO	pull up, 33kΩ	General Purpose IO
11	/ETHER_ACT_LED		O		Ethernet Speed Indicator
12	/BOOT_CS		O		Boot Chip Select
13	/ETHER_LNK_LED		O		Ethernet Link & Activity Indicator
14	/uP_IOWR		O		Variable-latency I/O Write Enable
15	/BATT_FAULT		I	pull up, 10kΩ pull down 100kΩ	Main Battery Fault
16	/uP_MRD		O		Static Memory Output Enable
17	GND		P		ground
18	3.3V_WRLAN		PO		Ethernet power
19	3.3V_IN		PI		3.3V input power
20	Reserved				
21	/WAKEUP	1	I	pull up, 33kΩ	Wakeup
22	/CHRDY		I	pull up, 10kΩ	Channel Ready
23	GPIO99	99	IO	pull up, 33kΩ	General Purpose IO

Pin	Name	PXA270 GPIO	Type	Termination On Module (note 1)	Description
24	n/c				unused
25	GPIO27	27	IO	pull up, 33kΩ	General Purpose IO
26	n/c				unused
27	/IRQ_TS	22	I	pull up, 33kΩ	Touch panel interrupt
28	/CPU_TRST		I	pull up, 10kΩ	PXA270 JTAG
29	GPIO12	12	IO	pull up, 33kΩ	General Purpose IO
30	CPU_TMS		I	pull up, 33kΩ	PXA270 JTAG
31	n/c				unused
32	CPU_TDO		O		PXA270 JTAG
33	n/c				unused
34	CPU_TDI		I	pull up, 33kΩ	PXA270 JTAG
35	n/c				unused
36	CPU_TCK		I	pull down, 33kΩ	PXA270 JTAG
37	/uP_WAIT	18	IO	pull up, 4.7kΩ	Variable Latency IO Ready
38	n/c				unused
39	RTS1T	41	O		Serial 1 Full-Function UART
40	n/c				unused
41	CTS1T	35	I	pull down, 33kΩ	Serial 1 Full-Function UART
42	n/c				unused
43	TXD1T	39	O	pull up, 10kΩ	Serial 1 Full-Function UART
44	n/c				unused
45	RXD1T	34	I	pull up, 33kΩ	Serial 1 Full-Function UART
46	GPIO97	97	IO	pull up, 33kΩ	General Purpose IO
47	DTR1T	40	O		Serial 1 Full-Function UART
48	GPIO20	20	IO	pull up, 33kΩ	General Purpose IO
49	DSR1T	37	I		Serial 1 Full-Function UART
50	/RESET_OUT		O		Reset Out
51	/VDD_FAULT		I	pull up, 33kΩ	VDD Fault
52	n/c				unused
53	uP_AUX_CLK		O	series 22Ω	SDRAM Memory Clock
54	GPIO96	96	IO		General Purpose IO
55	GND		P		ground
56	GPIO21	21	IO		General Purpose IO
57	n/c				unused
58	n/c				unused
59	n/c				unused
60	n/c				unused
61	3.3V_IN		PI		3.3V input power
62	3.3V_IN		PI		3.3V input power
63	3.3V_IN		PI		3.3V input power
64	3.3V_IN		PI		3.3V input power
65	SSP_FRM	24	O		SSP Slave Select
66	uP_BUS_CLK		O	series 22Ω	Synchronous Static Memory Clock

Pin	Name	PXA270 GPIO	Type	Termination On Module (note 1)	Description
67	SSP_MOSI	25	O		SSP Transmit Data
68	GND		P		ground
69	SSP_MISO	26	I	pull up, 33kΩ	SSP Receive Data
70	/uP_RAS		O	series 22Ω	SDRAM Row Address Strobe
71	SSP_SCK	23	O		SSP Clock
72	/uP_CAS		O	series 22Ω	SDRAM Column Address Strobe
73	uP_MD0		IO		Expansion Bus, Data 0
74	n/c				unused
75	uP_MD1		IO		Expansion Bus, Data 1
76	n/c				unused
77	uP_MD2		IO		Expansion Bus, Data 2
78	n/c				unused
79	uP_MD3		IO		Expansion Bus, Data 3
80	uP_RD_/WR		O		Read/Write
81	uP_MD4		IO		Expansion Bus, Data 4
82	/uP_MWR		O		Memory Write Enable
83	uP_MD5		IO		Expansion Bus, Data 5
84	/uP_MRD		O		Memory Output Enable
85	uP_MD6		IO		Expansion Bus, Data 6
86	n/c				unused
87	uP_MD7		IO		Expansion Bus, Data 7
88	DCD1T	36	I		Serial 1 Data Carrier Detect
89	GND		P		ground
90	uP_MA0		O		Expansion Bus, Address 0
91	uP_MD8		IO		Expansion Bus, Data 8
92	uP_MA1		O		Expansion Bus, Address 1
93	uP_MD9		IO		Expansion Bus, Data 9
94	uP_MA2		O		Expansion Bus, Address 2
95	uP_MD10		IO		Expansion Bus, Data 10
96	uP_MA3		O		Expansion Bus, Address 3
97	uP_MD11		IO		Expansion Bus, Data 11
98	uP_MA4		O		Expansion Bus, Address 4
99	uP_MD12		IO		Expansion Bus, Data 12
100	uP_MA5		O		Expansion Bus, Address 5
101	uP_MD13		IO		Expansion Bus, Data 13
102	uP_MA6		O		Expansion Bus, Address 6
103	uP_MD14		IO		Expansion Bus, Data 14
104	uP_MA7		O		Expansion Bus, Address 7
105	uP_MD15		IO		Expansion Bus, Data 15
106	uP_MA8		O		Expansion Bus, Address 8
107	3.3V_IN		PI		3.3 V input power
108	uP_MA9		O		Expansion Bus, Address 9
109	GND		P		ground
110	uP_MA10		O		Expansion Bus, Address 10
111	uP_MD16		IO		Expansion Bus, Data 16
112	uP_MA11		O		Expansion Bus, Address 11
113	uP_MD17		IO		Expansion Bus, Data 17

Pin	Name	PXA270 GPIO	Type	Termination On Module (note 1)	Description
114	*uP_MA12*		*O*		*Expansion Bus, Address 12*
115	*uP_MD18*		*IO*		*Expansion Bus, Data 18*
116	*uP_MA13*		*O*		*Expansion Bus, Address 13*
117	*uP_MD19*		*IO*		*Expansion Bus, Data 19*
118	*uP_MA14*		*O*		*Expansion Bus, Address 14*
119	*uP_MD20*		*IO*		*Expansion Bus, Data 20*
120	*uP_MA15*		*O*		*Expansion Bus, Address 15*
121	*uP_MD21*		*IO*		*Expansion Bus, Data 21*
122	*uP_MA16*		*O*		*Expansion Bus, Address 16*
123	*uP_MD22*		*IO*		*Expansion Bus, Data 22*
124	*uP_MA17*		*O*		*Expansion Bus, Address 17*
125	*uP_MD23*		*IO*		*Expansion Bus, Data 23*
126	*uP_MA18*		*O*		*Expansion Bus, Address 18*
127	*GND*		*P*		*ground*
128	*uP_MA19*		*O*		*Expansion Bus, Address 19*
129	*uP_MD24*		*IO*		*Expansion Bus, Data 24*
130	*uP_MA20*		*O*		*Expansion Bus, Address 20*
131	*uP_MD25*		*IO*		*Expansion Bus, Data 25*
132	*uP_MA21*		*O*		*Expansion Bus, Address 21*
133	*uP_MD26*		*IO*		*Expansion Bus, Data 26*
134	*uP_MA22*		*O*		*Expansion Bus, Address 22*
135	*uP_MD27*		*IO*		*Expansion Bus, Data 27*
136	*uP_MA23*		*O*		*Expansion Bus, Address 23*
137	*uP_MD28*		*IO*		*Expansion Bus, Data 28*
138	*uP_MA24*		*O*		*Expansion Bus, Address 24*
139	*uP_MD29*		*IO*		*Expansion Bus, Data 29*
140	*uP_MA25*		*O*		*Expansion Bus, Address 25*
141	*uP_MD30*		*IO*		*Expansion Bus, Data 30*
142	*/uP_AEN*		*O*		*Address Enable*
143	*uP_MD31*		*IO*		*Expansion Bus, Data 31*
144	*3.3V_IN*		*PI*		*3.3V input power*

Note:

1. Pull-ups are to 3.3 V unless otherwise specified.

3.2.2 J1: Docking Header: Display, Touch Panel, USB, Audio

Board Connector: 2x40 pin header, 0.5mm, Hirose DF12(3.0)-80DP-0.5V(86)

Mating Connector: 2x40 pin receptacle, 0.5mm, Hirose DF12(3.0)-80DS-0.5V(86)

Connector J1 of the TurboXb module mates to a receptacle on a solution board

Pin	Name	PXA270 GPIO	Type	Termination On Module (note 2)	Description
1	n/c				unused
2	n/c				unused
3	n/c				unused
4	n/c				unused
5	n/c				unused
6	n/c				unused
7	n/c				unused
8	n/c				unused
9	n/c				unused
10	n/c				unused
11	n/c				unused
12	n/c				unused
13	n/c				unused
14	n/c				unused
15	n/c				unused
16	n/c				unused
17	GND		P		ground
18	AC97_SD_OUT	30	O		AC'97 Serial Data Out
19	AC97_SD_IN	29	I		AC'97Serial Data Ins
20	AC97_SYNC	31	O		AC'97 Sync
21	/AC97_RESET	113	O		AC'97 Reset
22	AC97_BITCLK	28	I		AC'97 Bit Clock
23	STATUS2		O		Status 2
24	/CFON		O		CF Enable
25	n/c				unused
26	n/c				unused
27	n/c				unused
28	n/c				unused
29	LDD16	86	O		LCD Display Data 16
30	n/c				unused
31	n/c				unused
32	GND		P		ground
33	n/c				unused
34	/TS_CS	14	O		Touch panel Frame
35	TS_CLK	19	O		Touch panel Clock
36	L_BIAS	77	O		LCD Bias Drive
37	LDD17	87	O		LCD Display Data 17
38	L_PCLK	76	O	series 22Ω 15pF to GND	LCD Pixel Clock
39	L_LCLK	75	O		LCD Line Clock
40	L_FCLK	74	O		LCD Frame Clock
41	LDD15	73	O		LCD Display Data 15
42	LDD11	69	O		LCD Display Data 11
43	LDD12	70	O		LCD Display Data 12
44	GND		P		ground

Pin	Name	PXA270 GPIO	Type	Termination On Module (note 2)	Description
45	LDD13	71	O		LCD Display Data 13
46	LDD14	72	O		LCD Display Data 14
47	LDD15	73	O		LCD Display Data 15
48	LDD5	63	O		LCD Display Data 5
49	LDD6	64	O		LCD Display Data 6
50	LDD7	65	O		LCD Display Data 7
51	LDD8	66	O		LCD Display Data 8
52	LDD9	67	O		LCD Display Data 9
53	LDD10	68	O		LCD Display Data 10
54	LDD4	62	O		LCD Display Data 4
55	GND		P		ground
56	LDD0	58	O		LCD Display Data 0
57	LDD1	59	O		LCD Display Data 1
58	LDD2	60	O		LCD Display Data 2
59	LDD3	61	O		LCD Display Data 3
60	LDD4	62	O		LCD Display Data 4
61	/CF_CE		O		CF Chip Enable
62	uP_PCC_RDYA	53	O	pull up, 10kΩ	DRAM Clock Enable
63	COM2_ON		O		Serial 2 Enable
64	COM1_3_ON		O		Serial 1 & 3 Enable
65	USBH_OVR_CRNT	88	I		USB Host Power Indicator
66	GND		P		ground
67	/USBC_OVR_CRNT		I	pull down, 1kΩ	USB Function Power Indicator
68	USBH_PWR_EN		O		USB Host Power Enable
69	/USBC_PWR_EN		O		USB Function Power Enable
70	USBH_M		AIO		USB Host port -
71	USBH_P		AIO		USB Host port +
72	USBC_M		AIO		USB Function port -
73	USBC_P		AIO		USB Function port +
74	/uP_BUFF_OE		O		Expansion Bus Data Buffer Output Enable
75	GND		P		ground
76	uP_BUFF_DIR_DATA		O		Expansion Bus Data Buffer Direction
77	GND		P		ground
78	n/c				unused
79	n/c				unused
80	n/c				unused

Note:

2. Pull-ups are to 3.3 V unless otherwise specified.

3.2.3 J2: Docking Header: CF, SD/MMC, Serial 2 & 3, I²C & CPLD JTAG

Board Connector: 2x40 pin header, 0.5mm, Hirose DF12(3.0)-80DP-0.5V(86)

Mating Connector: 2x40 pin receptacle, 0.5mm, Hirose DF12(3.0)-80DS-0.5V(86)

Connector J2 of the TurboXb module mates to a receptacle on a solution board.

Pin	Module Name	PXA270 GPIO	Type	Termination On Module (note 3)	Description
1	/AUDIO_ON	101	O		Audio On Control
2	SD_DAT1	109	IO	pull up, 33kΩ	SD/MMC Data 1
3	SD_DAT2	110	IO	pull up, 33kΩ	SD/MMC Data 2
4	SD_DAT3	111	IO	pull up, 33kΩ	SD/MMC Data 3
5	Backlight_ON/OFF	100	O		Control for Backlight On/Off switch
6	/PANEL_ON	95	O		Panel On Control
7	UBUFF_PNL_ENA	94	O		Unbuffered LCD Panel Enable
8	LED0	93	O		Software-Controllable Status
9	GND		P		ground
10	RXD2T	46	I	pull up, 33kΩ	Serial 2 Standard UART
11	TXD2T	47	O		Serial 2 Standard UART
12	uP_DQM0		O		SDRAM DQM Data byte mask control
13	uP_DQM1		O		SDRAM DQM Data byte mask control
14	uP_DQM2		O		SDRAM DQM Data byte mask control
15	uP_DQM3		O		SDRAM DQM Data byte mask control
16	uP_BUFF_DIR_DATA		O		Expansion Bus Data Buffer Direction
17	/CFBEN	108	O	pull up, 33kΩ	CF Buffer Enable
18	GPIO103	103	IO	pull up, 33kΩ	General Purpose IO
19	GPIO104	104	IO	pull up, 33kΩ	General Purpose IO
20	GND		P		ground
21	/CFREG	55	O		CF Register Select
22	/CFDETECT	107	I	pull up, 33kΩ	CF Card Detect
23	GPIO106	106	IO	pull up, 33kΩ	General Purpose IO
24	GPIO98	98	IO	pull up, 33kΩ	General Purpose IO
25	GPIO105	105	IO	pull up, 33kΩ	General Purpose IO
26	/CFWAIT	56	I	pull up, 33kΩ	CF Wait
27	CFREADY	52	I	pull up, 33kΩ	CF Ready
28	/CFIOIS16	57	I		CF I/O Select 16
29	/CFCE2		O		CF High Byte Enable
30	/CFCE1		O		CF Low Byte Enable
31	CFRESET	10	O	pull up, 33kΩ	CF Reset
32	GND		P		ground
33	/CFIOWR	51	O	pull up, 33kΩ	CF I/O Write
34	/CFIORD	50	O	pull up, 33kΩ	CF I/O Read

Pin	Module Name	PXA270 GPIO	Type	Termination On Module (note 3)	Description
35	/CFWE	49	O	pull up, 4.7kΩ	CF Write Enable
36	/CFOE	48	O	pull up, 33kΩ	CF Output Enable
37	CPLD_TDI		I	pull up, 33kΩ	CPLD JTAG
38	CPLD_TMS		I	pull up, 33kΩ	CPLD JTAG
39	CPLD_TD0		O		CPLD JTAG
40	CPLD_TCK		I	pull down, 33kΩ	CPLD JTAG
41	TXD3T	43	O		Serial 3 PXA270 Bluetooth UART
42	RXD3T	42	I	pull up, 33kΩ	Serial 3 PXA270 Bluetooth UART
43	CTS3T	44	I		Serial 3 PXA270 Bluetooth UART
44	GND		P		
45	RTS3T	45	O	pull down, 33kΩ	Serial 3 PXA270 Bluetooth UART
46	TXD2T	47	O		Serial 2 Standard UART
47	RXD2T	46	I	pull up, 33kΩ	Serial 2 Standard UART
48	SD_CMD	112	IO	pull up, 33kΩ	SD/MMC Command
49	AUDIOPA_ON	102	O		Audio Power Amplifier On
50	SD_DAT0	92	IO	pull up, 33kΩ	SD/MMC Data 0
51	SD_CLK	32	O		SD/MMC Card Bus Clock
52	SW0	91	I		DIP Switch 0 (note 4)
53	UIO		IO	pull up, 33kΩ	USIM IO
54	SW1	114	I		DIP Switch 1 (note 4)
55	GND		P		ground
56	/SD_CD	116	I	pull down, 33kΩ	SD/MMC Card Detect
57	/SD_WP	115	I		SD/MMC Write Protect
58	/SD_ON	90	O		SD/MMC Power Control
59	RIB1T	38	I		Serial 1 Ring Indicator
60	/PCC_CE1A		O		PC Card Chip Enable 1
61	n/c				unused
62	/PCC_CE2A		O		PC Card Chip Enable 2
63	I2C_SCL	3	IO	pull up, 1.2kΩ	Power Manager I2C Clock
64	I2C_SDA	4	IO	pull up, 1.2kΩ	Power Manager I2C Data
65	TS_DIN	13	O		Touch panel Data In (to solution board)
66	GND		P		ground
67	TS_DOUT	11	I		Touch Panel Data Out (from solution board)
68	VEEPWM	17	O		Contrast Control PWM
69	BCKPWM	80	O		Backlight PWM
70	uP_SDCKE		O		SDRAM Clock Enable
71	GPIO118	118	IO		General Purpose IO
72	/uP_SDCS1		O		SDRAM Chip Select
73	n/c				unused
74	PWR_EN		O		Core Power Enable
75	SYS_EN		O		System Power Enable

Pin	Module Name	PXA270 GPIO	Type	Termination On Module (note 3)	Description
76	*GPIO84*	*84*	*IO*		*General Purpose IO*
77	*GND*		*P*		*ground*
78	*GPIO82*	*82*	*IO*	*pull up, 33kΩ*	*General Purpose IO*
79	*/CARDAON*	*81*	*O*		*CF Power Enable*
80	*/CARDAON_5V*	*83*	*O*		*CF Voltage Sense*

Note:

3. Pull-ups are to 3.3 V unless otherwise specified.
4. Include 47kΩ pull-up resistors for SW0 (J2 52) and SW1 (J2 54) on the solution board.

4 Feature Reference

This chapter provides details about the various features of the TurboXb and about how they can fit together to create a system that meets your application needs. The TurboXb is a full-featured, application-ready module. It integrates with an application-specific solution board for a total production solution.

The details provided in this manual document how the TurboXb functions with the Eurotech Solution Board. This solution board implements many of the TurboXb capabilities. Designers can use the schematic as a reference design for developing custom boards. For a full description of the Eurotech Solution Board and its features, refer to the TurboXb Development System User's Manual.

Design details are provided as guidelines only and apply to the revision listed in the revision history (section 7.2). See the Eurotech support site (section 2.3) for the latest release of the schematic and manuals.

4.1 Processor Architecture

The TurboXb bases its architecture on the PXA270 XScale RISC microprocessor. This section describes the core functionality specific to the TurboXb including boot code, interrupts, and GPIO assignments. See the Intel PXA27x Processor Family: Developer's Manual. (Order number 280000-001, April 2004) for a complete description of the processor architecture.

4.1.1 Boot Code

The TurboXb uses the first block of on-board flash to store the boot code. At the factory, boot code is loaded using the JTAG interface located on connector P2 (section 3.2.1). Most Eurotech TurboXb boot loaders are field-upgradeable by including a CompactFlash (CF) port on the solution board.

4.1.2 Interrupts

The XScale processor GPIOs support external interrupts. When programmed as an input, a GPIO can serve as an interrupt source. The current Eurotech BSP uses several GPIOs as interrupts. The following table summarizes the external interrupt sources and the devices to which they are connected. Additional GPIOs are available for use as external interrupts. However, the current BSP may not support them. If your application requires additional interrupts, contact Eurotech Sales for information about modifying the BSP.

See the Operating System Manual for details about how the XScale handles interrupts.

Interrupt Signal	Module	Solution Board	IRQ Handler
/CPLD_IRQ	*CPLD*		*GPIO0*
/WAKEUP		*Button*	*GPIO1*
/IRQ_TS		*Touch panel*	*GPIO22*
/CFDETECT		*CF port*	*GPIO107*

4.1.3 PXA270 GPIO Cross-Reference

The following table describes how the TurboXb utilizes the XScale GPIO lines (*GPn*) and how each signal is terminated. Some GPIOs are not available on the connectors. These are marked as "internal" in the table. A GPIO pin can perform multiple functions depending upon the application and BSP. This manual describes the function used with the Eurotech Solution Board. However, the Eurotech Solution Board does not use all GPIOs listed.

The XScale maps many alternate functions not listed in the table to the GPIO pins. The Eurotech BSP supports the function given in the following table and may not support the alternate functions. If your application requires use of the alternate functions, contact Eurotech Sales for information about modifying the BSP.

GPIO	Name	Type	Termination On Module (note 5)	Description
0	/CPLD_IRQ	I	pull up, 33kΩ	Interrupt from CPLD (internal)
1	/WAKEUP	I	pull up, 33kΩ	Wakeup
3	I2C_SCL	IO	pull up, 1.2kΩ	Power Manager I2C
4	I2C_SDA	IO	pull up, 1.2kΩ	
9	uP_AUX_CLK	I	series 22Ω	SDRAM Memory Clock (internal)
10	CFRESET	O	pull up, 33kΩ	CF Reset
11	TS_DOUT	I		Touch Panel Data Out (from solution board)
12	GPIO12	IO	pull up, 33kΩ	General Purpose IO
13	TS_DIN	O		Touch panel Data In (to solution board)
14	/TS_CS	O		Touch panel Frame
15	GPIO15	IO	pull up, 33kΩ	General Purpose IO
16	CPLD_CLK	O		CPLD Clock (internal)
17	VEEPWM	O		Contrast Control PWM
18	/uP_WAIT	IO	pull up, 4.7kΩ	Variable Latency IO Ready
19	TS_CLK	O		Touch panel Clock
20	GPIO20	IO	pull up, 33kΩ	General Purpose IO
21	GPIO21	IO		General Purpose IO
22	/IRQ_TS	I	pull up, 33kΩ	Touch panel Interrupt
23	SSP_SCK	O		SSP 1
24	SSP_FRM	O		
25	SSP_MOSI	O		
26	SSP_MISO	I	pull up, 33kΩ	
27	GPIO27	IO	pull up, 33kΩ	General Purpose IO
28	AC97_BITCLK	I		AC'97 Codec Signals
29	AC97_SD_IN	I		
30	AC97_SD_OUT	O		
31	AC97_SYNC	O		
32	SD_CLK	O		SD/MMC Bus Clock
33	/CS5	O	pull up, 4.7kΩ	Chip Select for Static memory (internal)
34	RXD1T	I	pull up, 33kΩ	Serial 1 Full-Function UART
35	CTS1T	I	pull down, 33kΩ	
36	DCD1T	I		
37	DSR1T	I		
38	RIB1T	I		
39	TXD1T	O	pull up, 10kΩ	
40	DTR1T	O		
41	RTS1T	O		

GPIO	Name	Type	Termination On Module (note 5)	Description
42	RXD3T	I	pull up, 33kΩ	Serial 3, Bluetooth UART
43	TXD3T	O		
44	CTS3T	I		
45	RTS3T	O	pull down, 33kΩ	
46	RXD2T	I	pull up, 33kΩ	Serial 2, Standard UART
47	TXD2T	O		
48	/CFOE	O	pull up, 33kΩ	CF Output Enable
49	/CFWE	O	pull up, 4.7kΩ	CF Write Enable
50	/CFIORD	O	pull up, 33kΩ	CF I/O Read
51	/CFIOWR	O	pull up, 33kΩ	CF I/O Write
52	CFREADY	I	pull up, 33kΩ	CF Ready
53	uP_PCC_RDYA	O	pull up, 10kΩ	DRAM Clock Enable
54	/PCC_CE2	O	pull up, 33kΩ	PC Card Enable 2 (internal)
55	/CFREG	O		CF Register Select
56	/CFWAIT	I	pull up, 33kΩ	CF Wait
57	/CFIOIS16	I		CF I/O Select 16
58	LDD0	O		LCD Display Data 0-15
59	LDD1	O		
60	LDD2	O		
61	LDD3	O		
62	LDD4	O		
63	LDD5	O		
64	LDD6	O		
65	LDD7	O		
66	LDD8	O		
67	LDD9	O		
68	LDD10	O		
69	LDD11	O		
70	LDD12	O		
71	LDD13	O		
72	LDD14	O		
73	LDD15	O		
74	L_FCLK	O		LCD Vertical Sync
75	L_LCLK	O		LCD Horizontal Sync
76	L_PCLK	O	series 22Ω 15pF to GND	LCD Pixel Clock
77	L_BIAS	O		LCD Data Enable
78	/CS2	O	pull up, 4.7kΩ	Chip Select for Static memory (internal)
79	PSKTSEL	O	pull up, 33kΩ	PC Card Slot Select (internal)
80	BCKPWM	O		Backlight PWM
81	/CARDAON	O		CF Power Enable
82	GPIO82	IO	pull up, 33kΩ	General Purpose IO
83	/CARDAON_5V	O		CF Voltage Sense
84	GPIO84	IO		General Purpose IO
85	/PCC_CE1	O	pull up, 33kΩ	PC Card Enable 1 (internal)
86	LDD16	O		LCD Display Data 16

GPIO	Name	Type	Termination On Module (note 5)	Description
87	LDD17	O		LCD Display Data 17
88	USBH_OVR_CRNT	I		USB Host Power Indicator
89	USBHPEN1	O		USB Host Power Enable (internal)
90	/SD_ON	O		SD/MMC Power Control
91	SW0	I		DIP Switch 0
92	SD_DAT0	IO	pull up, 33kΩ	SD/MMC Data 0
93	LED0	O		Software-Controllable Status
94	UBUFF_PNL_ENA	O		LCD Panel Enable
95	/PANEL_ON	O		Panel On Control
96	GPIO96	IO		General Purpose IO
97	GPIO97	IO	pull up, 33kΩ	General Purpose IO
98	GPIO98	IO	pull up, 33kΩ	General Purpose IO
99	GPIO99	IO	pull up, 33kΩ	General Purpose IO
100	Backlight_ON/OFF	O		Backlight On/Off Control
101	/AUDIO_ON	O		Audio On Control
102	AUDIOPA_ON	O		Audio Power Amplifier On
103	GPIO103	IO	pull up, 33kΩ	General Purpose IO
104	GPIO104	IO	pull up, 33kΩ	General Purpose IO
105	GPIO105	IO	pull up, 33kΩ	General Purpose IO
106	GPIO106	IO	pull up, 33kΩ	General Purpose IO
107	/CFDETECT	I	pull up, 33kΩ	CF Card Detect
108	/CFBEN	O	pull up, 33kΩ	CF Buffer Enable
109	SD_DAT1	IO	pull up, 33kΩ	SD/MMC Data 1-3
110	SD_DAT2	IO	pull up, 33kΩ	
111	SD_DAT3	IO	pull up, 33kΩ	
112	SD_CMD	IO	pull up, 33kΩ	SD/MMC Command
113	/AC97_RESET	O		AC'97 Codec Reset
114	SW1	I		DIP Switch 1
115	/SD_WP	I		SD/MMC Write Protect
116	/SD_CD	I	pull down, 33kΩ	SD/MMC Card Detect
117	Reserved			
118	GPIO118	IO		General Purpose IO

Note:

5. Pull-ups are to 3.3 V unless otherwise specified.

4.2 Memory

The TurboXb combined with a solution board provides a variety of storage capabilities. The following sections describe the different types of memory supported by the TurboXb.

4.2.1 Synchronous DRAM

Synchronous DRAM (SDRAM) is included on the TurboXb for kernel, application, and display frame buffer use. Standard memory configuration is 64 MB. Data bus width supports 32-bit accesses while allowing access to individual bytes via the XScale data mask function. The memory clock speed is one-half the CPU core clock speed. Typical memory bus operation is at 99.5 MHz.

The self-refreshed RAM consumes most of the system sleep current. Sleep current increases roughly in direct proportion to the amount of RAM installed.

4.2.2 Non-Volatile Memory

The TurboXb supports several ways to store data that will survive a power failure. Some devices can only be accessed through operating system drivers, and not all are available for application data storage.

Flash Memory

Flash memory is the primary site for non-volatile data storage on the TurboXb. Standard configuration is 32 MB. The data bus width is 32-bit.

Eurotech systems store the operating system, applications, and system configuration settings in the on-board flash. Most operating systems configure a portion of the flash as a flash disk, which acts like a hard disk drive.

CompactFlash Cards

CompactFlash cards provide removable storage in a wide variety of capacities. The TurboXb supports a Type I and II, 3.3 V or 5 V CompactFlash interface on the XScale external memory bus. Section 4.4.7 describes the details of using the TurboXb expansion bus. Adding CompactFlash to a solution board can be a cost-effective means to expand system storage capacity.

SD/MMC Cards

A designer can use the XScale SD/MMC signals to implement a SD/MMC socket on a solution board providing mass storage. Section 4.4.4 describes the details of using the SD/MMC signals.

Real-Time Clock (RTC) NVRAM

A solution board can connect a real-time clock to the TurboXb through the I^2C bus (section 4.4.6). The DS1307 is an example of a RTC device. It retains the system date and time when the system is powered down as long as main or backup power is provided to the chip. Connecting a long-life 3 V battery to the RTC is a common method to supply backup power.

The operating system supports reading the RTC on boot and wakeup and setting the RTC when the system time or date is changed. Drivers are not available to access the internal NVRAM. Contact Eurotech Sales if your application requires this feature.

4.3 System Controller

The System Controller supports the XScale processor providing additional control signals for XScale boot, expansion bus, serial ports, and USB. The following table describes the control signals that are available externally and the termination included on each signal. See section 6.4.4 for electrical specifications.

Connector	Name	Type	Termination On Module (note 6)	Description
P2 6	*/FAST_CS*	*O*		*Fast Chip Select*
P2 8	*/SLOW_CS*	*O*		*Slow Chip Select*
P2 12	*/BOOT_CS*	*O*		*Boot Chip Select*
P2 22	*/CHRDY*	*I*	*pull up, 10kΩ*	*Channel Ready*
P2 142	*/uP_AEN*	*O*		*Address Enable*
J1 17	*/CFON*	*O*		*CF Enable*
J1 18	*STATUS2*	*O*		*Status 2*
J1 74	*/uP_BUFF_OE*	*O*		*Data Buffer Output Enable*
J1 76 *J2 25*	*uP_BUFF_DIR_DATA*	*O*		*Data Buffer Direction*
J1 61	*/CF_CE*	*O*		*CF Chip Enable*
J2 11	*/CFCE1*	*O*		*CF Low Byte Enable*
J2 12	*/CFCE2*	*O*		*CF High Byte Enable*
J2 60	*/PCC_CE1A*	*O*		*PC Card Chip Enable 1*
J2 62	*/PCC_CE2A*	*O*		*PC Card Chip Enable 2*
J1 63	*COM2_ON*	*O*		*Serial 2 Enable*
J1 64	*COM1_3_ON*	*O*		*Serial 1 & 3 Enable*
J1 67	*/USBC_OVR_CRNT*	*I*	*pull down, 1kΩ*	*USB Function Power Indicator*
J1 68	*USBH_PWR_EN*	*O*		*USB Host Power Enable*
J1 69	*/USBC_PWR_EN*	*O*		*USB Function Power Enable*

Note:

6. Pull-ups are to 3.3 V unless otherwise specified.

4.4 Communications

The TurboXb supports several industry-standard channels for communication with peripheral and peer devices. These include USB Host and Function ports, logic-level serial ports, Ethernet, SD/MMC, synchronous serial ports, and I^2C bus. In addition, the XScale external memory bus is included on connector P2, expanding the TurboXb capabilities as a CompactFlash or 3.3 V digital expansion bus.

4.4.1 USB

Signals to implement a USB 1.1 Host port, supporting low (1.5 Mbps) and full (12 Mbps) speeds, and a full speed Function port are included on the TurboXb. Both the USB Host (downstream) port and the USB Function ("Client" or upstream) port are managed by the XScale processor with the System Controller providing additional control signals. These signals are located on connector J1 (section 3.2.2). Electrical specifications for the XScale and System Controller are in sections 6.4.2 and 6.4.4, respectively.

USB Host

XScale USB Host signals, USBH_P and USBH_M, allow connection of one USB device to the TurboXb. USB mouse and keyboard are the most common client devices, but you can connect any USB function device that has USB drivers installed on the TurboXb. These signals connect directly to the XScale processor without termination or transient suppression.

The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The solution board must supply the 5 V power required by client devices. Eurotech recommends use of a power switch. The TurboXb supports two power control signals for the USB Host port. It configures XScale GPIO88 as USBH_OVR_CRNT. This signal is on J1 pin 65 and detects over-current conditions. USBH_PWR_EN is an output from the System Controller that controls power to the USB port. It is located on J1 pin 68.

USB Function (Client)

The TurboXb includes the USB Function (or "Client") port signals, USBC_P and USBC_M. These signals allow the TurboXb to appear as a client device to USB Host devices such as desktop and laptop computers. The USB Function port signals connect directly to the XScale processor without termination or transient suppression.

In order to create a fully functioning USB Function port, designers must consider the following design guidelines. The TurboXb supports the full USB connection speed (12 Mbps). Tying a 1.5 kΩ pull-up to the USB+ signal indicates this capability to host hardware. The System Controller output /USBC_PWR_EN controls power to the 1.5 kΩ pull-up, simulating a cable disconnection to the USB host controller. This signal can force the host to re-enumerate the TurboXb (e.g. after wakeup) and is available on J1 pin 69.

The host computer supplies the USB Function device power. Since the TurboXb is self-powered (not powered by the USB cable), a power input is not needed. However, the USB input power is useful for sensing when a USB cable is connected and for powering the 1.5 kΩ pull-up resistor that indicates full speed. The signal /USBC_OVR_CRNT is an input to the System Controller and indicates a USB cable connection. This signal is located on J1 pin 65.

4.4.2 Serial Ports

The three XScale serial ports are included on the TurboXb at 3.3 V logic levels, as listed in the following table.

Port	# signals	Connector
Serial 1	9-wire	J2, P2
Serial 2	3-wire	J2
Serial 3	5-wire	J2

The XScale standard UART, Serial 2, and Bluetooth UART, Serial 3, supply two or four signals, respectively. Serial 2 uses TX and RX ("three-wire serial", counting GND), while Serial 3 adds RTS and CTS ("five-wire serial", counting GND). Serial 1 uses the XScale full-function UART, which adds four more signals (DTR, DSR, DCD, and RI) to supply the full complement of modem control signals.

The serial port signals connect directly to the XScale and should be treated electrically as GPIOs. See section 6.4.2 for electrical specifications.

4.4.3 Ethernet

A LAN9116 10/100 BT Ethernet controller located on the TurboXb provides Ethernet capability. The Ethernet signals are available on connector P2 (section 3.2.1) for connection to an off-board socket. Electrical specifications are listed in section 6.4.5.

4.4.4 Secure Digital (SD) and Multimedia Card (MMC) Controller

The TurboXb supports Secure Digital Memory (SD), Secure Digital I/O (SDIO), MultiMedia Card (MMC), and synchronous serial (SPI) modes of operation. SD and SDIO cards can run in 4-bit, 1-bit, and SPI modes. MMC cards run in 1-bit or SPI modes. The XScale SD/MMC controller has FIFOs that support Direct Memory Access (DMA) to and from memory.

The XScale SD/MMC controller signals are available on connector J2 (section 3.2.3). XScale GPIO90 configured as /SD_ON can control power to an external SD/MMC socket. See section 6.4.2 for electrical specifications.

This manual lists the signals for use in 4-bit SDIO mode. The following table illustrates how the signals are mapped differently depending on the mode of operation. Signal names and types denote the direction of the signal relative to the TurboXb.

The Secure Digital standard references SPI-mode signals with respect to the card. Pin 2 of the SD header is listed as "Data In". This user manual and PXA270 documents reference the signals with respect to the socket. Pin 2 is listed as "Data Out".

SD socket		TurboXb name	Description					
pin	name		4-bit Mode		1-bit Mode		SPI Mode	
1	*DAT3*	*SD_DAT3*	*Data 3*	*IO*	*unused*	*-*	*/MMC_CS1*	*O*
2	*CMD*	*SD_CMD*	*Command*	*IO*	*Command*	*IO*	*Data Out*	*O*
3	*VSS1*	*ground*	*-*	*P*	*-*	*P*	*-*	*P*
4	*VDD*	*SD_PWR*	*-*	*PO*	*-*	*PO*	*-*	*PO*
5	*CLK*	*SD_CLK*	*Clock*	*O*	*Clock*	*O*	*Clock*	*O*
6	*VSS2*	*ground*	*-*	*P*	*-*	*P*	*-*	*P*
7	*DAT0*	*SD_DAT0*	*Data 0*	*IO*	*Data*	*IO*	*Data In*	*I*
8	*DAT1*	*SD_DAT1*	*Data 1*	*IO*	*Interrupt*	*I*	*Interrupt*	*I*
9	*DAT2*	*SD_DAT2*	*Data 2*	*IO*	*unused*	*-*	*/MMC_CS0*	*O*

In SPI mode, pin 9 of an SD/MMC card is unused. Chip Select 0 is shown in this row to illustrate the alternate signal mapping to SD_DAT2.

Some Secure Digital sockets supply the following signals, which are not part of the SD/SDIO standard. XScale GPIOs implement these signals.

SD pin	TurboXb name	Description	Type
10	*/SD_CD*	*Card Detect*	*I*
11	*/SD_WP*	*Write Protect*	*I*

Operating system drivers may not be available for all modes of operation. Contact Eurotech for driver availability for the operating system you are using.

4.4.5 Synchronous Serial Ports

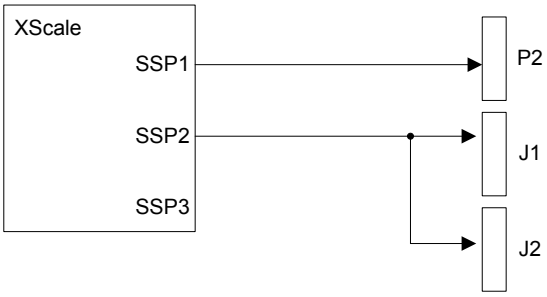
Synchronous serial port (SSP) standards share the same simple architecture: a clock line, transmit and receive lines, ground, and one or more device selects. Each device on the bus requires its own select line. Buses may be full or half-duplex, clocking data one or both directions at the same time, respectively. Each standard defines which devices are bus masters and which are slaves.

To clarify direction of the data signals, the SSP bus master transmit line (TXD) is also known as MOSI (Master Out, Slave In), while its receive line (RXD) is known as MISO (Master In, Slave Out). The Slave Select (SS) signal, which enables the slave device's transmitter, is also known as FRM.

The XScale provides three identical synchronous serial ports, each of which features the following capabilities:

- Frame sizes from 4 to 32-bits
- Sixteen-entry, 32-bit transmit and receive FIFOs
- Adjustable FIFO threshold interrupts
- Bit clock speeds from 6.3 kbps to 13 Mbps
- Support for the following protocols:
    - Motorola's SPI (Serial Peripheral Interface)
    - National Semiconductor's Microwire
    - Texas Instruments' SSP (Synchronous Serial Protocol)
    - PSP (a Programmable Serial Protocol)
- Operation as master or slave
- Receive-without-transmit operation
- SSP/PSP Network mode, supporting up to eight time slots

Each of these features is available for use on the TurboXb. The following diagram illustrates the connectivity of the XScale synchronous serial ports.



The Eurotech BSP makes use of the synchronous serial ports as given in the following table. See section 6.4.2 for electrical specifications.

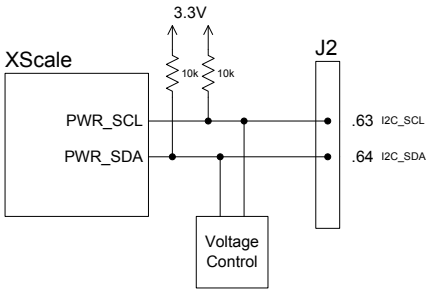
SSP Bus	Connector	Standard Use
SSP1	*P2*	*External SSP*
SSP2	*J1, J2*	*Touch panel controller*
SSP3	*n/a*	*Not Available*

4.4.6 I²C Bus Master

I²C (Inter-IC) Bus is a multi-master, "two-wire" synchronous serial bus developed by Philips for communications between integrated circuits (ICs). The bus master addresses devices using the data line and provides a synchronous clock for reading and writing devices. Client devices respond only when queried by the master device. Philips has developed many I²C devices, but other organizations have adopted I²C as a convenient means for addressing peripherals in a system.

The TurboXb uses the XScale processor as the I²C bus controller to communicate with the CPU core voltage controller. I²C also communicates with external devices on connector J2 (section 3.2.3). Electrical specifications are listed in section 6.4.2.

The following diagram illustrates the I²C architecture on the TurboXb.



The I²C bus address of the voltage control is given in the table below.

Device	Address	Function
LTC1663	0100 000x	Voltage Control

4.4.7 Expansion Bus

The XScale external memory bus along with several additional control signals are available on connectors P2, J1, and J2, expanding the capabilities of the TurboXb. These signals add a CompactFlash socket to a solution board or provide a 3.3 V digital expansion bus.

The signals listed in the following table are buffered before reaching the connector. See section 6.4.3 for electrical specifications.

Name	Type	Description	Pin
uP_MA0-25	*O*	*Address0-25*	*P2*
uP_MD0-31	*IO*	*Data0-7*	*P2*
/uP_IOWR	*O*	*Variable-latency I/O Write Enable*	*P2 14*
/uP_MRD	*O*	*Memory Output Enable*	*P2 16* *P2 84*
/uP_MWR	*O*	*Memory Write Enable*	*P2 82*

Additional signals are included to support external memory accesses and CompactFlash cards. The signals listed in the following tables are not buffered and connect to either the System Controller CPLD or XScale processor. These signals should be treated electrically as GPIOs. The Eurotech Solution Board does not use all signals listed. See sections 6.4.2 and 6.4.4 for electrical specifications.

XScale Processor Signals				
Name	**Type**	**Termination On Module (note 7)**	**Description**	**Pin**
uP_RD_/WR	*O*		*Read/Write*	*P2 80*
uP_BUS_CLK	*O*	*series 22Ω*	*Synchronous Static Memory Clock*	*P2 66*
uP_AUX_CLK	*O*	*series 22Ω*	*SDRAM Memory Clock*	*P2 53*
/uP_WAIT	*IO*	*pull-up, 4.7kΩ*	*Variable Latency IO Ready*	*P2 37*
/uP_RAS	*O*	*series 22Ω*	*SDRAM Row Address Strobe*	*P2 70*
/uP_CAS	*O*	*series 22Ω*	*SDRAM Column Address Strobe*	*P2 72*
uP_SDCKE	*O*		*SDRAM Clock Enable*	*J2 70*
/uP_SDCS1	*O*		*SDRAM Chip Select*	*J2 72*
uP_DQM3	*O*		*SDRAM DQM Data byte mask control*	*J2 26*
uP_DQM2	*O*			*J2 27*
uP_DQM1	*O*			*J2 28*
uP_DQM0	*O*			*J2 29*
/CFOE	*O*	*pull-up, 33kΩ*	*CF Output Enable*	*J2 5*
/CFWE	*O*	*pull-up, 4.7kΩ*	*CF Write Enable*	*J2 6*
/CFIORD	*O*	*pull-up, 33kΩ*	*CF I/O Read*	*J2 7*
/CFIOWR	*O*	*pull-up, 33kΩ*	*CF I/O Write*	*J2 8*
CFRESET	*O*	*pull-up, 33kΩ*	*CF Reset*	*J2 10*
/CFIOIS16	*I*		*CF I/O Select 16*	*J2 13*
CFREADY	*I*	*pull-up, 33kΩ*	*CF Ready*	*J2 14*
/CFWAIT	*I*	*pull-up, 33kΩ*	*CF Wait*	*J2 15*
/CFDETECT	*I*	*pull-up, 33kΩ*	*CF Card Detect*	*J2 19*
/CFREG	*O*		*CF Register Select*	*J2 20*
/CFBEN	*O*	*pull-up, 33kΩ*	*CF Buffer Enable*	*J2 24*
CPLD System Controller Signals				
Name	**Type**	**Termination On Module (note 7)**	**Description**	**Pin**
/uP_AEN	*O*		*Address Enable*	*P2 142*
/uP_BUFF_OE	*O*		*Data Buffer Output Enable*	*J1 74*
uP_BUFF_DIR_DATA	*O*		*Data Buffer Direction*	*J1 76* *J2 25*
/CFON	*O*		*CF Enable*	*J1 17*
/CF_CE	*O*		*CF Chip Enable*	*J1 61*
/CFCE1	*O*		*CF Low Byte Enable*	*J2 11*
/CFCE2	*O*		*CF High Byte Enable*	*J2 12*
/PCC_CE1A	*O*		*PC Card Chip Enable 1*	*J2 60*
/PCC_CE2A	*O*		*PC Card Chip Enable 2*	*J2 62*
/CHRDY	*I*	*pull-up, 10kΩ*	*Channel Ready*	*P2 22*
/FAST_CS	*O*		*Fast Chip Select*	*P2 6*
/SLOW_CS	*O*		*Slow Chip Select*	*P2 8*

Note:

7. Pull-ups are to 3.3 V unless otherwise specified.

4.5 User Interface and Display

The TurboXb uses the integrated XScale LCD controller to drive liquid crystal displays (LCDs). Connector J1 supplies the control and data signals needed to drive LCDs, while backlight brightness control signals are located on connector J2.

The Eurotech BSP supports an external touch panel controller on XScale SSP2 with a corresponding interrupt signal, /IRQ_TS. Touch panel signals are located on connectors P2, J1, and J2.

4.5.1 Display

Display Type Supported

Eurotech has configured the TurboXb for a wide variety of display types and sizes. Consult the Eurotech support site (section 2.3) for the latest list of displays supported by Eurotech. If a display is not on the list, contact Eurotech Sales for information about Eurotech' panel configuration service.

The XScale controller uses system memory for the display frame buffer and can drive VGA (640x480) and SVGA (800x600) displays easily. Larger displays will work with the XScale, with some constraints imposed by the controller architecture. The Eurotech Support Forums provide details about the design tradeoffs that are required to support larger displays (see Topic ID 580).

Display Signals

The XScale LCD controller provides the interface to drive a flat-panel display. XScale display signals *LDD0* through *LDD17*, as well as the pixel clock, vertical sync, and horizontal sync, are included on connector J1 (section 3.2.2). These signals connect directly to the XScale processor; therefore, they should be externally buffered and EMI/RFI filtered before reaching the display. See section 6.4.2 for electrical specifications.

The TurboXb uses two XScale GPIOs to control power to the display. GPIO95 configured as /PANEL_ON controls the power to the display and external panel buffers. GPIO94 is used as the panel enable to the display, UBUFF_PNL_ENA. Both signals are included on connector J2 at pin 35 and pin 34 respectively (section 3.2.3). See section 6.4.2 for the electrical specifications for XScale GPIO signals.

4.5.2 Creating LCD Display Cables

Eurotech has designed cables for a wide variety of displays. See the list of supported displays on the Eurotech support forums. Cable drawings for supported displays are available on request.

While Eurotech does not provide support to customers to create their own cables, designers with LCD experience may be able to design their own. For those that do so, a key point to keep in mind is that the XScale LCD interface maps its display controller pins differently based on LCD technology and color palette size.

The following table illustrates how they are mapped for some of the more common technologies. Consult the PXA270 User's Manual for more information (Intel PXA27x Processor Family: Developer's Manual. Order number 280000-001, April 2004. pp. 7-49 to 7-53).

XScale Signal Name	Color Active			Color Passive			Mono Passive			
	18-bit	16-bit	12-bit	Dual		Single	Dual		Single DPD	Single
LDD0	B0	B0	B0	DU0	top	D0	DU0	top	D0	D0
LDD1	B1	B1	B1	DU1		D1	DU1		D1	D1
LDD2	B2	B2	B2	DU2		D2	DU2		D2	D2
LDD3	B3	B3	B3	DU3		D3	DU3		D3	D3
LDD4	B4	B4		DU4		D4	DL0	bottom	D4	not used
LDD5	B5	G0	G0	DU5		D5	DL1		D5	
LDD6	G0	G1	G1	DU6		D6	DL2		D6	
LDD7	G1	G2	G2	DU7		D7	DL3		D7	
LDD8	G2	G3	G3	DL0	bottom	not used				
LDD9	G3	G4		DL1						
LDD10	G4	G5		DL2						
LDD11	G5	R0	R0	DL3						
LDD12	R0	R1	R1	DL4						
LDD13	R1	R2	R2	DL5						
LDD14	R2	R3	R3	DL6						
LDD15	R3	R4		DL7						
LDD16	R4									
LDD17	R5									
L_PCLK	PCLK			PCLK						
L_LCLK	HSYNC			LCLK						
L_FCLK	VSYNC			FCLK						
L_BIAS	DE			LBIAS						

Note: Double pixel data (DPD) mode = 1

4.5.3 Developing Display Drivers

The XScale has a bank of registers that define the timing for displays. In addition, the operating system must define the region of memory for the frame buffer(s).

Eurotech provides display timings for supported displays on request. For displays not yet supported, Eurotech has a panel configuration service to create panel timings and cable drawings. Contact Eurotech Sales for further details.

4.5.4 Brightness Control (Backlight)

Most LCDs include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Some LCDs, such as passive transflective displays, can be viewed in daylight without backlighting.

Backlight inverters drive the panel backlights. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. Fortunately, most backlight inverters include control signals to dim and turn off the backlight.

The TurboXb supplies two signals for backlight control, BCKPWM and Backlight_On/OFF, on connector J2 pin 69 and pin 36 respectively (section 3.2.3). XScale GPIO80, configured as BCKPWM, is a pulse width modulation signal supplying an analog output voltage to control the intensity of the backlight. XScale GPIO100 configured as Backlight_On/OFF switches the backlight on and off. See section 6.4.2 for electrical specifications.

4.5.5 Contrast Control (Vee)

VEEPWM, located on J2 pin 68, controls the contrast of passive panels. Many passive panels require a positive or negative bias voltage in the range of fifteen to thirty volts to bias the passive LCD display.

Some displays include a Vee generator and simply require a low-voltage analog signal to control the contrast. VEEPWM, implemented by XScale GPIO17, is a pulse width modulated output used for this purpose. Electrical specifications are given in section 6.4.2.

4.5.6 Touch Panel

The TurboXb supports an external touch panel controller on XScale SSP2. See section 4.4.5 for details on the synchronous serial ports. In addition, the XScale GPIO22 signal acts as the touch panel interrupt, /IRQ_TS. The signals supporting the touch panel are located on connectors P2, J1 and J2 (section 3.2). See section 6.4.2 for electrical specifications.

4.6 Audio

The XScale processor includes an AC ’97 controller supporting the Audio Codec ’97 Component Specification, Revision 2.0. Intel developed the AC ’97 specification to implement audio and modem IO functionality in mainstream computer systems. The specification defines the interface used to transfer digital audio, modem, microphone input, register control, and status information between the XScale and an external AC ’97 Codec. The XScale receives digitized audio samples from the AC ’97 Codec and stores them in memory. For playback or synthesized audio, the XScale retrieves stored audio samples and sends them to the AC ’97 Codec. The AC’97 Codec then converters the audio sample to an analog audio waveform for output through an audio amplifier. The digital AC-link used in the transfer is a synchronous, fixed-rate, full-duplex serial bus.

The AC ’97 controller, as configured on the TurboXb, supports the following AC ’97 features:

- Hardware support of 16-bit samples and software support of less than 16-bit samples on five independent channels that include stereo pulse code modulation (PCM) in, stereo PCM out, modem out, modem-in, and mono microphone in.
- Multiple sample rate AC ’97 2.0 Codecs operating at up to 48 kHz. The external Codec controls the varying rate.
- Read/write access to AC ’97 registers
- Three 32-bit, 16 entries receive FIFOs
- Two 32-bit, 16 entries transmit FIFOs

The AC’97 signals are located on connector J1 (section 3.2.2) and connect directly to the XScale processor. These signals should be treated electrically as GPIOs. See sections 6.4.2 for electrical specifications.

4.7 EMI/RFI and ESD Protection

The TurboXb incorporates termination on some high-frequency signals as described in this chapter. However, it does not include protection from electrostatic discharge (ESD) or suppression of electromagnetic and radio-frequency interference (EMI/RFI). Devices such as transient voltage suppressors, EMI fences, and filters on I/O lines must be included on the solution board.

4.7.1 Agency Certifications

Many products using Eurotech single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. Because Eurotech supplies only the single-board computer and not fully integrated systems, Eurotech cannot provide meaningful system-level emissions test results.

The crystal frequencies (section 6.4.6) and electrical specifications listed in Chapter 6 may provide helpful information for agency certifications.

4.7.2 Protecting the Power Supply Inputs

It is the responsibility of the designer or integrator to provide surge protection on the input power lines. This is especially important if the power supply wires will be subject to EMI/RFI or ESD.

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5 System Integration

The TurboXb module operates with the Eurotech Solution Board or a solution board specifically designed for your application. Section 4 of this manual details how the TurboXb functions with the Eurotech Solution Board. Refer to this schematic for example implementations of the functionality described.

When integrating the TurboXb with a solution board, designers must address system-level issues such as power management. In addition, a solution board must include certain functionality to support the TurboXb. This section provides details about the XScale power management system and tips about designing a custom solution board.

5.1 Power Management Modes

Power management is especially critical in portable and handheld applications where battery power is at a premium. Handheld and portable systems available today never really turn "off." They make use of power management algorithms that cycle the electronics into "standby" and "sleep" modes but never fully remove power from the full system. This section describes the various power management modes of the XScale processor and how the TurboXb makes use of them.

5.1.1 XScale Power Management Modes

The XScale processor supports four operational modes: Turbo, Run, Idle, and Sleep.

- Sleep mode uses the least amount of electrical power. The processor core is powered off and only a few processor peripherals (RTC, I/Os, and interrupt control) remain active. The transition back to Run mode may take a few hundred milliseconds, as clocks must stabilize and hardware that was powered off must be reinitialized.
- Idle mode reduces power consumption by pausing the processor core clock. Processor peripherals remain enabled. This mode is used for brief periods of inactivity and offers a quick transition back to Run mode.
- Run mode is the standard mode used when applications are running. It offers the best MIPS/mW (performance vs. power) performance when running applications from RAM.
- Turbo mode runs the processor core at up to three times the Run mode speed. Since external memory fetches are still performed at the memory bus frequency, Turbo mode is best used when running the application entirely from cache.

5.1.2 Power Management using the TurboXb

The TurboXb can actively be configured to be in XScale Run or Sleep modes. Turbo and Idle modes are controlled by the operating system and typically are transparent to the application.

In Turbo, Run, and Idle modes, the power supplies are in their standard, full-power state, and applications run normally on the system. The operating system is responsible for adjusting the core voltage (Vddi) for optimal power consumption in each mode. Vddi is a variable-voltage power supply controlled by the XScale I^2C bus. This voltage-scaling feature allows the operating system to manage power consumption over the full range of CPU clock rates.

Several XScale GPIOs function as discrete control signals used to turn off power to various subsystems included on a solution board. This load-shedding feature can extend battery life and significantly reduce power consumption during the Turbo, Run, and Idle modes. Applications and the operating system determine how selective power management is utilized. See the TurboXb Development System Manual for examples of subsystem power management.

In Sleep mode, sometimes called "Suspend" mode, the processor puts the SDRAM in a low-power, self-refresh mode, the processor core shuts off, most peripheral sub-systems are shut down, and the power supplies drop into low-power states or turn off entirely. In the sleep state, the TurboXb consumes very little power, most of which is dedicated to the maintenance of the RAM. See section 6.3.1 for specifications.

System Sleep

Three methods are available to put the system into Sleep mode. These are the /BATT_FAULT input, the /VDD_FAULT input, or software control.

The TurboXb automatically goes in Sleep mode when either of the two inputs, /BATT_FAULT or /VDD_FAULT, are asserted. The /BATT_FAULT input signals that the main system battery is low or removed, while the /VDD_FAULT input indicates that the main system power source is going out of regulation. Both signals are included on connector P2 and are pulled-up on the module.

Applications can put the system to sleep programmatically. Operating systems may also put the system to sleep if the system has not been used for a certain amount of time or for other reasons. In remote, battery-powered applications, software Sleep can be used in conjunction with the Timed Wakeup feature for minimum power consumption.

System Wakeup

Various mechanisms can wake the system from Sleep mode. Three examples, described below, are the /Wakeup input, timed wakeup, and an external event.

Shorting the /WAKEUP signal to ground will wake the system. The signal is connected to the XScale GPIO1 and located on P2 pin 4 or pin 21. If the system was put to sleep with either the /BATT_FAULT or /VDD _FAULT signals, the /WAKEUP input is the only external wakeup source the processor will recognize. Electrical specifications are listed in section 6.4.1.

The XScale can wake up at a predetermined time. Software controls this feature.

The functionality implemented on a solution board can wake the system. For example, an external touch panel controller can interrupt the processor when touch panel events occur. Before going to sleep, the processor can place the controller in a low-power sleep mode from which the controller generates a wakeup interrupt when a touch event occurs.

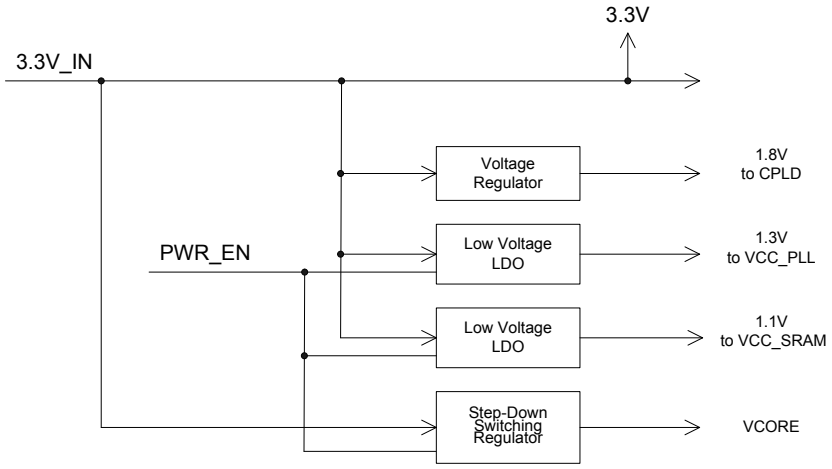
5.2 *Power Management System*

This section provides an overview of the TurboXb power supply architectures including input power requirements and external loads. For specific information about the power supply, consult the electrical specifications in section 6.3

5.2.1 Power Supply Architecture

Power generation is partitioned across the TurboXb and a solution board. The TurboXb module requires a 3.3 V input typically supplied by the solution board. On-board regulators generate the core power and all other powers required by the XScale.

The TurboXb power supply is laid out as shown in the following diagram. In addition to powering on-board circuitry, the 3.3V input is regulated to supply the various XScale voltages.



During Sleep mode, the XScale core power supply enable signal, PWR_EN, disables on-board power supplies. This signal is available on connector J2 pin 74 and can control an external power supply. The output is negated when the system is entering sleep mode.

5.2.2 Create a Power Budget

Embedded system designers using the TurboXb should have a clear understanding of how power usage will be allocated in the system they design. Designers should create a power budget that takes into account the types of devices that are expected to be used with the TurboXb.

Baseline power consumption of the TurboXb is listed in section 6.3.2. Loads on the 3.3 V come from on-board devices and one external device. The TurboXb provides a 3.3 V power output, 3.3V_WRLAN, for an external Ethernet interface.

5.3 Custom Solution Board Design

The TurboXb integrates with a solution board to meet various system requirements. This manual provides the details of how the TurboXb functions with the Eurotech Solution Board and BSP. Designers should use this solution board schematic as a reference design for developing an application-specific solution board.

Many applications will not require all the features implemented on the Eurotech Solution Board. However, certain functions and design considerations are required for reliable operation. The following table lists the functional blocks of the Eurotech Solution Board. Each block is evaluated as required, recommended, or optional. If your application does not require a function, follow the design guidelines given in the table.

Required	Design Guidelines
Dip Switch Inputs	*Include 47kΩ pull-up resistors on SW0 (J2 52) and SW1 (J2 54)*
Recommended	
Reset Switch	*Include external reset input or button*
Wakeup Switch	*Include external wakeup input or button*
Serial Port 3	*Include debug port connector*
Software-Controllable LED	*Include buffer to LED*
Real Time Clock	*Include DS1307 with battery*
CPU JTAG	*Include debug connector*
CPLD JTAG	*Include debug connector*
Optional	
CompactFlash	*Terminate /CFIOIS16 signal*
USB Host	*Terminate USBH_P, USBH_M and USBH_OVR_CRNT*
USB Function	*Terminate USBC_P and USBC_M*
Serial Port 1	*Terminate DSR1T, DCD1T, and RIB1T*
Serial Port 3	*Terminate CTS3T*
Ethernet	*Terminate ETHER_RX+ and ETHER_RX-*
SD/MMC	*Terminate /SD_WP*
Touch panel	*Terminate TS_DOUT*
AC'97 Codec	*Terminate AC97_BITCLK and AC97_SD_IN*

6 System Specifications

6.1 Mechanical Specifications

This section describes the dimensions and mounting of the module.

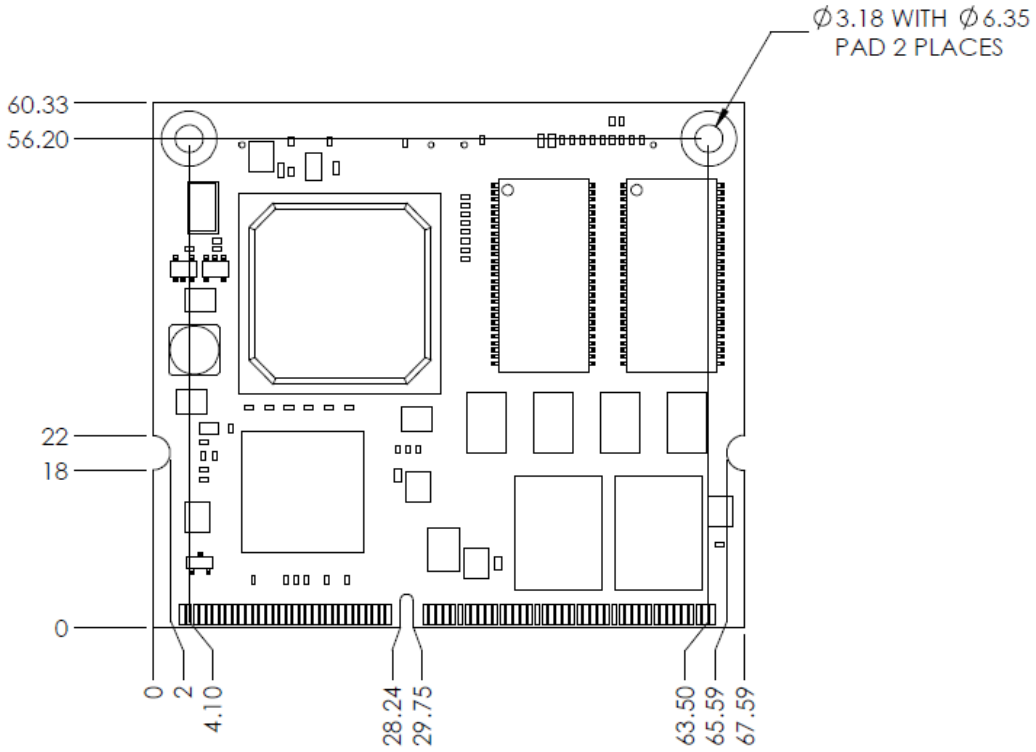
6.1.1 Mounting Holes

Two holes are provided, opposite the card-edge connector, for mounting.

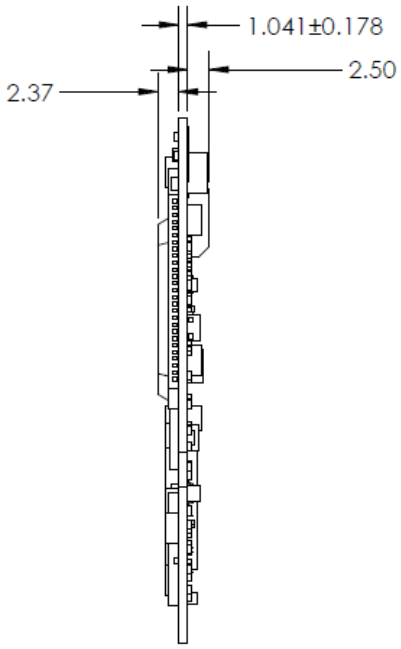
6.1.2 Mechanical Drawing

The mechanical drawings in this section specify the dimensions of the TurboXb, as well as locations of key components on the board. All dimensions are in mm.

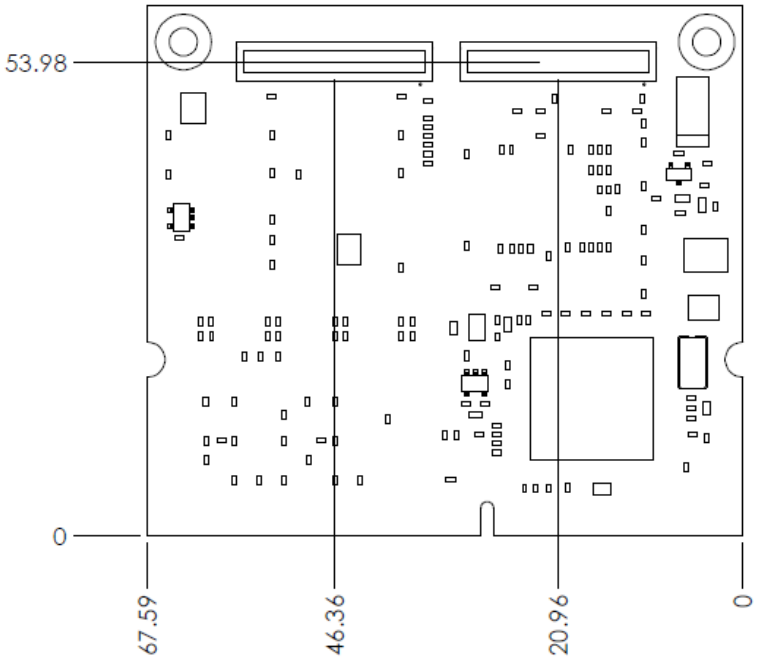
The following drawing illustrates the top view.



The following drawing illustrates the side view. Note that the height of the final assembly also depends on the mechanical constraints of the mating SODIMM card-edge socket.



The following drawing illustrates the bottom view.



6.1.3 Installing and Removing the TurboXb Module

The TurboXb connects to a solution board through two high-density connectors and a card-edge socket. The following procedures describe how to install and remove the module from a solution board.

Important! Observe industry-standard electronic handling procedures when handling the TurboXb module. The headers expose signals on the system bus that do not have ESD protection.

Installing the TurboXb Module

Follow these steps to install a TurboXb module onto a solution board:

1. Connect a grounding wrist strap to your hands.
2. Place the solution board on an ESD mat.
3. Holding the TurboXb module by the edges with the processor facing up and the card at approximately a 30-degree angle, slide it gently into the card-edge slot until the retention levers click.
4. Press downward on the edge of the TurboXb module opposite the card-edge connector to engage the two high-density connectors on the underside of the module.

Removing the TurboXb Module

Follow these steps to detach a TurboXb module from a solution board:

1. Connect a grounding wrist strap to your hands.
2. Place the solution board with TurboXb on an ESD mat.
3. Gently lift the edge opposite the card-edge connector until the TurboXb module releases from the two sockets.
4. Pull the card retention levers slightly away from the TurboXb module.
   The TurboXb will shift slightly and the levers will remain in their extended positions.
5. Holding the TurboXb module by its edges, pull it out of the card-edge slot.

6.2 Environmental Specifications

The following are environmental specifications for the TurboXb module.

Symbol	Parameter	Min	Typ.	Max	Units
	Operating temperature	-40		+85	°C

6.3 Power Specifications

6.3.1 Power Supply

The TurboXb requires a main input power that generates other voltages required by the XScale processor, in addition to powering the on-board circuitry. A synchronous step-down switching regulator generates the XScale core voltage. The XScale processor can change its core voltage, Vddi, dynamically to achieve lower power consumption at high clock rates.

The two modes of operation for the TurboXb are Run and Sleep. During Sleep mode, the XScale PWR_EN signal disables on-board power supplies.

Absolute Maximum Ratings

Supply Voltage (3.3V_IN) .....3.6 V

Symbol	Parameter		Min	Typ.	Max	Units
System Power						
Vin	Supply voltage (note 8)		3.0	3.3	3.6	V
I (Vin)		Run			tbd	mA
		Sleep			tbd	mA
Vsdram	SDRAM voltage (note 9)		3.0	3.3	3.6	V
Vbatt	Battery voltage (note 10)		3.08	3.3	3.6	V
Vddi	Processor core voltage		0.8075	0.85	1.705	V
PWR_EN (note 11)						
Vol	Io max		0		0.3	V
Voh	Io min		Vin – 0.3		Vin	V
Io			-3		3	mA
tpwr_en	(note 12)				10	ms

Notes:

8. On-board components determine this rating.
9. SDRAM determines this rating.
10. The reset circuitry forces /RESET_IN low at Vbatt min.
11. The PWR_EN signal connects to the PXA270, which determines this rating.
12. If PWR_EN is used to disabled the external supply, Vin must be stable within tpwr_en after the signal is asserted.

6.3.2 Power Consumption

Power consumption varies based on the peripheral connections, the level of processor activity, and the LCD and backlight driven. A LCD and backlight adds significantly to the total power consumption of a system. For example, the Sharp LQ64D343 5V TFT VGA display draws about one watt, and the Taiyo-Yuden LS520 backlight inverter draws about six watts at full intensity.

The following table lists typical power consumption for the TurboXb with varying activity levels. The measurements are accurate to ± 5-10%.

Test Condition	Vin = 3.3 V	
Sleep mode	tbd	tbd
CPU idle (note 13)	tbd	tbd
Run mode, max (note 14)	tbd	tbd
Units	mA	mW

Notes: Power consumption was measured on a rev A TurboXb Development System with no peripheral connections and the following additional conditions:

13. System in Run mode at 104 MHz. Running Linux, the system is predominantly in Idle mode (<5% CPU utilization).
14. System in Run mode at 520 MHz, running Linux. Full (95-100%) processor utilization achieved by running multiple instances of a graphics-intensive application.

6.4 Electrical Specifications

This section provides electrical specifications for the TurboXb.

6.4.1 Reset, Wakeup

The /RESET_IN signal located on connector P2 can function as either an input or an output. In addition to an external source, reset circuitry located on the TurboXb activates this signal. The reset circuitry monitors the 3.3V_IN input and forces the signal low when the voltage falls below a threshold voltage.

The /WAKEUP signal connects to the XScale GPIO1 pin and is used to wake the system from sleep mode.

Absolute Maximum Ratings

Reset, Wakeup Inputs (/RESET_IN, /WAKEUP)..... 3.4 V (note 15)

Symbol	Parameter	Min	Typ.	Max	Units
/RESET_IN					
Vrst	Trigger voltage (note 16)		3.08		V
trst	Reset pulse duration (note 17)	140	240	560	ms
Vprst	Pull-up voltage		3.3		Vbatt
Rprst	Pull-up resistance		10		kΩ
/WAKEUP					
Vpwkup	Pull-up voltage		3.3		Vbatt
Rpwkup	Pull-up resistance		33		kΩ
twkup	Wakeup pulse duration (note 18)	100			ms

Notes:

15. The /RESET_IN and /WAKEUP signals are connected to the PXA270, which determines this rating.
16. The reset circuitry forces /RESET_IN low at this voltage.
17. /RESET_IN signal remains low for trst after 3.3V_IN rises above Vrst.
18. A low-level voltage on /WAKEUP for at least twkup initiates wakeup.

6.4.2 PXA270 Processor

Section 4.1.3 lists all XScale GPIOs used on the TurboXb. Some signals include pull-up or pull-down resistors as given in the GPIO cross reference while many connect directly to the PXA270. No ESD/RFI protection is included.

Absolute Maximum Ratings

Input voltage, digital I/O pins.....3.4 V

Symbol	Parameter	Min	Typ.	Max	Units
Vddx		3.0	3.3	3.6	V
Digital Outputs					
Vol		0		0.3	V
Voh		Vddx – 0.3		Vddx	V
Io		-3		3	mA
Digital Inputs					
Vil		-0.1		0.2 * Vddx	V
Vih		0.8 * Vddx		Vddx + 0.1	V
I2C Bus (SDA, SCK)					
	Bus clock (note 19)	100		400	kHz
	Buffer size			1	byte

Notes:

19. The PXA270 supports "standard" and "fast" I2C speeds of 100 and 400 kHz.

6.4.3 Expansion Bus Buffers

Several XScale external memory bus signals are buffered on the TurboXb before reaching the connectors. These buffered signals include uP_MD(0..31), uP_MA(0..25), /uP_MRD, /uP_MWR, and /uP_IOWR.

Absolute Maximum Ratings

Input voltage, digital I/O pins.....6.5 V

Symbol	Parameter	Min	Typ.	Max	Units
Buffered Outputs					
Vol	V_{cc}=3 V, I source max			0.8	V
Voh	V_{cc}=3 V, I source min	2			V
I source		-12		12	mA
Rs	Internal series resistance		26		Ω
tpd		1.5		4.8	ns
Buffered Inputs					
Vil	V_{cc}=2.7 V to 3.6 V			0.8	V
Vih	V_{cc}=2.7 V to 3.6 V	2.0			V

6.4.4 System Controller

A Xilinx XC2C64A CPLD on the TurboXb manages several system control signals. Section 4.3 lists these signals including whether termination is included. The CPLD is programmed at the factory using the CPLD JTAG interface.

Absolute Maximum Ratings

Input voltage, digital I/O pins..... -0.5 to 4.0 V

Symbol	Parameter	Min	Typ.	Max	Units
Vcc	Supply voltage for internal logic and input buffers		1.8		V
Vccio	Supply voltage for output drivers	3.0	3.3	3.6	V
Digital Outputs					
Vol	I source max			0.4	V
Voh	I source min	Vccio-0.4			V
I source		-8		8	mA
Digital Inputs					
Vil		-0.3		0.8	V
Vih		2.0		3.9	V

6.4.5 Ethernet

An Ethernet controller, SMSC LAN9116, provides 10/100BT Ethernet capability on the TurboXb module. This device includes a built-in IEEE 802.3 physical layer for twisted pair Ethernet applications. In addition to the analog I/O, the LAN9116 provides two signals configured as open-drain outputs to drive external LEDs.

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	Supply voltage	3.0	3.3	3.6	V
Analog I/Os					
V+	with respect to ground			6	V
V-	with respect to ground	-0.5			V
Open-drain Outputs					
Vol				0.4	V
Iol				12	mA

6.4.6 Crystal Frequencies

Agencies certifying the TurboXb for compliance for radio-frequency emissions typically need to know the frequencies of on-board oscillators. The following table lists the frequencies of all crystals on the TurboXb.

Crystal	Device	Typ.	Units
XT1	XScale core	13.000	MHz
XT2	XScale RTC	32.768	kHz
Y3	Ethernet	25.000	MHz

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7 Board Revision History

7.1 Identifying the Board Revision

The product revision number of the TurboXb module is printed on the solder mask located on the component side, along the edge of the board.

7.2 TurboXb Module Revision History

The following is an overview of the revisions to the TurboXb module.

7.2.1 Revision 3

Prototype

7.2.2 Revision A

Initial release

Revision A corresponds to the product revision number PXA270 card engine v1.3.1.

Changes

AC ’97 codec removed.

Core voltage power supply added.

7.2.3 Revision B

Changes

Signals on P2 changed, as listed in the following table.

Pin	From	To
20	*BALE*	*Reserved*
38	*MODE3*	*n/c*
40	*MODE2*	*n/c*
44	*MODE0*	*n/c*
61	*3.3V_BATT*	*3.3V_IN*
62	*3.3V_SDRAM*	*3.3V_IN*
63	*3.3V_SDRAM*	*3.3V_IN*
64	*3.3V_SDRAM*	*3.3V_IN*
74	*/uP_MWE3*	*n/c*
76	*/uP_MWE2*	*n/c*
78	*/uP_MWE1*	*n/c*
80	*/uP_MWE0*	*uP_RD_/WR*

Signals on J1 changed, as listed in the following table.

Pin	From	To
62	*GPIO53*	*uP_PCC_RDYA*

Signals on J2 changed, as listed in the following table.

Pin	From	To
61	*PWM_OUT0*	*n/c*
73	*VCC_USIM*	*n/c*

Termination changed, as listed in the following table.

Pin	Signal	From	To
P2 37	*/uP_WAIT*	*pull up, 4.75kΩ*	*pull up, 4.7kΩ*
J1 62	*uP_PCC_RDYA*	*pull up, 33kΩ*	*pull up, 10kΩ*
J1 67	*/USBC_OVR_CRNT*	*pull down, 150Ω*	*pull down, 1kΩ*
J2 6	*/CFWE*	*pull up, 33kΩ*	*pull up, 4.7kΩ*
J2 56	*/SD_CD*	*none*	*pull-down, 33kΩ*
J2 63	*I2C_SCL*	*pull up, 10kΩ*	*pull up, 1.2kΩ*
J2 64	*I2C_SDA*	*pull up, 10kΩ*	*pull up, 1.2kΩ*

Termination added on RXD1T (pull up, 33kΩ) and CTS1T (pull down, 33kΩ).

Termination added on RXD3T (pull up, 33kΩ) and RTS3T (pull down, 33kΩ).

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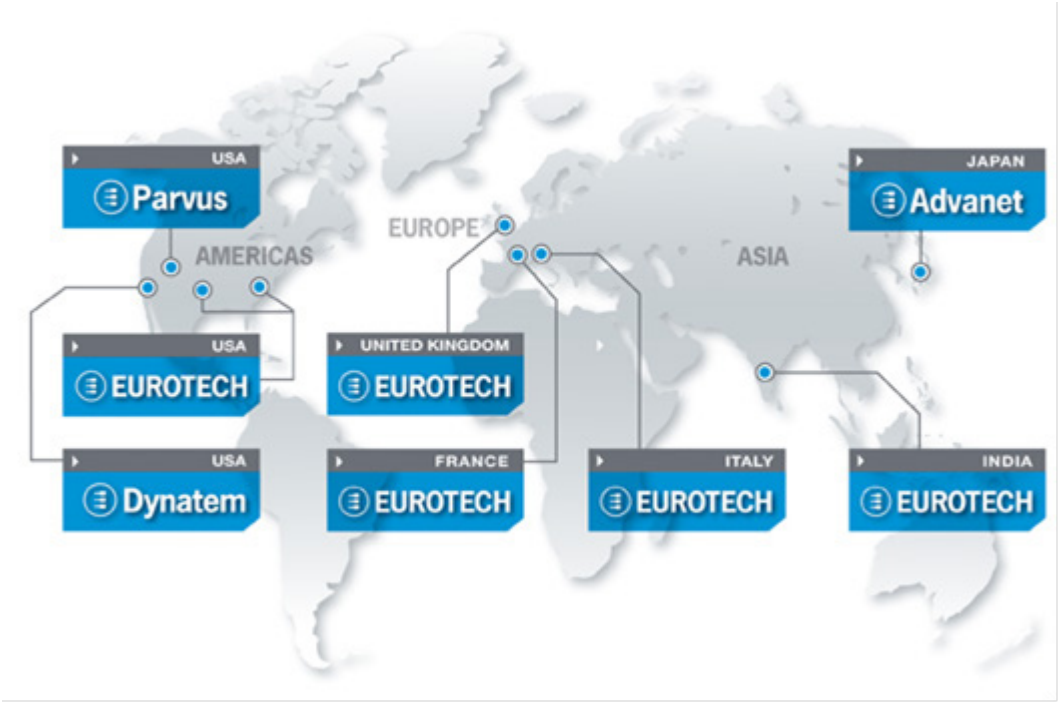

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