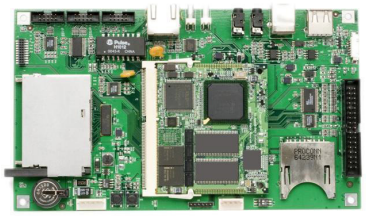
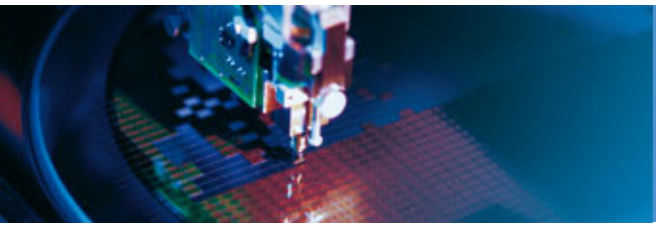
USER MANUAL





TurboXb

PXA270 Development System

Rev A – July 2011 – 110130-1001A

www.eurotech.com

EUROTECH
Imagine. Build. Succeed.

Disclaimer

The information in this document is subject to change without notice and should not be construed as a commitment by any Eurotech company. While reasonable precautions have been taken, Eurotech assumes no responsibility for any error that may appear in this document.

Trademarks

All trademarks both marked and not marked appearing in this document are the property of their respective owners.

Revision History

Issue no.	*PCB*	*Date*	*Comments*
1		21-Sep-2006	Preliminary release
2		24-Aug-2007	Second preliminary release
3		28-Aug-2007	Third preliminary release
A		22-Jul-2011	Initial release

For contact details, see page 51.

Contents

Introduction

TurboXb is a full-featured, application-ready module based on the Marvell® PXA270 processor. With unique customization capabilities, the processor module integrates readily with a wide range of application-specific solution boards to meet customers' specific design requirements. TurboXb offers an economical, reliable system to get product to market effectively and efficiently.

This manual describes the TurboXb development system and is intended for software application developers and system integrators. A system-level overview of the TurboXb module is provided in this manual. For a full description of the module and its features, refer to the TurboXb Module User's Manual.

The TurboXb development system consists of the following components:

- Solution board with a TurboXb module installed
- Flat panel display and cable
- Backlight inverter and cable
- Touch panel and cable
- 100-240 VAC power adapter
- Plexiglas mounting
- Developer's cable kit including
  - Serial port DB9 adapter (Eurotech cable #610111-80001)
  - DB9F/F null modem cable
  - USB A-B cable
- Operating system of your choice
- User's Guide (this document and operating system guide)

Please make sure you have received ***all*** the components before you begin your development.

Handling Your Board Safely

Anti-static Handling

The TurboXb module and solution board contain CMOS devices that could be damaged by electrostatic discharge (ESD). Observe industry standard electronic handling procedures when handling the board. Where possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the board or touching any components on the board.

Packaging

Please ensure that, should a board need to be returned to Eurotech, it is adequately packed, preferably in the original packing amterial.

Electromagnetic Compatibility (EMC)

The TurboXb development system is classified as a component with regard to the European Community EMC regulations and it is the user's responsibility to ensure that systems using the board are compliant with the appropriate EMC standards.

RoHS Compliance

The European RoHS Directive (Restriction on the use of certain Hazardous Substances – Directive 2002/95/EC) limits the amount of six specific substances within the composition of the product.

The TurboXb development system is available in both RoHS compliant and non-RoHS configurations. A full *RoHS Compliance Materials Declaration Form* for the TurboXb development system is included as Appendix B – RoHS Compliance, page 47. Further information regarding RoHS compliance is available on the Eurotech web site at www.eurotech.com.

Conventions

The following table lists the symbols that are used in this manual.

Symbol	Explanation
	Note – information that requires your attention
	Warning – proceeding with a course of action may damage your equipment or result in loss of data

The following table describes the conventions that specify signal names.

Convention	Explanation
GND	digital ground plane
#	active low signal
+	positive signal in differential pair
-	negative signal in differential pair

The following table describes the abbreviations that specify the signal types.

Type	Explanation
I	signal is an input to the system
O	signal is an output from the system
IO	signal may be input or output
P	power and ground
A	analog signal
OD	open-drain
nc	no connection
reserved	use is reserved to Eurotech

Some signals include termination on the TurboXb module or solution board. The following table describes the abbreviations that specify the signal termination.

Termination	Explanation
PU	pull-up resistor to the specified voltage
PD	pull-down resistor
R	series resistor

TurboXb Features

TurboXb Development System

Processor

- PXA270 processor
- Clock rates from 104 to 520 MHz
- Voltage and frequency scaling

Memory

- 64 MB synchronous DRAM
- 32 MB Flash memory
- Battery-backed real-time clock
- External memory support
  - CompactFlash, Type I and II, 3.3 V and 5 V
  - USB disk drive
  - SD/MMC card

Communications

- Two Universal Serial Bus ports
  - USB 1.1 Host port supporting low and full speeds
  - Client port supporting full speed
- Three serial ports
  - Serial 1: EIA-232 or optional 3.3 V, 9-wire
  - Serial 2: EIA-232 or optional 3.3 V, 3-wire
  - Serial 3: EIA-232 or optional 3.3 V, 5-wire
- 10/100 Mbps Ethernet
- Synchronous Serial Port
- Secure Digital and MultiMediaCard interface
- I^2C bus with I^2C master device

User Interface and Display

- Flat panel interface
- Backlight interface with control signals for intensity and on/off
- Resistive touch panel interface, 4-wire or optional 5-wire

Audio Interface

- AC '97 codec
- Stereo microphone input
- Stereo speaker outputs, 2 x 1W
- Stereo headphone output

Power Supply

- 5 V main power input
- Backlight power input

Mechanical

- 180 mm x 105 mm dimensions

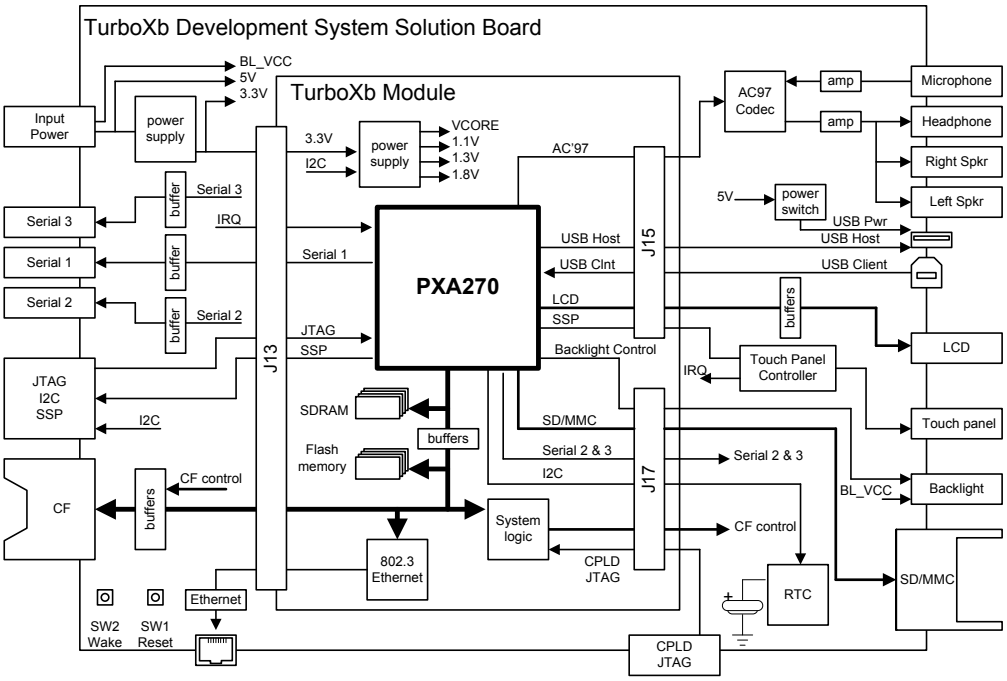
Environmental

- Operating temperature
  - Industrial: -40°C to +85°C

Hardware Specification

Block Diagram

The following diagram illustrates the system organization of the TurboXb development system. Arrows indicate the direction of control and not necessarily signal flow.



Core Processor

The TurboXb is a full-featured, application ready module based on the PXA270 processor.

Boot Code

The TurboXb module uses the first block of on-board flash to store the boot code. At the factory, boot code is loaded using the JTAG interface. Most Eurotech TurboXb boot loaders are field-upgradeable using a flash card on the CompactFlash socket.

Interrupts

Several internal interrupts are used on the TurboXb development system. However, the solution board does not provide any external interrupts.

Memory

The TurboXb module combined with the solution board provides a variety of storage capabilities. The following sections describe the different types of memory available on the TurboXb development system.

Synchronous DRAM

Synchronous DRAM (SDRAM) is included on the TurboXb module for kernel, application, and display frame buffer use. The standard memory configuration is 64 MiB. Other memory configurations are available as a volume production option. Data bus width supports 32-bit accesses while allowing access to individual bytes via the PXA270 data mask function. Typical memory bus operation is at 99.5 MHz. Notice that the memory clock speed is one-half the CPU core clock speed.

Non-volatile Memory

Non-volatile memory included on the TurboXb development system supports application data storage and a real-time clock function.

Flash memory is the primary site for non-volatile data storage on the TurboXb module. The standard configuration is 32 MiB with a 32-bit data bus width. Other memory configurations are available as a volume production option. Eurotech systems store the operating system, applications, and system configuration settings in the on-board flash. Most operating systems configure a portion of the flash as a flash disk, which acts like a hard disk drive.

The TurboXb development system uses a real-time clock (RTC) chip to retain the system date and time when the system is powered down. This chip includes 56 bytes of non-volatile RAM that is maintained as long as main or backup power is provided to the chip. A long-life 3 V battery connected to the RTC supplies backup power. See Power Specification, page 39 for RTC backup power specifications.

The operating system typically reads the RTC on boot or on wakeup and sets the RTC when the system time or date is changed. The system communicates with the RTC on the I^2C bus. See I2C Bus, page 15. Drivers are not available to access this feature. Contact Eurotech Sales if your application requires access to the RTC.

External Memory

Three types of external memory interfaces provide mass storage options for the TurboXb development system. The solution board includes a CompactFlash interface, a SD/MMC interface, and an USB Host port that can connect external memory to the system.

CompactFlash cards provide removable storage in a wide variety of capacities. The TurboXb development system supports a Type I and II, 3.3 V or 5 V CompactFlash interface on socket J14. See J14: CompactFlash, page 34. Normally, the socket is de-energized. The operating system is responsible for turning the socket on when a card is inserted and turning it off when the card is removed. This capability can be a cost-effective means to expand system storage.

Next, you can use a SD/MMC card in socket J18 to provide mass storage. See J18: SD/MMC, page 37. For a description of the various modes of operation for the SD/MMC interface, see Secure Digital and MultiMediaCard Interface, page 13.

Lastly, an USB disk drive can connect to the USB Host port on the solution board. Any USB device that has USB drivers installed on TurboXb module can connect to this port. See Universal Serial Bus, page 12 for details about the USB Host port.

Communications

The TurboXb development system has several industry-standard channels for communication with peripheral and peer devices. These include USB ports, serial ports, Ethernet, a SD/MMC interface, a synchronous serial port, and an I^2C bus.

Universal Serial Bus

The TurboXb development system provides two Universal Serial Bus (USB) ports. The USB Host port supports the USB 1.1 specification operating at low (1.5 Mbps) and full (12 Mbps) speeds, while the USB Client port supports full speed. The PXA270 processor manages both the USB Host port and the USB Client port. This capability enables the TurboXb development system to operate as a self-powered hub, with one Host and one Client port.

One USB device can connect directly to the TurboXb development system using the USB Host port. The Type A USB connector J9 provides the host signals. See J9: USB Host, page 31. USB mouse and keyboard are the most common client devices, but you can connect any USB client device that has USB drivers installed on the TurboXb development system. Use a USB Hub to connect more than one USB client device.

The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The TurboXb development system supplies 5 V power to the USB Host port through a power switch with over-current detection. Make sure to account for power used through USB in your power budget.

The TurboXb development system includes one full speed USB Client port. This interface allows the TurboXb development system to appear as a client device to USB Host devices such as desktop and laptop computers. The USB Client port is available on the Type B USB connector J10. See J10: USB Client, page 32.

USB client devices are self-powered or can receive power from the host computer. Since the USB cable does not power the TurboXb development system, the USB Client port does not need a power input. However, the USB input power is useful for sensing when a USB cable is connected. Circuitry on the solution board senses a connection and interrupts the PXA270 processor.

Serial Ports

External interfaces to the three PXA270 serial ports are included on the TurboXb development system. The following table describes these serial interfaces.

Port	# signals	Header	Production Options
Serial 1	9-wire	J2: Serial 1 (EIA-232), page 29	3.3 V
Serial 2	3-wire	J3: Serial 2 (EIA-232), page 29	3.3 V
Serial 3	5-wire	J1: Serial 3 (EIA-232), page 28	3.3 V

The PXA270 standard UART, Serial 2, and Bluetooth UART, Serial 3, supply two or four signals, respectively. Serial 2 uses TX and RX, while Serial 3 adds RTS and CTS. Serial 1 interfaces to the PXA270 Full-function UART, which adds four more signals (DTR, DSR, DCD, and RI) to supply the full complement of modem control signals.

Standard TurboXb development systems include EIA-232 transceivers on the three PXA270 serial ports. The PXA270 processor has the capability to shutdown the transceivers. Ferrite beads are included on all signals for EMC suppression.

Individual ports can be configured for 3.3 V logic levels as volume production options. Serial ports configured for 3.3 V logic level operation connect to the processor through series resistors and should be treated as digital I/Os. For PXA270 processor specifications, see PXA270 Processor, page 41.

Ethernet

An Ethernet controller located on the TurboXb module provides 10/100 Mbps Ethernet capability. The solution board completes the Ethernet circuit providing a magnetic transceiver and the RJ-45 socket J6. See J6: Ethernet, page 30.

Secure Digital and MultiMediaCard Interface

The Secure Digital and MultiMediaCard (SD/MMC) interface enables mass storage and I/O expansion. Connector J18 connects to the TurboXb module SD/MMC interface. The PXA270 processor drives this interface and controls power to this socket. See J18: SD/MMC, page 37. ESD protection is included on all signals.

This interface supports Secure Digital Memory (SD), Secure Digital I/O (SDIO), MultiMediaCard (MMC), and synchronous serial (SPI) modes of operation. SD and SDIO cards can run in 4-bit, 1-bit, and SPI modes. MMC cards run in 1-bit or SPI modes. This manual lists the signals for use in 4-bit SDIO mode.

The following table illustrates how the signals are mapped differently depending on the mode of operation. Signal names and types denote the direction of the signal relative to the TurboXb. Notice that the Secure Digital standard references SPI-mode signals with respect to the card. Pin 2 of the SD header is listed as "Data In". This manual and PXA270 documents reference the signals with respect to the socket. Pin 2 is listed as "Data Out".

SD Socket		TurboXb Name	Description					
Pin	Name		4-bit Mode		1-bit Mode		SPI Mode	
1	DAT3	SD_DAT3	Data 3	IO	unused	-	/MMC_CS1	O
2	CMD	SD_CMD	Command	IO	Command	IO	Data Out	O
3	VSS1	ground	-	P	-	P	-	P
4	VDD	SD_PWR	-	PO	-	PO	-	PO
5	CLK	SD_CLK	Clock	O	Clock	O	Clock	O
6	VSS2	ground	-	P	-	P	-	P
7	DAT0	SD_DAT0	Data 0	IO	Data	IO	Data In	I
8	DAT1	SD_DAT1	Data 1	IO	Interrupt	I	Interrupt	I
9	DAT2	SD_DAT2	Data 2	IO	unused	-	/MMC_CS0	O

Notice that in SPI mode, pin 9 of an SD/MMC card is unused. Chip Select 0 is shown in this row to illustrate the alternate signal mapping to SD_DAT2.

Some SD sockets supply the following signals, which are not part of the SD/SDIO standard. These signals are connected on socket J18.

SD Socket Pin	TurboXb Name	Description	Type
10	/SD_CD	Card Detect	I
11	/SD_WP	Write Protect	I

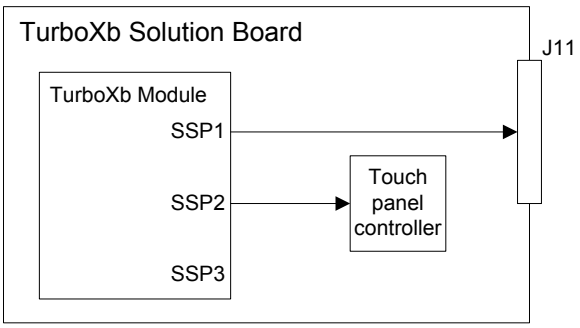
Operating system drivers may not be available for all modes of operation. Contact Eurotech for driver availability for the operating system that you are using.

Synchronous Serial Ports

Synchronous serial port (SSP) standards share the same simple architecture: a clock line, transmit and receive lines, ground, and one or more device selects. Each device on the bus requires its own select line. Buses may be full or half-duplex, clocking data one or both directions at the same time, respectively. Each standard defines which devices are bus masters and which are slaves.

To clarify direction of the data signals, the SSP bus master transmit line (TXD) is also known as MOSI (Master Out, Slave In), while its receive line (RXD) is known as MISO (Master In, Slave Out). The Slave Select (SS) signal, which enables the slave device's transmitter, is known as FRM also.

The TurboXb development system uses two PXA270 synchronous serial ports as illustrated in the following diagram.

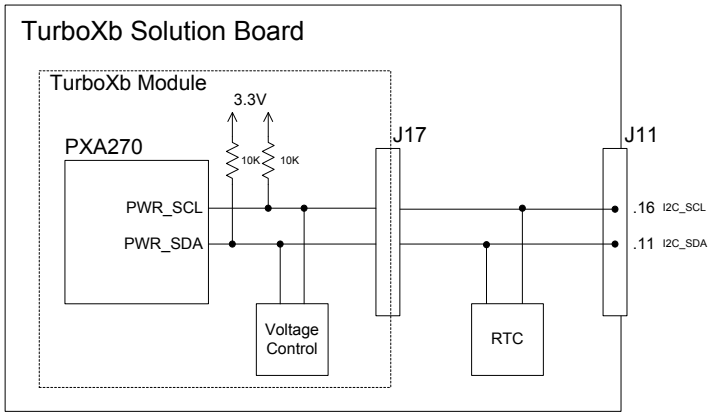


PXA270 SSP2 communicates with the touch panel controller. Applications can use SSP1 for control of external peripherals on connector J11. See J11: Processor JTAG, I2C, and SSP, page 33. The TurboXb module generates the SSP bit clocks from the on-board 13 MHz clock. It does not support an external clock input. For electrical specifications, see PXA270 Processor, page 41. Consult the operating system references for details about how to use the SSP bus for external devices. Notice that SSP3 is not available for use.

I²C Bus

I²C (Inter-IC) is a multi-master, two-wire synchronous serial bus for communications between integrated circuits and for addressing peripherals in a system. The bus master addresses devices using the data line and provides a synchronous clock for reading and writing devices. Client devices respond only when queried by the master device. The TurboXb development system uses the PXA270 processor as the I²C bus master to communicate with the RTC and the CPU core voltage controller. In addition, connector J11 includes an external connection to the I²C bus. See J11: Processor JTAG, I2C, and SSP, page 33. For electrical specifications, see PXA270 Processor, page 41.

The following diagram illustrates the I²C architecture on TurboXb development system. Notice that the TurboXb module includes 10kΩ pull-up resistors on the I²C bus.



The following table lists the addresses of the I²C devices.

Device	Address	Function
DS1307	1101 000	Real-time clock
LTC1663	0100 000	Voltage control

The DS1307 supports a maximum bit rate of 100 kbps. Do not use the I²C bus at rates faster than 100 kbps.

User Interface and Display

The TurboXb development system uses the integrated PXA270 display controller to drive liquid crystal displays (LCDs). Connector J16 supplies the power, control, and data signals needed to drive LCDs, while backlight and touch panel signals are located on headers J12 and J21, respectively. See Display and Backlight, page 42 for electrical specifications of the LCD interface and backlight signals, and see Touch Panel Controller, page 43 for electrical specifications of the touch panel interface.

Display

Eurotech has configured the TurboXb development system for a wide variety of display types and sizes. Consult the support site for the latest list of displays supported by Eurotech. If a display is not on the list, contact Eurotech Sales for information about Eurotech's panel configuration service.

The PXA270 controller uses system memory for the display frame buffer and can drive VGA (640x480) and SVGA (800x600) displays easily. Larger displays will work with the PXA270, with some constraints imposed by the controller architecture. The Eurotech Support Forums provide details about the design tradeoffs that are required to support larger displays.

The TurboXb development system supplies the power, control, and data signals required to drive LCDs on connector J16. See J16: LCD, page 35. The system supports LCDs operating at 3.3 V or 5 V. One of two resistors selects the supply voltage, as described in the following table.

Resistor	LCD Supply Voltage
R55	3.3 V
R56	5 V (default)

PXA270 display signals LDD0 through LDD15 as well as the pixel clock, vertical sync, and horizontal sync are buffered and EMI/RFI filtered before reaching connector J16. The display signal buffers can operate at either 5 V or 3.3 V. One of two on-board resistors sets the display signal voltage, as described in the following table.

Resistor	Display Signal Buffer Voltage
R99	3.3 V (default)
R100	5 V

The PNL_RL and PNL_UD signals are used for active (TFT) displays that support changing the scan direction. This feature allows the display to be flipped right-to-left (RL) or up-and-down (UD) by changing the voltage on these signals. The following table describes the possible configurations.

Signal	Pull-up Resistor	Pull-down Resistor
PNL_UD	R59 (default)	R57
PNL_RL	R53 (default)	R54

Eurotech has designed cables for a wide variety of displays. See the list of supported displays on the Eurotech support site. Cable drawings for supported displays are available on request.

While Eurotech does not provide support to customers to create their own cables, designers with LCD experience may be able to design their own. For those that do so, a key point to keep in mind is that the PXA270 LCD interface maps its display controller pins differently based on LCD technology and color palette size.

The following table illustrates how the display controller pins are mapped for some of the more common technologies. Consult the PXA270 User's Manual for more information. Notice that Double pixel data (DPD) mode = 1.

PXA270 Signal Name	Color Active			Color Passive			Mono Passive			
	18-bit	16-bit	12-bit	Dual		Single	Dual	Single DPD		Single
LDD0	B0	B0	B0	DU0	top	D0	DU0	top	D0	D0
LDD1	B1	B1	B1	DU1		D1	DU1		D1	D1
LDD2	B2	B2	B2	DU2		D2	DU2		D2	D2
LDD3	B3	B3	B3	DU3		D3	DU3		D3	D3
LDD4	B4	B4		DU4		D4	DL0	bottom	D4	not used
LDD5	B5	G0	G0	DU5		D5	DL1		D5	
LDD6	G0	G1	G1	DU6		D6	DL2		D6	
LDD7	G1	G2	G2	DU7		D7	DL3		D7	
LDD8	G2	G3	G3	DL0	bottom	not used				
LDD9	G3	G4		DL1						
LDD10	G4	G5		DL2						
LDD11	G5	R0	R0	DL3						
LDD12	R0	R1	R1	DL4						
LDD13	R1	R2	R2	DL5						
LDD14	R2	R3	R3	DL6						
LDD15	R3	R4		DL7						
LDD16	R4									
LDD17	R5									
L_PCLK	PCLK		PCLK							
L_LCLK	HSYNC		LCLK							
L_FCLK	VSYNC		FCLK							
L_BIAS	DE		LBIAS							

The PXA270 includes a bank of registers that define the timing for displays. In addition, the operating system must define the region of memory for the frame buffer(s).

Eurotech provides display timings for supported displays on request. For displays not yet supported, Eurotech has a panel configuration service to create panel timings and cable drawings. Contact Eurotech Sales for further details.

Backlight

Most LCDs include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Some LCDs, such as passive transflective displays, can be viewed in daylight without backlighting.

Backlight inverters drive the panel backlights. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. Fortunately, most backlight inverters include control signals to dim and turn off the backlight.

The TurboXb development system provides power to the backlight and software control of backlight intensity and backlight on/off. Power is routed from the input power header J19, through the solution board, and to header J12. See J12: Backlight, page 34. This provides greater flexibility when selecting backlight inverters for an application. Two signals are provided for backlight control on header J12. BACKLIGHT_PWM is a filtered PWM signal from the PXA270 processor that supplies an analog output voltage to control the intensity of the backlight. The BACKLIGHT_ON signal is an open-collector output to turn the backlight on and off.

Contrast Control

Many passive panels require a positive or negative bias voltage in the range of fifteen to thirty volts to bias the passive LCD. Some displays include a VEE generator and require a low-voltage analog signal to control the contrast. The VCON output is a PWM-controlled output used for these purposes. This signal is included on connector J16. See J16: LCD, page 35.

Touch Panel

The TurboXb development system supports 4-wire and 5-wire analog resistive touch panels. The 5-wire controller is a volume production option. A touch screen controller included on the solution board provides the touch panel interface on header J21. All signals are EMI/RFI filtered and include ESD protection. See J21: Touch Panel, page 38.

Audio

The TurboXb development system includes an AC '97 codec for stereo audio input and output. It supports a microphone, speaker, and headphone, as described in the following sections. See Audio, page 43 for electrical specifications of the audio system.

Audio Inputs: Microphone Pre-amps

The TurboXb development system supports the direct connection of a stereo electret microphone to stereo jack J5. See J5: Stereo Microphone Jack, page 30. The audio signals run through pre-amplifiers that low-pass filter and boost the signal before being passed on to the audio codec.

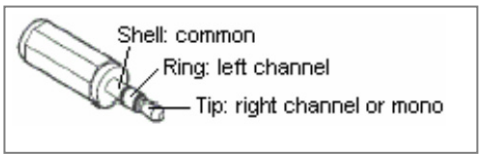
The microphone ground on J5 connects to an analog ground plane on the TurboXb development system for improved signal-to-noise ratio. On-board pull-ups power the electret microphones.

Audio Outputs: Speakers and Headphones

The audio amplifier included on the TurboXb development system supports both differential and single-ended output devices allowing applications to use either stereo headphones or speakers. Differential (or "bridge") drive delivers greater output power and is suitable for speakers, which can be wired independently from each other. Single-ended mode is used for devices like headphones, which have a common ground between output channels.

The TurboXb development system includes two headers to drive a stereo 1W speaker output. See J7: Stereo Speaker: Right Channel, page 31 and J8: Stereo Speaker: Left Channel, page 31. When using the TurboXb development system to drive speakers, the output amplifier operates in differential mode. Connect speakers to the SPKR_L+/- and SPKR_R+/- outputs on J7 and J8.

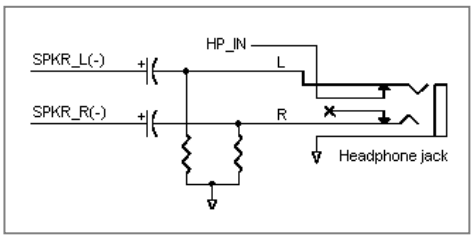
Standard headphones use a plug wired as shown at right. Three rings on the plug provide right and left channels and a common return. Mono headphones do not include the center ring.



The mating headphone jack includes spring contacts to make an electrical connection with the headphone and mechanically hold the plug in place. Some jacks include a mechanical switch suitable for use with the HP_IN signal that activates when a plug inserts into the jack.

The headphone jack J4 included on the TurboXb development system, is wired to automatically switch the amplifier to single-ended mode when a headphone plug is inserted in the jack. See J4: Stereo Headphone Jack, page 30. It includes a mechanical switch that indicates when a headphone plug has been inserted. This will disable the drive to any speakers connected to the system. When the headphone plug is removed, the circuit pulls down the HP_IN signal, enabling differential outputs.

The wiring of J4 is shown at right with wire blocking capacitors in series with the SPKR- signals. These capacitors block the DC component of the audio signal and complete the conversion from differential to single-ended output drive.



The selection of the blocking capacitor size is based on the lowest frequency the application will need to play out. Larger capacitors give improved bass response (lower frequency cutoff) but are physically larger and cost more. The corner frequency for the low-pass filter created by the capacitor and the headphone speaker is calculated as $fo=1/(2\pi R_L C)$. A 330 uF capacitor into a 32 ohm headphone speaker will give a low cutoff frequency of 15 Hz. The TurboXb development system uses 330 uF electrolytic capacitors rated for at least 6.3 V.

The pull-down resistors shown in the diagram drain any charge that builds up on the headphone outputs when headphones are not connected. The TurboXb development system uses 1 kΩ resistors.

Keep in mind that the resulting impedance of the parallel-connected headphone speakers is half that of a single headphone speaker. See Audio, page 43 for details about the minimum impedance an audio output channel can drive.

Power Requirements

Power management is especially critical in high performance systems that also require low power dissipation. Handheld and portable systems available today never really turn "off." They make use of power management techniques that cycle the electronics into power saving modes, but never fully remove power from the full system. This section provides information about power and power management on the TurboXb development system. For a complete description of the PXA270 power management modes, refer to the TurboXb Module User's Manual.

Power Management Modes

The PXA270 supports four operational modes: Turbo, Run, Idle, and Sleep. Applications can configure the TurboXb to operate in Run or Sleep modes. The operating system controls the Turbo and Idle modes, which typically are transparent to the application. Run mode is the standard mode used when applications are running. It offers the best MIPS/mW (performance vs. power) performance when running applications from RAM. Sleep mode uses the least amount of electrical power. During Sleep mode, the processor core is powered off, and only a few processor peripherals remain active.

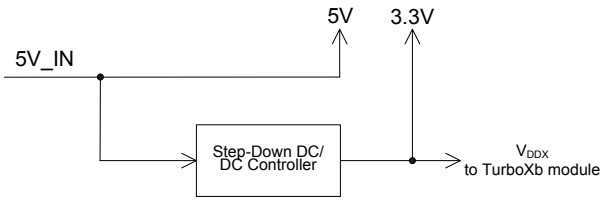
Various methods transition the TurboXb development system into and out of Sleep mode. Applications can put the system to sleep programmatically. Operating systems may also put the system to sleep if the system has not been used for a certain amount of time or for other reasons. In remote, battery-powered applications, software Sleep can be used in conjunction with the timed wakeup feature for minimum power consumption.

The following mechanisms can wake the system from Sleep mode:

- Wakeup switch
  Pressing the wakeup switch SW2 will wake the system.
- Touch panel
  The touch panel controller interrupts the processor when touch panel events occur. Before going to sleep, the processor can place the controller in a low-power sleep mode from which the controller generates a wakeup interrupt when an event occurs.
- Timed wakeup
  The PXA270 can wake up at a predetermined time. Software controls this feature.

Power Management System

The TurboXb development system power supply is designed for high efficiency and low noise. It utilizes a high-efficiency current mode step-down DC/DC controller to regulate the incoming 5 V DC power to 3.3 V. The controller's burst mode is disabled lowering the output noise and reducing both the audio and RF interference. On-board circuitry is powered by both the 5 V input and the regulated 3.3 V, while the TurboXb module is powered by the 3.3 V only. The following diagram illustrates the TurboXb development system power supply.



Power generation is partitioned across the TurboXb module and solution board. The TurboXb module requires a single 3.3V input. Regulators included on the module generate core power and all other powers required by the PXA270. See Power Specification, page 39 for TurboXb development system power supply specifications.

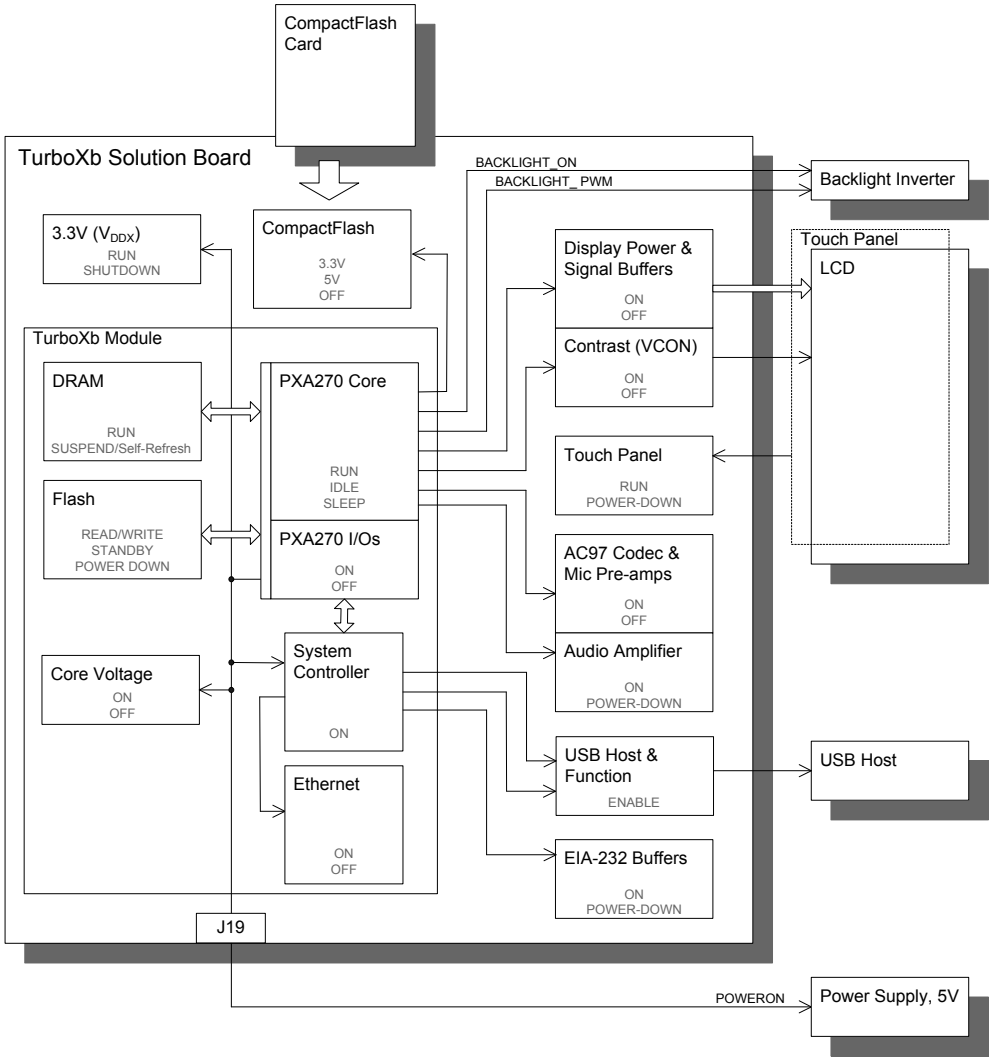
It is the responsibility of the designer or integrator to provide surge protection on the input power lines. This is especially important if the power supply wires will be subject to EMI/RFI or ESD.

The TurboXb development system can selectively turn off power to various subsystems. This load-shedding feature can extend battery life and significantly reduce power consumption. Applications and the operating system determine how selective power management is utilized.

The following are the subsystems that can be disabled selectively:

- LCD (display power and signal buffers)
- Backlight
- Audio output amplifier
- Audio codec and microphone pre-amps
- Serial EIA-232 buffers
- USB ports
- CompactFlash

The following diagram illustrates the architecture of the TurboXb power management system. At the heart of the system is the PXA270 processor that controls the state of the various power subsystems. In the diagram, the power management modes of each subsystem are indicated in gray. Arrows indicate the direction of both signal flow and of power management.



In addition to disabling select subsystems, the TurboXb development system supports sleep operation through control of its on-board peripherals and power supplies. The signal POWERON can control an external power supply. See J19: Input Power, page 37. The system negates this signal when entering Sleep mode. See Power Specification, page 39 for electrical specifications.

Designing for Optimal Power Management

Designing a system for optimal power management requires careful attention to many details. Embedded system designers using the TurboXb development system should have a clear understanding of how power usage will be allocated in the system they design. Designers should create a power budget that takes into account the types of devices that are expected to be used with the TurboXb development system.

Power consumption varies based on the peripheral connections, the level of processor activity, and the LCD and backlight driven. A LCD and backlight adds significantly to the total power consumption of a system. For example, the Sharp LQ64D343 5V TFT VGA display draws approximately one watt, and the Taiyo-Yuden LS520 backlight inverter draws approximately six watts at full intensity.

The following lists detail some of the typical loads placed on the TurboXb development system power supplies. Baseline power consumption of the TurboXb development system is given in Power Specification, page 39.

Typical external loads on the 5 V include the following:

- Display
- CompactFlash cards
- USB devices
- Headphone/Speaker(s)
  Assume 80% efficiency

Typical on-board loads on the 5 V include the following:

- 3.3 V Supply
  Multiply by 115% to account for 3.3 V power supply efficiency

In addition to the TurboXb module, typical external loads on the 3.3 V power supply include the following:

- Display
- CompactFlash cards

When designing systems for minimal power consumption during Sleep mode, make sure to consider DC losses to external connections. The following are a few of the ways your system may "leak" when asleep:

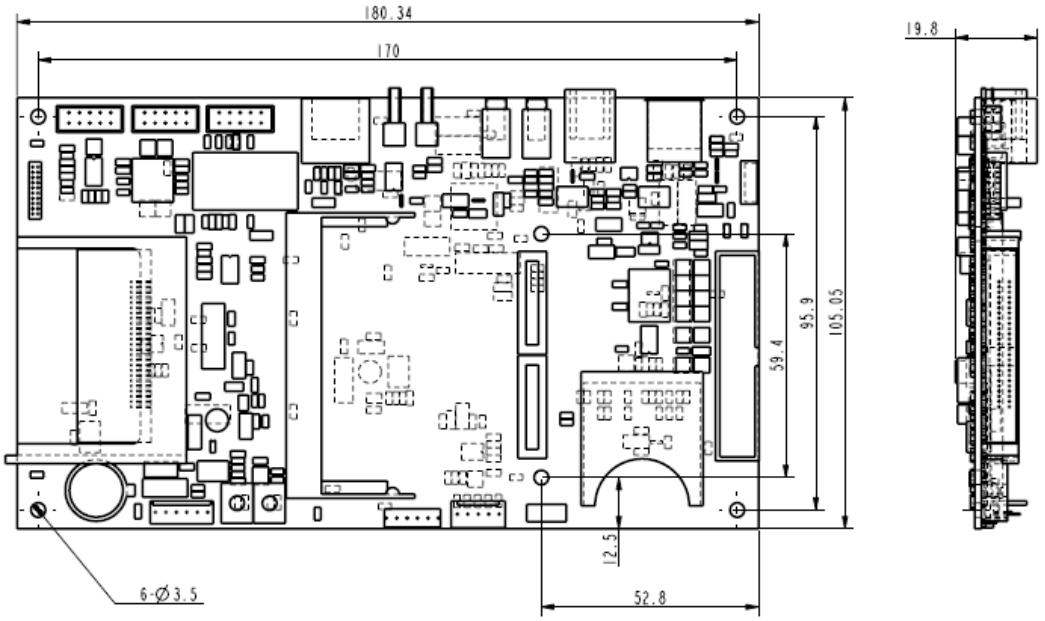
- CompactFlash cards
  Cards in place when the system is asleep can drain power through the Card Detect lines. Assume that the two lines ground the internal pull-ups included on these signals while the card is inserted.
- USB devices
  Depending on how USB devices are powered and how the operating system handles USB, USB devices may draw power during Sleep mode.

Mechanical

The TurboXb development system is 180 mm by 105 mm in size. This section describes the dimensions, mounting, and clearances of the system, in addition to the procedure for handling the TurboXb module.

Mechanical Drawing

The following mechanical drawing specifies the dimensions of the TurboXb development system, as well as locations of mounting holes on the board. All dimensions are in mm.



Mounting Holes

Four holes, one on each corner of the solution board, are provided for mounting. The diameter of the holes is 3.5 mm. Mounting holes are plated through and connected to the ground plane.

For reliable ground connections, use locking washers (star or split) when securing a TurboXb development system in an enclosure. Make sure that washers do not extend beyond the limits of the pads provided.

Clearances

Total height including the highest component on top, board thickness, and highest component on bottom is 19.8 mm. Selection of connectors and wiring harnesses will determine height of final assembly.

Installing and Removing the TurboXb Module

The TurboXb module connects to the solution board through two high-density connectors and a card-edge socket. The following procedures describe how to install and remove the module from the solution board.

Observe industry-standard electronic handling procedures when handling the TurboXb module. The headers expose signals on the system bus that do not have ESD protection.

Installing the TurboXb Module

Follow these steps to install a module onto the solution board:

- Connect a grounding wrist strap to your hands.
- Place the solution board on an ESD mat.
- Holding the module by the edges with the processor facing up and at approximately a 30-degree angle, slide it gently into the card-edge slot until the retention levers click.
- Gently press downward on the edge of the module opposite the card-edge connector to engage the two high-density connectors on the underside of the module.

Removing the TurboXb Module

Follow these steps to remove a module from the solution board:

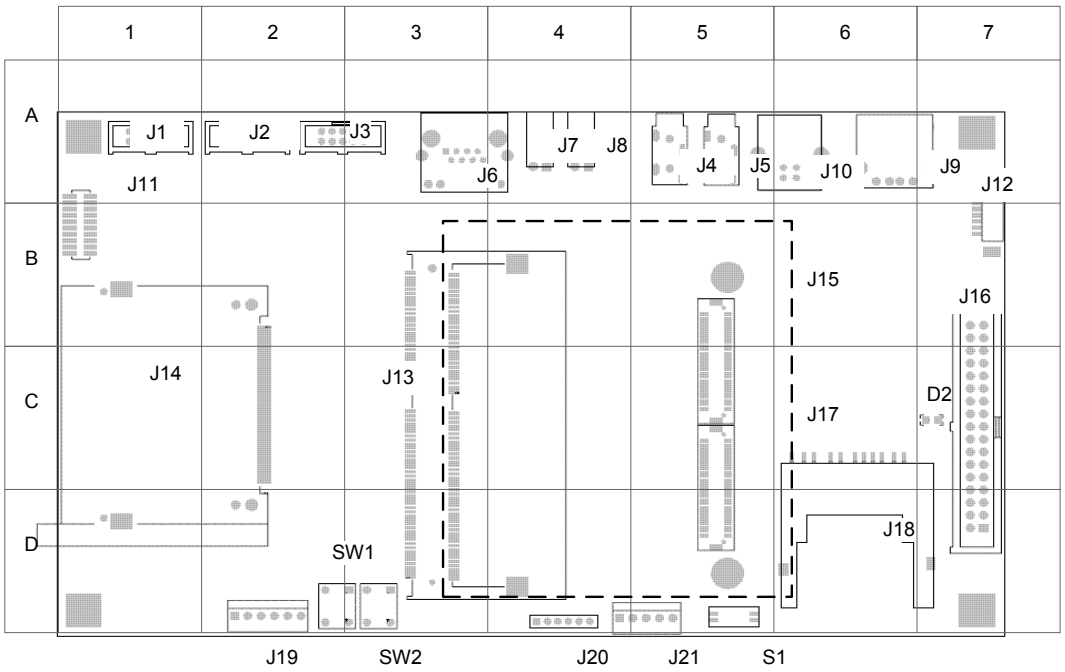
- Connect a grounding wrist strap to your hands.
- Place the solution board on an ESD mat.
- Gently lift the edge opposite the card-edge connector until the module releases from the two sockets.
- Pull the card retention levers slightly away from the module.The module will shift slightly and the levers will remain in their extended positions.
- Holding the module by its edges, pull it out of the card-edge slot.

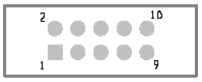
Connectors, LEDs and Jumpers

Identifying Connectors

The following diagram illustrates the location of key components on the TurboXb development system. The TurboXb module is located in the center of the solution board indicated with a dashed line border. Two connectors, J15 and J17, lie under the module.

Components are located based upon the grid overlay of the component side of the solution board. For example, headphone jack J4 lies at location A5, and the CompactFlash socket covers B1 through D2. Component locations given in the following sections refer to this diagram.





The pins of headers and connectors on Eurotech products are numbered sequentially. Most double-row headers place even pins on one side and odd pins on the other. The diagram at right indicates how pins are numbered, as seen from the component side of the board. Connectors J14, J15, and J17 are exceptions and do not follow this numbering.

To locate pin 1 of a connector or jumper, try the following:

- Look for a visible number or marking on the board that indicates connector pin numbering. A notch or dot usually indicates pin 1.
- Look at the underside of the board. The square pad is pin 1.
- Download the mechanical drawing of the TurboXb development system from the Eurotech support site. The square or indicated pad on each connector is pin 1.

Switches, Controls, and Indicators

This section describes various switches, controls, and indicators on the TurboXb development system. The location indicated for each item refers to the grid diagram in Identifying Connectors, page 26.

SW1: Reset

Location on board: D2-D3

SW1 is the reset button for the TurboXb development system. Pressing SW1 shorts the signal RESET_IN# (J11: Processor JTAG, I2C, and SSP, page 33) to ground issuing a hardware reset to the PXA270 processor and system peripherals. Press this button to restart the system without cycling power. See Reset, page 40 for electrical specifications.

SW2: Wakeup

Location on board: D3

SW2 is the wakeup switch for the TurboXb development system. Press this switch to wake the system when in Sleep mode. See Power Management Modes, page 20 for details about Sleep mode.

S1: DIP Switch

Location on board: D5-D6

S1 is a two-position DIP switch. DIP switch positions 1 and 2 connect to the PXA270 processor. When in the ON position, the switches are closed and connect to ground. Otherwise, they are pulled up.

Most operating systems on the TurboXb development system reserve these switches for operating system use. Consult the operating system manual for details.

Software-controlled LED

Location on board: C7

The TurboXb development system includes one green LED controlled by the processor. The same buffer drives LED D2 and the display signal lines. Therefore, LED D2 is off when the display signal buffers are disabled.

Ethernet LEDs

Location on board: A3-A4 (Ethernet socket J6)

The Ethernet LEDs indicate valid Ethernet connection, speed, and bus activity. The Ethernet socket J6 integrates the LEDs with the socket.

Connectors

The following tables describe the electrical signals available on the connectors of the solution board. Each section provides relevant details about the connector including part numbers, mating connectors, signal descriptions, and references to related sections.

The location indicated for each item refers to the grid diagram in Identifying Connectors, page 26. For precision measurements of the location of the connectors on the system, see Mechanical Drawing, page 24.

J1: Serial 3 (EIA-232)

Board connector: 2x5 shrouded header, 2 mm, Samtec STMM-105-01-T-D

Mating connector: TCSD series

Location on board: A1

Header J1 provides the PXA270 Bluetooth UART signals including hardware flow control at EIA-232 levels. See Serial Ports, page 12 for a description of the serial ports.

Pin	Name	Type	Description
1	n/c		
2	n/c		
3	RXD3	I	Receive data 3
4	RTS3	O	Ready to send 3
5	TXD3	O	Transmit data 3
6	CTS3	I	Clear to send 3
7	n/c		
8	n/c		
9	GND	P	ground
10	n/c		

J2: Serial 1 (EIA-232)

Board connector: 2x5 shrouded header, 2 mm, Samtec STMM-105-01-T-D

Mating connector: TCSD series

Location on board: A2

Header J2 supplies the PXA270 Full-function UART signals including hardware flow control at EIA-232 levels. See Serial Ports, page 12 for a description of the serial ports.

Pin	Name	Type	Description
1	DCD1	I	Data carrier detect 1
2	DSR1	I	Data set ready 1
3	RXD1	I	Receive data 1
4	RTS1	O	Ready to send 1
5	TXD1	O	Transmit data 1
6	CTS1	I	Clear to send 1
7	DTR1	O	Data terminal ready 1
8	RIBI	I	Ring indicator 1
9	GND	P	ground
10	n/c		

J3: Serial 2 (EIA-232)

Board connector: 2x5 shrouded header, 2 mm, Samtec STMM-105-01-T-D

Mating connector: TCSD series

Location on board: A2-A3

Header J3 includes the PXA270 Standard UART signals at EIA-232 levels. See Serial Ports, page 12 for a description of the serial ports.

Pin	Name	Type	Description
1	n/c		
2	n/c		
3	RXD2	I	Receive data 2
4	n/c		
5	TXD2	O	Transmit data 2
6	n/c		
7	n/c		
8	n/c		
9	GND	P	ground
10	n/c		

J4: Stereo Headphone Jack

Board connector: 3.5 mm stereo jack, PJ-327

Mating connector: standard stereo plug

Location on board: A5

Stereo jack J4 supports a direct connection to a stereo headphone. See Audio Outputs: Speakers and Headphones, page 19 for details of the operation of the headphone.

Pin	Name	Type	Description
1	GND	P	ground
2	SPKR_R	AO	Headphone, right channel
3	SPKR_L	AO	Headphone, left channel
4	HP_IN	O	Headphone connected

J5: Stereo Microphone Jack

Board connector: 3.5 mm stereo jack, PJ-327

Mating connector: standard stereo plug

Location on board: A5-A6

Stereo jack J5 provides a direct input for a stereo microphone. See Audio Inputs: Microphone Pre-amps, page 18 for a description of the microphone interface.

Pin	Name	Type	Description
1	MIC_GND	P	Microphone ground
2	MIC_R	AI	Microphone, right channel
3	MIC_L	AI	Microphone, left channel
4	n/c		

J6: Ethernet

Board connector: RJ-45 socket with LEDs, Tyco 5569564-1

Mating connector: RJ-45 plug

Location on board: A3-A4

Socket J6 supports a standard 10/100 Mbps Ethernet, RJ-45 port. Shields are tied to chassis ground. See Ethernet, page 13 for details of the Ethernet.

J7: Stereo Speaker: Right Channel

Board connector: 2-pin header, right angle with friction lock, 0.1-inch, Molex 22-05-3021

Location on board: A4

Header J7 includes the signals to drive the right channel of a stereo speaker output. See Audio Outputs: Speakers and Headphones, page 19 for details of the operation of the speakers.

Pin	Name	Type	Description
1	SPKR_R-	AO	Stereo speaker, right channel
2	SPKR_R+	AO	

J8: Stereo Speaker: Left Channel

Board connector: 2-pin header, right angle with friction lock, 0.1-inch, Molex 22-05-3021

Location on board: A4

Header J8 includes the signals to drive the left channel of a stereo speaker output. See Audio Outputs: Speakers and Headphones, page 19 for details of the operation of the speakers.

Pin	Name	Type	Description
1	SPKR_L-	AO	Stereo speaker, left channel
2	SPKR_L+	AO	

J9: USB Host

Board connector: USB Type A receptacle, Amp 787616-1

Mating connector: USB Type A plug

Location on board: A6-A7

Connector J9 provides the signals for the PXA270 USB Host port. Connector shields are tied to chassis ground. See Universal Serial Bus, page 12 for a description of the USB connectivity.

Pin	Name	Type	Description
1	USB_HOST_PWR	PO	DC power output
2	USB_HOST-	IO	USB Host port data
3	USB_HOST+	IO	
4	HOST_GND	P	ground

J10: USB Client

Board connector: USB Type B receptacle, Amp 787780-1

Mating connector: USB Type B plug

Location on board: A6

Connector J10 supplies the signals for the PXA270 USB Client port. Connector shields are tied to chassis ground. See Universal Serial Bus, page 12 for a description of the USB connectivity.

Pin	Name	Type	Description
1	USB_FCN_CNCT	PI	DC power input used to sense connection
2	USB_FCN-	IO	USB Client port data
3	USB_FCN+	IO	
4	FCN_GND	P	ground

J11: Processor JTAG, I²C, and SSP

Board connector: 2x10 socket, 0.05-inch, Samtec SFMC-110-02-S-D

Mating connector: TFMDL series

Location on board: A1-B1

Connector J11 includes a hardware reset input, an external connection to the I²C bus, a SSP port, and a JTAG interface. In addition to the external connection on connector J11, the hardware reset signal, RESET_IN#, connects to SW1 (SW1: Reset, page 27) and to reset circuitry located on the TurboXb module. See Reset, page 40 for electrical specification for this signal.

The I²C bus and SSP port provide serial communication with external devices. See I2C Bus, page 15 and Synchronous Serial Ports, page 14, respectively for detail about these interfaces. The JTAG interface is used during manufacturing for programming and debug; otherwise, it is not supported for application use. Production customers may use this connector to reprogram boot code. Notice that connector J11 does not match the Eurotech standard pinout for the JTAG interface.

Pin	Name	Type	Termination	Description
1	/CPU_TRST	I	PU 10kΩ 3.3 V	PXA270 JTAG reset
2	/RESET_IN	IO	PU 10kΩ 3.3 V	Hardware reset
3	CPU_TMS	I	PU 33kΩ 3.3 V	
4	GND	P		
5	CPU_TCK	I	PD 33kΩ	
6	GND	P		PXA270 JTAG
7	CPU_TDI	I	PU 33kΩ 3.3 V	
8	GND	P		
9	CPU_TDO	O		
10	GND	P		ground
11	I2C_SDA	IO	PU 10kΩ 3.3 V	I²C data
12	CPU_JTAG_VREF	PO		Reference voltage
13	SSP_FRM	O		SSP slave select
14	VUC	PO		Reference voltage
15	SSP_MISO	I	PU 33kΩ 3.3 V	SSP receive data
16	I2C_SCL	IO	PU 10kΩ 3.3 V	I²C clock
17	SSP_MOSI	O		SSP transmit data
18	GND	P		ground
19	SSP_SCK	O		SSP clock
20	GND	P		ground

J12: Backlight

Board connector: 7-pin header, right angle, 1.25 mm, Molex 53261-0771

Mating connector: 51021-0700

Location on board: A7

Header J12 includes the power and control signals required by an external backlight inverter. The backlight power input, BACKLIGHT_VCC (J19: Input Power, page 37) is filtered and passed through to this header. See Backlight, page 18 for a description of the backlight control.

Pin	Name	Type	Termination	Description
1 2	BL_VCC	PO		Filtered backlight power
3 4	GND	P		ground
5	BACKLIGHT_ON	OC	PU 47kΩ BL_VCC	Backlight on/off
6	BACKLIGHT_PWM	AO		Backlight intensity
7	GND	P		ground

J13: Docking Header: System Bus, Ethernet, SSP, Serial 1, and JTAG

Board connector: SODIMM-144 socket with retention clips, Molex 54698-7000

Location on board: B3-D3

The TurboXb module is installed in SODIMM socket J13.

J14: CompactFlash

Board connector: Type II CompactFlash card header, CFCMD-35015W100

Mating connector: CompactFlash card

Location on board: B1-D2

The 50-pin CompactFlash socket J14 conforms to the CompactFlash standard for Type I and II cards operating at 3.3 V or 5 V. Shields are tied to chassis ground. See External Memory, page 11 for information about CompactFlash.

J15: Docking Header: Display, Touch Panel, USB, and Audio

Board connector: 2x40 pin receptacle, 0.5 mm, Hirose DF12(3.0)-80DS-0.5V(86)

TurboXb module connector: 2x40 pin header, 0.5 mm, Hirose DF12(3.0)-80DP-0.5V(86)

Location on board: B5-C5

Header J1 of the TurboXb module mates to receptacle J15.

J16: LCD

Board connector: 2x17 shrouded terminal strip, 0.1-inch, Samtec HTST-117-01-L-D

Mating connector: HCSD series

Location on board: B7-D7

Connector J16 provides a parallel interface to a LCD. The following table describes the signals included on the connector. Signal names shown are for TFT active matrix color LCDs at 16 bit-per-pixel (bpp). See Display, page 16 for further details about the LCD interface.

Pin	PXA270 Signal Name	Color Active TFT Display at 16bpp	
		Eurotech Signal Name	Description
1		n/c	
2		GND	ground
3	L_PCLK	PNL_PIXCLK	Pixel clock
4	L_LCLK	PNL_HSYNC	Horizontal sync
5	L_FCLK	PNL_VSYNC	Vertical sync
6		GND	ground
7	LDD15	PNL_RED0	Red data
8	LDD11	PNL_RED1	
9	LDD12	PNL_RED2	
10	LDD13	PNL_RED3	
11	LDD14	PNL_RED4	
12	LDD15	PNL_RED5	
13		GND	ground
14	LDD5	PNL_GREEN0	Green data
15	LDD6	PNL_GREEN1	
16	LDD7	PNL_GREEN2	
17	LDD8	PNL_GREEN3	
18	LDD9	PNL_GREEN4	
19	LDD10	PNL_GREEN5	
20		GND	ground
21	LDD4	PNL_BLUE0	Blue data
22	LDD0	PNL_BLUE1	
23	LDD1	PNL_BLUE2	
24	LDD2	PNL_BLUE3	
25	LDD3	PNL_BLUE4	
26	LDD4	PNL_BLUE5	
27		GND	ground

Pin	PXA270 Signal Name	Color Active TFT Display at 16bpp	
		Eurotech Signal Name	Description
28	L_BIAS	PNL_LBIAS	Data enable
29 30		PNL_PWR	5 V or 3.3 V (set by R56 or R55)
31		PNL_RL	Horizontal mode select (set by R53 or R54)
32		PNL_UD	Vertical mode select (set by R59 or R57)
33	GPIO94	PNL_ENA	Panel enable
34	Filtered PWM1	VCON	Low-voltage adjust for contrast control of some displays

J17: Docking Header: CF, SD/MMC, Serial 2 & 3, I^2C, and JTAG

Board connector: 2x40 pin receptacle, 0.5 mm, Hirose DF12(3.0)-80DS-0.5V(86)

TurboXb module connector: 2x40 pin header, 0.5 mm, Hirose DF12(3.0)-80DP-0.5V(86)

Location on board: C5-D5

Header J2 of the TurboXb module mates to receptacle J17.

J18: SD/MMC

Board connector: SD card header, FCI 10022711-002PLF

Mating connector: standard SD/MMC card

Location on board: C6-D7

Socket J18 supplies the signals for the Secure Digital and MultiMediaCard (SD/MMC) interface. Shields are tied to chassis ground. See Secure Digital and MultiMediaCard Interface, page 13 for details about the various modes of operation.

Pin	Name	Type	Description
1	SD_DAT3	IO	SD/MMC data
2	SD_CMD	IO	SD/MMC command
3	GND	P	ground
4	SD_PWR	P	Software-controlled 3.3 V
5	SD_CLK	O	SD/MMC clock
6	GND	P	ground
7	SD_DAT0	IO	
8	SD_DAT1	IO	SD/MMC data
9	SD_DAT2	IO	
10	/SD_CD	I	SD/MMC card detect
11	/SD_WP	I	SD/MMC write protect

J19: Input Power

Board connector: 6-pin header, right angle, 0.1-inch, Molex 22-05-2061

Mating connector: 6471 series

Location on board: D2

Header J19 accepts input power from external supplies. 5V_IN is the main input power to the TurboXb development system. On-board power regulators generate other voltages required by the TurboXb module and peripherals from 5V_IN. See Power Management System, page 21 for an overview of how the TurboXb development system power supply is structured. The backlight power input, BACKLIGHT_VCC, is filtered and passed through to header J12 (J12: Backlight, page 34).

Pin	Name	Type	Description
1	5V_IN	PI	5V input power
2	GND	P	ground
3	n/c		
4	BACKLIGHT_VCC	PI	Backlight power
5	POWERON	O	Output for power supply management
6	n/c		

J20: CPLD JTAG

Board connector: 6-pin terminal strip, 2 mm, Samtec TMM-106-03-T-S

Mating connector: TCSD series

Location on board: D4

Connector J20 is used to program and debug the CPLD located on the TurboXb module. This interface is not supported for application use.

Pin	Name	Type	Description
1	CPLD_JTAG_VREF	PO	Reference voltage
2	GND	P	ground
3	CPLD_TCK	I	CPLD JTAG
4	CPLD_TDO	O	
5	CPLD_TDI	I	
6	CPLD_TMS	I	

J21: Touch Panel

Board connector: 4-pin header with friction lock, 0.1-inch, Molex 22-23-2041
or 5-pin header with friction lock, 0.1-inch, Molex 22-23-2051

Mating connector: 6471 series

Location on board: D5

A touch panel connects to the TurboXb development system on header J21. The header provides the signals to support a 4- or 5- wire analog touch panel. Standard TurboXb development systems include a 4-wire touch panel. See Touch Panel, page 18 for details about the touch panel interface.

Pin	Name	Type	4-wire	5-wire	Description
1	TSMX	AIO	left	LL	Touch panel
2	TSPX	AIO	right	UL	
3	TSPY	AIO	top	UR	
4	TSMY	AIO	bottom	LR	
5	WIPER	AI			Touch panel wiper (optional 5-wire touch)

System Specification

Power Specification

The TurboXb development system requires a main input power of 5 V. Circuitry included on the solution board and TurboXb module generates all other voltages including the on-board supply voltage V_{DDX} and the processor core voltage V_{DDI}. The PXA270 processor can change V_{DDI} dynamically to achieve lower power consumption at high clock rates. In addition, the TurboXb development system can minimize power consumption by transitioning to Sleep mode. During Sleep mode, the POWERON signal de-asserts. When main power is removed, a battery included on the solution board supplies RTC backup power. The following are power specifications for the TurboXb development system.

Absolute maximum ratings

Supply Voltage (5V_IN) 5.1 V

Symbol	Parameter		Min	Typ.	Max	Units
System Power						
V_{5V_IN}	Input supply voltage		4.9	5.0	5.1	V
V_{DDX}	On-board supply (note 1)	Run		3.3		V
I (V_{DDX})	3.3 V available for display, CF, etc. (note 2)	Run			tbd	mA
		Sleep			tbd	mA
V_{DDI}	Processor core voltage		0.8075	0.85	1.705	V
POWERON						
V_{OH}	Output high level at I_O min		2.2			V
V_{OL}	Output low level at I_O max				0.55	V
I_O	Output current		-24		24	mA
$t_{POWERON}$	(note 3)				10	ms
RTC Backup Power						
V_{BAT}	Real-time clock battery backup		2.0	3.0	3.5	V
I_{BAT}	Current at V_{BAT} = 3.0 V			300	500	nA

Notes:

1. A DC/DC converter, LTC 1771, generates V_{DDX}. "Burst" mode is disabled.
2. The TurboXb module consumes tbd of the available tbd A.
3. If POWERON is used to disabled the external supply, V_{IN} must be stable within $t_{POWERON}$ after the signal is asserted.

Electrical Specification

This section provides electrical specifications for the TurboXb development system. For details about termination of individual signals, see the signal connectors in Connectors, page 28.

Reset

One of three methods can reset the system. The hardware reset signal RESET_IN# connects to connector J11, the reset button SW1, and reset circuitry located on the TurboXb module. The TurboXb module reset circuitry monitors the on-board 3.3 V and forces the signal low when the voltage falls below a threshold voltage. The following are electrical specifications for RESET_IN#.

Absolute maximum ratings
Reset Input (/RESET_IN) 3.4 V (note 4)

Symbol	Parameter	Min	Typ.	Max	Units
V_{DDX}	On-board supply voltage		3.3		V
RESET_IN#					
V_{TH}	Reset threshold voltage (note 5)		3.08		V
t_{RESET_IN}	Reset pulse duration (note 6)	140	240	560	ms
V_{IH}	Input high level	0.8 * V_{DDX}		V_{DDX} + 0.1	V
V_{IL}	Input low level	-0.1		0.2 * V_{DDX}	V

Notes:

4. RESET_IN# connects directly to the PXA270 processor, which determines this rating.
5. The reset circuitry on the TurboXb module forces RESET_IN# low at this voltage.
6. RESET_IN# signal remains low for t_{RESET_IN} after the input voltage to the TurboXb module rises above V_{TH}.

PXA270 Processor

The PXA270 processor provides the I^2C bus, SSP, and SD/MMC interface. These lines should be treated as digital I/Os and protected for over-current and over-voltage accordingly. The following are electrical specifications for the PXA270 processor.

Absolute maximum ratings

Input voltage, digital I/O pins 3.4 V

Symbol	Parameter	Min	Typ.	Max	Units
V_{DDX}	On-board supply voltage		3.3		V
Digital Outputs					
V_{OH}	Output high level at I_O min	V_{DDX} – 0.3		V_{DDX}	V
V_{OL}	Output low level at I_O max	0		0.3	V
I_O	Output current	-3		3	mA
Digital Inputs					
V_{IH}	Input high level	0.8 * V_{DDX}		V_{DDX} + 0.1	V
V_{IL}	Input low level	-0.1		0.2 * V_{DDX}	V
I2C Bus (SDA, SCK)					
	Bus clock (note 7)	100		400	kHz
	Buffer size			1	byte

Notes:

7. The PXA270 supports "standard" and "fast" I2C speeds of 100 and 400 kHz; however, the speed is limited to 100 kHz by the RTC.

Display and Backlight

Displays have a wide range of voltage and data requirements. The TurboXb development system includes an adjustable display power supply and display signal voltage to support these requirements, as well as controls for brightness (backlight) and contrast (passive LCD panels). The following are electrical specifications for the display and backlight interfaces.

Symbol	Parameter	Min	Typ.	Max	Units
LCD					
V_{PNL_PWR}	Display power supply (note 8 & 9)	3.3	5.0	5.0	V
I_{PNL_PWR}	Current limit accuracy	1.0	1.3	1.6	A
V_{PNL_DATA}	Display signal voltage (note 8 & 10)	3.3	3.3	5.0	V
Scan direction (active displays)					
R_{PNL_RL}	Pull-up/down resistance		4.7		kΩ
R_{PNL_UD}	Pull-up/down resistance		4.7		kΩ
V_{PNL_RL}	(note 11)	0	V_{PNL_PWR}	V_{PNL_PWR}	V
V_{PNL_UD}	(note 12)	0	V_{PNL_PWR}	V_{PNL_PWR}	V
Brightness Control					
V_{BL_VCC}	Backlight supply voltage		12		V
$V_{BACKLIGHT\_PWM}$	(note 13)	0		3.3	V
Contrast Control (passive LCD displays)					
V_{VCON}	Low-voltage contrast adjust (note14)	0		3.3	V

Notes:

8. The PXA270 enables the power to the display and display signal buffer.
9. One of two resistors selects the display voltage. R55 selects 3.3 V, while R56 selects 5 V. Standard systems are configured for 5 V operation.
10. One of two resistors selects the display signal voltage. R99 selects 3.3 V power for the buffer, while R100 selects 5 V power. Standard systems are configured for 3.3 V operation.
    5 V displays with V_{IH} <= 0.6•V_{PNL_PWR} (3.0 V) will work reliably with 3.3 V data.
11. PNL_RL is pulled up with R53 or pulled down with R54. Standard systems pull up PNL_RL.
12. PNL_UD is pulled up with R59 or pulled down with R57. Standard systems pull up PNL_UD.
13. BACKLIGHT_PWM is a filtered PXA270 PWM signal.
14. VCON is the low-voltage PWM signal used to control VEE. It can directly control contrast on some passive displays.

Touch Panel Controller

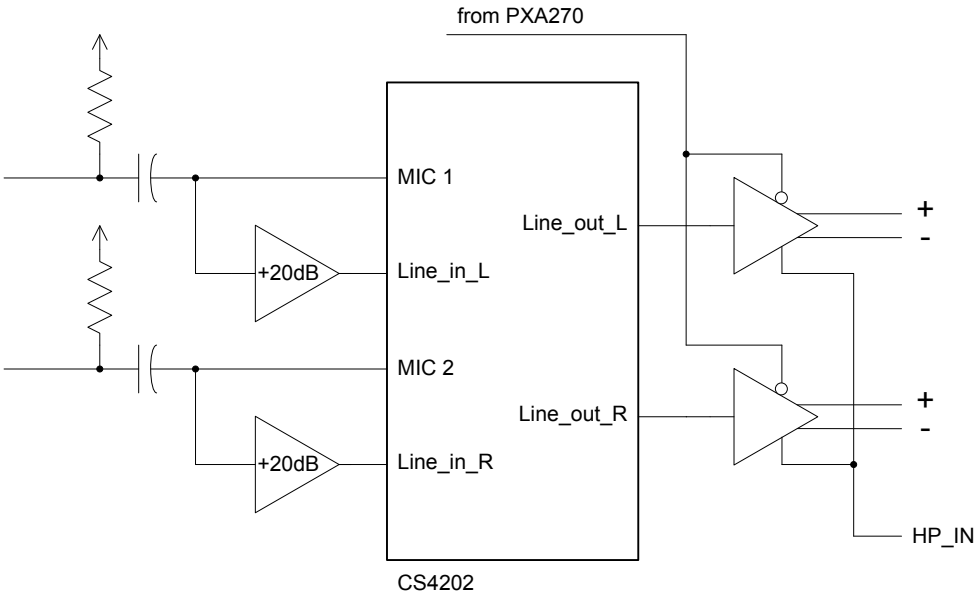
The TurboXb development system uses touch panel controllers from Burr Brown. It uses the ADS7846 to support 4-wire resistive touch panels and the ADS7845 to support 5-wire panels. The system is factory-configured for use with 4-wire panels. The following are electrical specifications for the touch panel controller.

Symbol	Parameter	Min	Typ.	Max	Units
V_{DD}	Supply voltage		3.3		V
---	A/D sample resolution		12		bit

Audio

For its audio subsystem, the TurboXb development system uses the Cirrus CS4202 AC'97 stereo codec with dual audio input and output channels, combined with an output power amplifier and a microphone pre-amp with power for electret microphones. The output amplifier supports differential and single-ended modes. When the HP_IN signal is greater than V_{HP_IN}, the amplifier is in single-ended mode; when lower, it is in differential mode.

The following diagram illustrates the relationship of the signal amplifiers to the codec.



The following are electrical specifications for the audio interface.

Absolute maximum ratings

V_{IN_MIC} 5 V_{DC}

Symbol	Parameter	Min	Typ.	Max	Units
D_{VDD}	Codec digital supply voltage (note 15)		3.3		V
A_{VDD}	Codec analog supply voltage (note 15)		5.0		V
f_{SO}	Sample rate, output		48		kHz
f_{SI}	Sample rate, input (note 16)	8		44.1	kHz
Audio Input					
V_{IN_MIC}	Signal input voltage		100		mV_{rms}
Gain	Pre-amp gain		20		dB
f_O	Pre-amp low-pass cutoff (note 17)		3.4		kHz
R_{IN_MIC}	Input impedance		12.5		kΩ
C_{IN_MIC}	DC blocking capacitor		1		µF
V_{MIC_PWR}	Microphone power (MIC_L/R+)		5		V
R_{MIC_PWR}	Microphone power, series resistance			3.2	kΩ
Audio Output					
R_L	Speaker load	4	8		Ω
V_{OUT}	ZSPKR=4Ω, differential mode			3.7	V_{rms}
V_{DC}	DC bias, differential mode		0.5		A_{VDD}
P_{SPKR}	Output power, ea. channel (note 18)				
	Differential, THD+N 1%, RL 4Ω		1.0	2.2	W
	Differential, THD+N 10%, RL 4Ω		1.0	2.7	W
	Differential, THD+N 1%, RL 32Ω		1.0	0.34	W
	Single-ended, THD+N 0.5%, RL 32Ω		75	85	mW
	Single-ended, THD+N 1%, RL 8Ω			340	mW
	Single-ended, THD+N 10%, RL 8Ω			440	mW
HP_IN					
R_{HP_IN}	Pull-up resistance			100	kΩ
V_{HP_IN}	Pull-up voltage		5		V
V_{TH}	Threshold voltage		4		V

Notes:

15. The PXA270 enables power to the audio subsystem.
16. The output sample rate is fixed, but the input sample rate can be set to 8, 11.025, 22.05, or 44.1 kHz.
17. Pre-amp anti-aliasing filter rolls off at 3dB/octave (first-order filter).
18. Typical values are guaranteed to the output power amplifier's AOQL (Average Outgoing Quality Level). Operating above typical values for a sustained period may result in thermal shutdown of the amplifier.

General Specification

This section provides general specifications for the TurboXb development system.

Crystal Frequencies

Agencies certifying the TurboXb development system for compliance for radio-frequency emissions typically need to know the frequencies of on-board oscillators. The following table lists the frequencies of all crystals on the TurboXb development system.

Crystal	Device	Typ.	Units
XT1	PXA270 core	13.000	MHz
XT2	PXA270 RTC	32.768	kHz
X1	Codec	24.576	MHz
X2	RTC	32.768	kHz
Y3	Ethernet	25.000	MHz

Appendix A – Reference Information

Product Information

Product notices, updated drivers, support material:

www.eurotech.com

USB Information

Universal Serial Bus (USB) specification and product information:

www.usb.org

Marvell

Information about the PXA270 processor:

www.marvell.com

CompactFlash

CompactFlash specification:

www.compactflash.org

Appendix B – RoHS Compliance

The Restriction of the use of certain Hazardous Substances (RoHS) Directive came into force on 1st July 2006. This product shall be designed using RoHS compliant components, and manufactured to comply with the RoHS Directive.

Eurotech has based its material content knowledge on a combination of information provided by third parties and auditing our suppliers and sub-contractor's operational activities and arrangements. This information is archived within the associated Technical Construction File. Eurotech has taken reasonable steps to provide representative and accurate information, though may not have conducted destructive testing or chemical analysis on incoming components and materials.

Additionally, packaging used by Eurotech for its products complies with the EU Directive 2004/12/EC in that the total concentration of the heavy metals cadmium, hexavalent chromium, lead and mercury do not exceed 100ppm.

Appendix C – Board Revision

This manual applies to the current revision of the module and solution board as given in the next sections.

Identifying the Board Revision

The product revision numbers of the TurboXb module and solution board are printed on the solder mask of the printed circuit boards. The revision number of the solution board is located in the area under the module. The TurboXb module revision number is located on the component side, along the edge of the board.

Solution Board Revision History

The following is an overview of the revisions to the solution board.

Revision A

Initial release

Revision A corresponds to the product revision number TurboXb_PB v2.1.

New features

Breakout headers of previous prototypes removed.

Standard Eurotech connectors used.

AC ’97 codec added.

TurboXb Module Revision History

The following is an overview of the revisions to the TurboXb module.

Revision 3

Prototype

Revision A

Initial release

Revision A corresponds to the product revision number PXA270 card engine v1.3.1.

Changes

AC ’97 codec removed.

Core voltage power supply added.

Appendix D – Frequently Asked Questions

TurboXb development systems are designed to get the developer up and running quickly.

To use the system, simply plug the power supply into the receptacle on the system.

Most operating systems cold boot within twenty seconds. If the screen does not display anything after five to ten seconds, check the following frequently asked questions:

Q: When I plug in power, my screen is white and nothing comes up on it.

A: Check the connector seating. The flat panel connector may have come loose in shipping. Press it firmly into the panel and reapply power to your system.

Q: When I plug in power, the LED does not turn on.

A: Your system may still be booting. The LED is software-controlled and may not turn on at boot.

Q: Do I have to turn off the system before I insert a CompactFlash card?

A: No. The TurboXb supports hot swapping of CompactFlash cards. Consult the operating system documentation for details.

Q: Do I need to observe any ESD precautions when working with the system?

A: Yes. Where possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the board or touching any components on the board.

Q: What do I need to start developing my application for the system?

A: You will need a flash ATA card (32 MiB or larger, 128 MiB recommended), SD/MMC card, or USB disk drive and the cables supplied with your system to interface your development station to the system. For further direction, consult the Eurotech guide for the installed operating system.

Q: Who can I call if I need help developing my application?

A: Eurotech provides technical support to get your development system running. For customers who establish a business relationship with Eurotech, we provide support to develop applications and drivers.

Q: Is there online support?

A: Yes. Information about the TurboXb hardware and software is available on the Eurotech support site at http://www.eurotech.com.

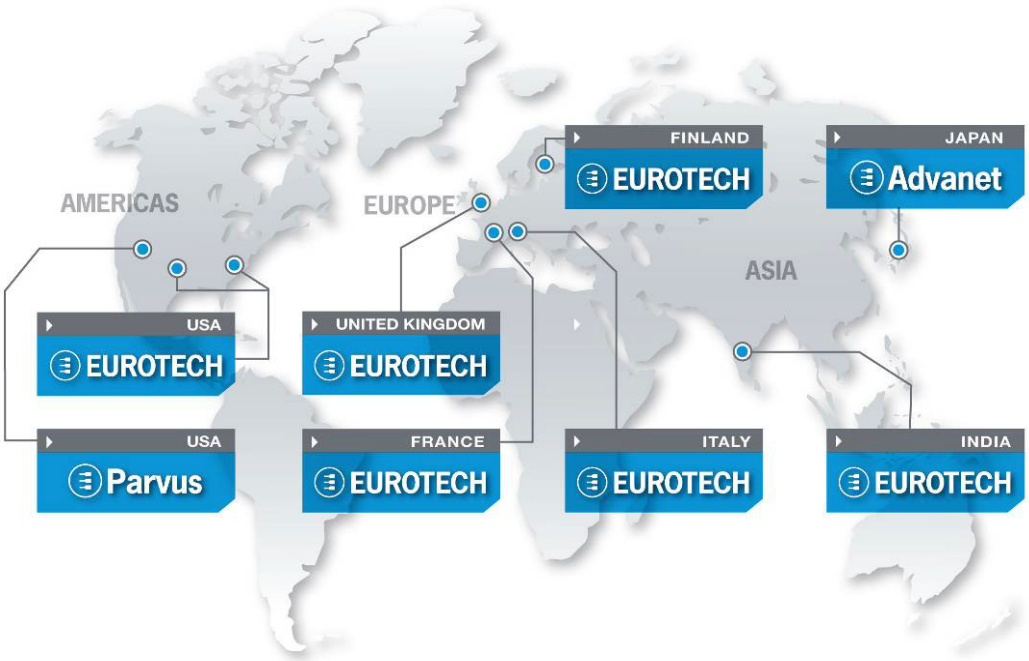
Q: Can I upgrade the version of the operating system?

A: Yes. Eurotech provides regular operating system updates on its developers' web site. For operating systems not maintained by Eurotech, contact the operating system vendor.

Q: I would like to interface to a different display panel. How can I do this?

A: Eurotech may have already interfaced to the panel of which you are interested. Consult Eurotech for availability.

Eurotech Worldwide Presence



AMERICAS

USA

EUROTECH
Toll free +1 888.941.2224
Tel. +1 301.490.4007
Fax +1 301.490.4582
E-mail: sales.us@eurotech.com
E-mail: support.us@eurotech.com
Web: www.eurotech-inc.com

PARVUS
Tel. +1 800.483.3152
Fax +1 801.483.1523
E-mail: sales@parvus.com
E-mail: tsupport@parvus.com
Web: www.parvus.com

EUROPE

Italy

EUROTECH
Tel. +39 0433.485.411
Fax +39 0433.485.499
E-mail: sales.it@eurotech.com
E-mail: support.it@eurotech.com
Web: www.eurotech.com

United Kingdom

EUROTECH
Tel. +44 (0) 1223.403410
Fax +44 (0) 1223.410457
E-mail: sales.uk@eurotech.com
E-mail: support.uk@eurotech.com
Web: www.eurotech.com

France

EUROTECH
Tel. +33 04.72.89.00.90
Fax +33 04.78.70.08.24
E-mail: sales.fr@eurotech.com
E-mail: support.fr@eurotech.com
Web: www.eurotech.com

Finland

EUROTECH
Tel. +358 9.477.888.0
Fax +358 9.477.888.99
E-mail: sales.fi@eurotech.com
E-mail: support.fi@eurotech.com
Web: www.eurotech.com

ASIA

Japan

ADVANET
Tel. +81 86.245.2861
Fax +81 86.245.2860
E-mail: sales@advanet.co.jp
E-mail: tsupport@advanet.co.jp
Web: www.advanet.co.jp

India

EUROTECH
Tel. +91 80.43.35.71.17
E-mail: sales.in@eurotech.com
E-mail: support.in@eurotech.com
Web: www.eurotech.com

To find your nearest contact refer to: www.eurotech.com/contacts

EUROTECH

www.eurotech.com

EUROTECH HEADQUARTERS
Via Fratelli Solari 3/a
33020 Amaro (Udine) – ITALY
Phone: +39 0433.485.411
Fax: +39 0433.485.499

For full contact details go to: www.eurotech.com/contacts