LXT970 Fast Ethernet Transceiver Layout and Design Guide

Application Note

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As of January 15, 2001, this document replaces the Level One document known as *AN71*.

Application Note

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1.0 Introduction and Overview

This application note provides detailed design and layout guidelines for the LXT970 and LXT970A PHY Transceivers. Both devices will be referred to as the LXT970 throughout the remainder of this document. This document also includes component selection information and recommendations for signal placement and routing.

The LXT970 is a dual-speed (10/100) Fast Ethernet PHY transceiver that supports 100BASE-TX, 100BASE-FX, and 10BASE-T applications. Refer to the LXT970 data sheet for complete details on all the device functions and capabilities. The diagram below shows implementation of the LXT970 in a typical design.

The LXT970 provides four interfaces:

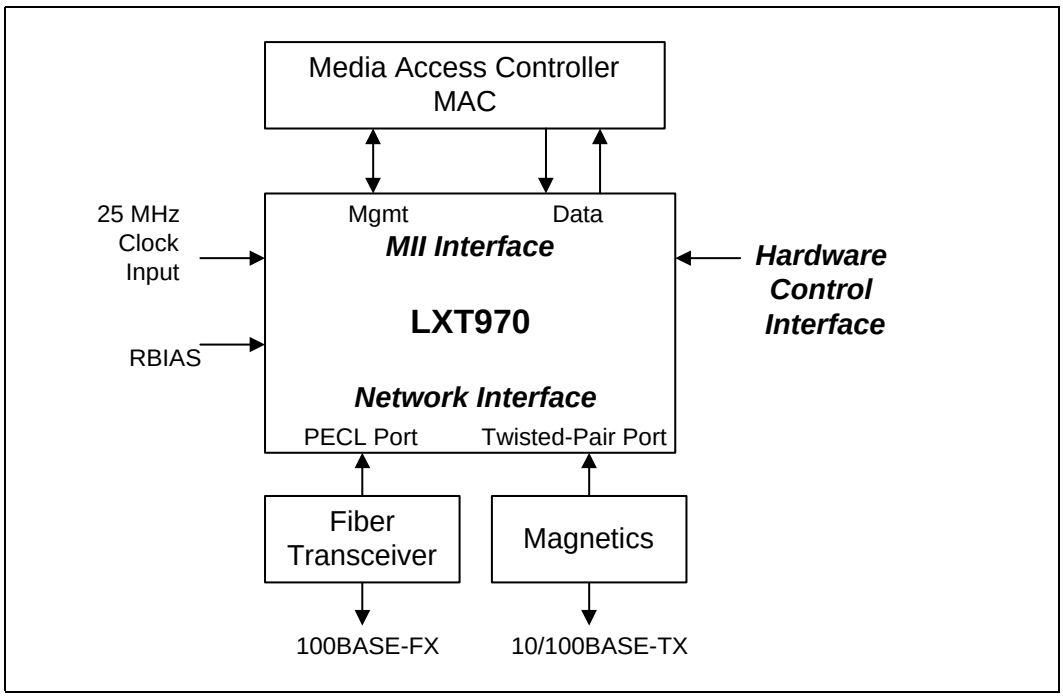
- The MII is an IEEE standard interface to the 10/100 Media Access Controller (MAC). It provides capabilities for exchanging data between the LXT970 and the MAC. In addition to data, the MII provides a two-wire management interface that can manage up to 31 LXT970 devices.
- The twisted-pair interface directly drives a 10/100 twisted-pair connection.
- The hardware control interface sets the initial state of the LXT970 at power-up.
- The pseudo-ECL (PECL) fiber interface supports 100BASE-FX applications.

2.0 Design and Layout Checklist

Good design practices are required throughout the entire design process in order to achieve maximum performance from the LXT970.

- Verify that all components meet application requirements. Use component listings as reference only.
- Design in filters for the analog power circuits. They may be removed if proven to be unnecessary.
- Use ample decoupling and bulk caps.
- Use a single analog power and ground plane for multiple devices. Keep ferrite bead currents under 65% of the rated load.
- Avoid breaks in the ground plane, especially in areas where it is shielding high-frequency signals.
- Provide termination resistors on all MII signals driven by the LXT970. Termination resistors are not required for the LXT970A when using the reduced MII driver level.
- Attach RBIAS to a 22.1 kΩ, 1% resistor to ground for internal reference current setup.
- Keep power and ground noise levels below 50 mV.
- Keep high-speed signals out of the area between LXT970 and the magnetics.

Figure 1. LXT970 10/100 Ethernet Transceiver Interface Diagram



3.0 Design Guidelines

3.1 General Guidelines

Good design practices are essential in meeting EMI and ESD requirements, and to achieve maximum line performance. These practices minimize high-speed digital switching noise, common-mode noise, and provide shielding between internal circuits and the environment. Good design practices apply *throughout* the entire design, not just to the LXT970, and include the following:

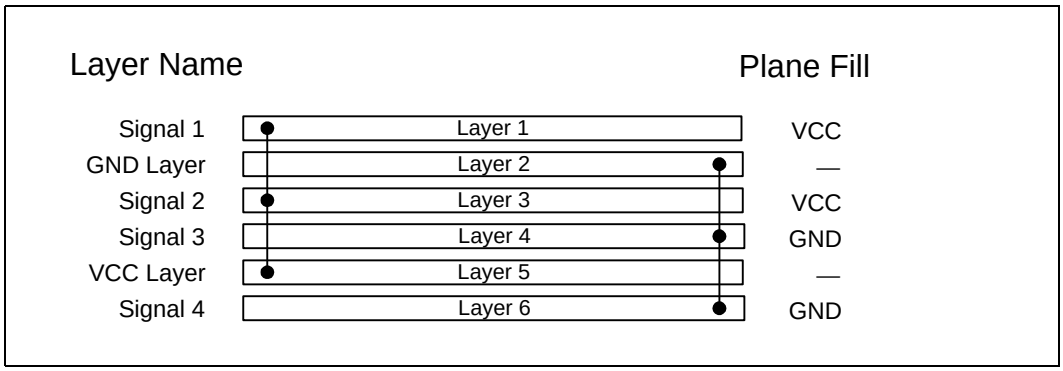
- Ensure that the power supply is rated for the load and that output ripple is minimal (<50 mV).
- Provide ample power and ground planes.
- Use bulk capacitors (4.7-10 µF) between the power and ground planes to minimize switching noise, particularly near high-speed busses (>25 MHz).
- Use an ample supply of .01 µF decoupling capacitors to reduce high-frequency noise on the power and ground planes.
- Filter and shield DC-DC converters and oscillators.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Do not route any digital signals between the LXT970 and the RJ-45 connectors at the edge of the board
- It is generally a good practice to fill in unused areas of the signal planes with solid copper and attach them with vias to a V_{CC} or ground plane that is not located adjacent to the signal layer. Refer to signal layer filling diagram in Figure 2.

3.2 Differential Signal Layout Guidelines

Layout techniques for the differential signals are as follows:

- Follow good general design practices.
- Route differential pairs close together and away from everything else.
- Keep both traces of each differential pair as close to the same length as possible.
- Avoid vias and layer changes.
- Keep transmit and receive pairs away from each other. Run orthogonally, or separate with a ground plane layer.
- Maintain the transmit and receive separation by placing all the transmit termination components on one side of the board and all the receive components on the other side.

Figure 2. Signal Layer Filling



4.0 Power and Ground

4.1 Power and Ground Planes

For high-speed communications design, the power and ground planes may be conceptually divided into four regions (the analog and digital power planes and the chassis and signal ground planes) as shown in Figure 3 on page 10.

The analog power region extends from the magnetics back to the LXT970. The power plane in this area should be filtered. Only components and signals pertaining to the interface should be placed or routed through this region.

The digital power region extends from the MII interfaces of the LXT970 through the rest of the board. Good design practices listed in the previous section should be followed throughout this area.

The digital section supplies power to the digital V_{CC} pin, MII V_{CC} pin, and to the external components. The analog section supplies power to V_{CCH}, V_{CCT}, and V_{CCR} pins of the LXT970. Refer to Figure 4 on page 11 for internal routing of power signals.

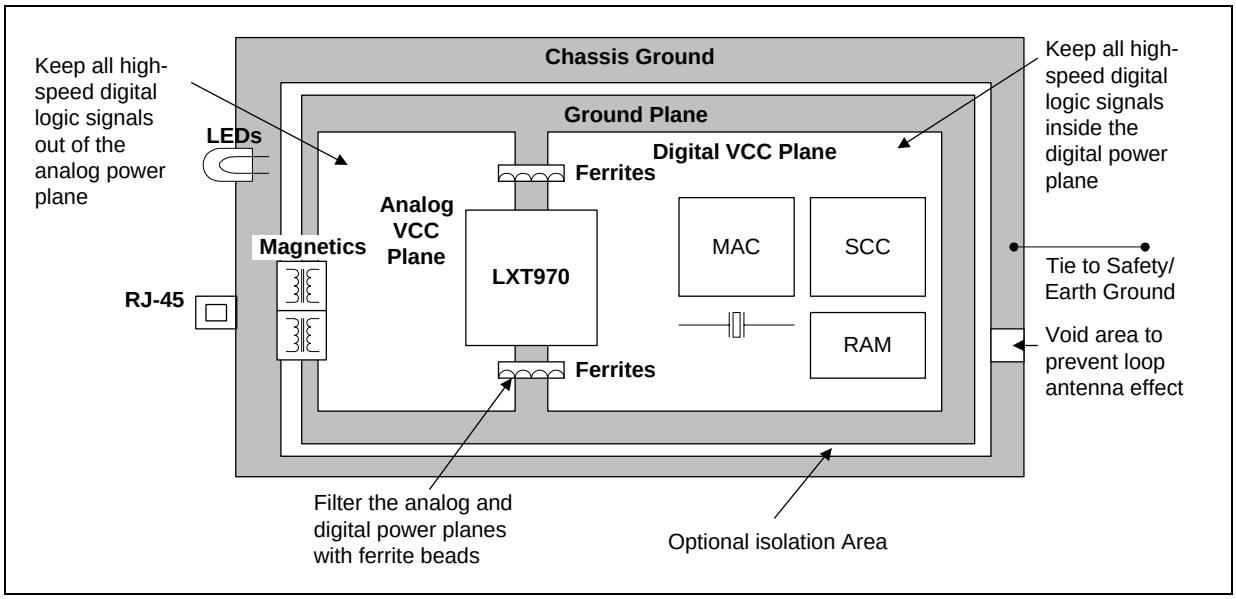
The chassis ground region extends from the front edge of the board (RJ-45 connectors) to the magnetics, and around the entire perimeter of the board. No signals should pass through this region except for external interfaces and LED signals. This region can be used for a separate chassis ground plane, which can be connected to the chassis, cable shields, unused signals, and safety earth ground.

The signal ground region is one continuous, unbroken plane that extends from the magnetics through the rest of the board. The signal ground plane may be combined with chassis ground or isolated from it. For isolation place a “moat” around the signal ground plane to separate signal ground from chassis ground. If the ground planes are combined, an isolation area is not required.

When laying out ground planes, special care must be taken to avoid creating loop antenna effect.

- Run all ground planes as solid square or rectangular regions.
- Avoid creating loops with ground planes around other planes. The only exception to this rule is chassis ground as shown in Figure 3.
- Ensure the chassis ground area (running the perimeter of the board) is voided at some point.
- Ensure the gap of the voided area in chassis ground is large enough to prevent a ground loop.

Figure 3. Power and Ground Plane Division



4.2 Design Considerations

Power supply ripple and digital switching noise can be created by:

- Overloaded or poorly regulated power supplies.
- Wide data busses (>32 bits) running at a high clock rate.
- DC-to-DC converters and crystal oscillators.

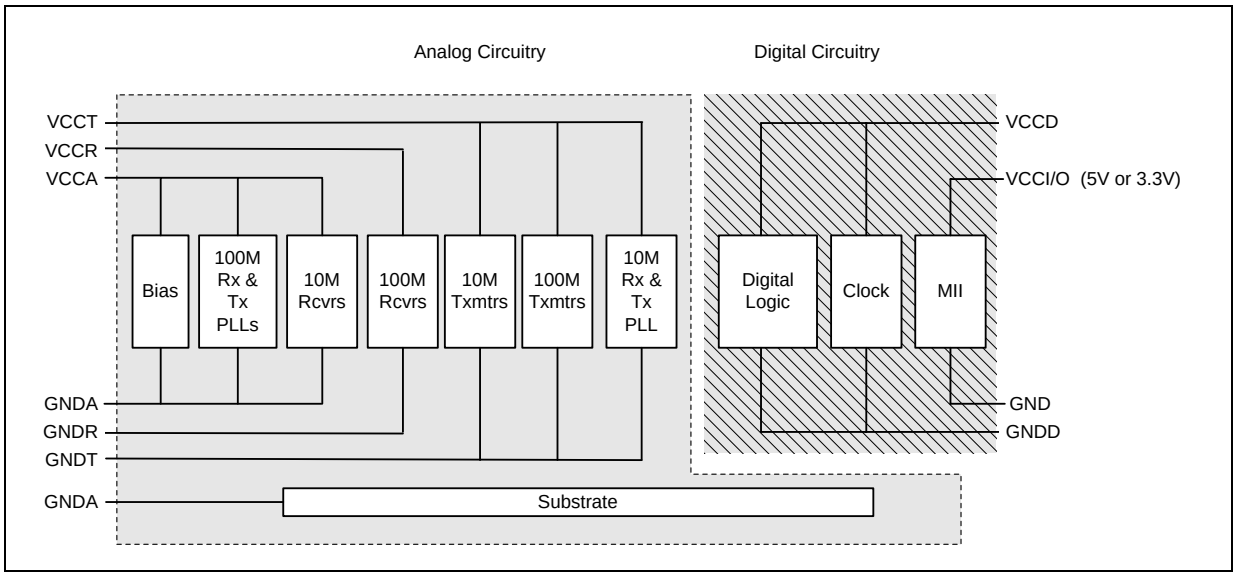
Noise created by these sources can be coupled through the power and ground planes into the transmitter and receiver and out onto the network. Coupling can occur via the termination circuits or through the analog power and ground pins of the LXT970.

The criteria in Table 1 is suggested for evaluating acceptable noise levels on the analog power and ground planes:

Table 1. Criteria for Analog Noise Levels

Noise Level	Acceptability
Under 50 mV	Acceptable
50 mV to 80 mV	Marginally Acceptable
Above 80 mV	Unacceptable

Figure 4. Power and Ground Placement

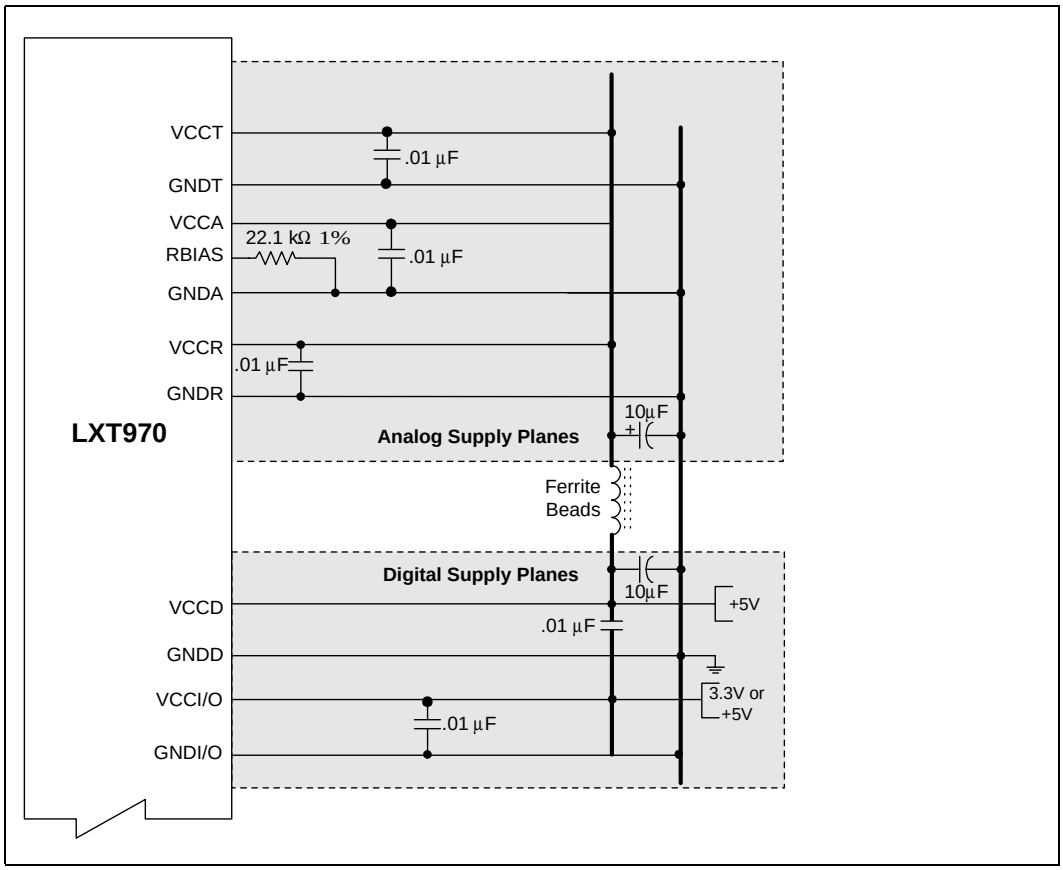


4.3 Design Implementation

Following good general design and layout guidelines will prevent most common signal and noise issues. The following recommendations apply to the design and layout of the power and ground planes:

- Divide the V_{CC} plane into two sections as shown in Figure 3 on page 10 (analog and digital). The break between the two planes should run under the device.
- When dividing the V_{CC} plane, it is not necessary to add extra layers to the board. Simply create moats or cutout regions in existing layers.
- Place a high-frequency bypass cap (.01µf) near each analog V_{CC} pin as shown in Figure 5.
- Join the digital and analog sections at one or more points by ferrite beads. Ensure the maximum current rating of the bead is at least 150% of the nominal current that is expected to flow through it (>400 mA per LXT970).
- Place a bulk capacitor (10 µF) on each side of each ferrite bead to stop switching noise from traveling through the ferrite.
- For designs with multiple LXT970s, it is acceptable to supply all from one analog V_{CC} plane. This plane can be joined to the digital V_{CC} plane at multiple points, with a ferrite bead at each one. It is also acceptable to create an individual analog V_{CC} *mini-plane* for each device.

Figure 5. Power and Ground Decoupling

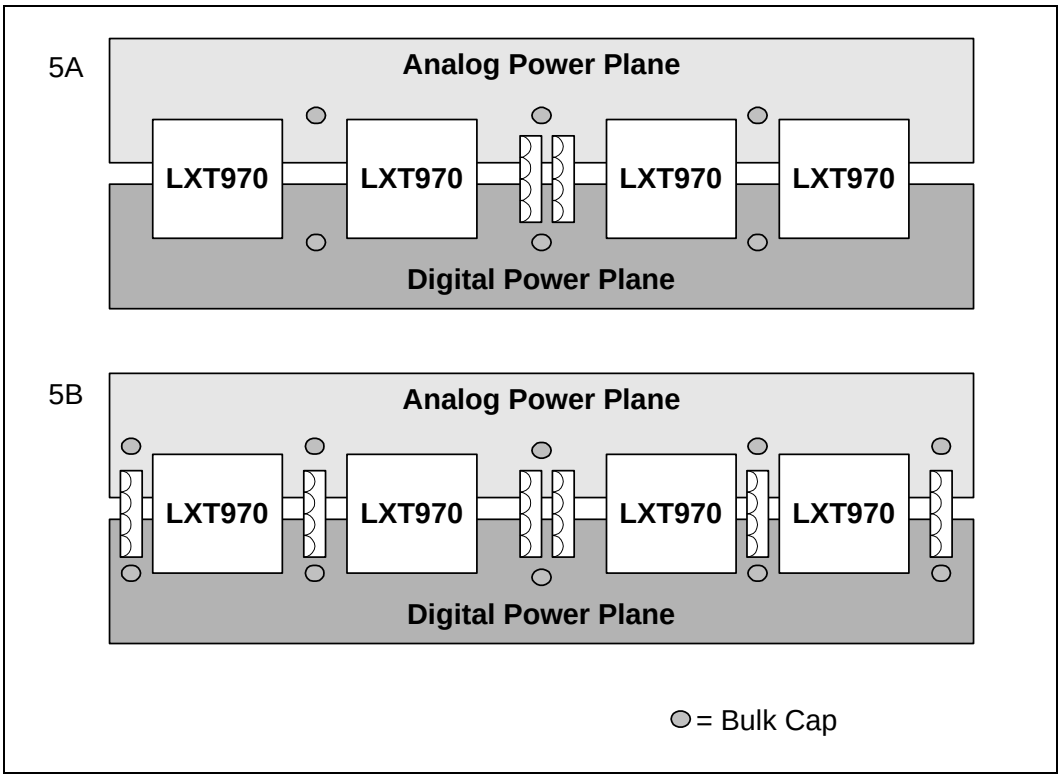


4.4 Multi-PHY Design Implementations

Figure 6 shows a general power plane layout for a design with multiple-970 devices. The following guidelines apply:

- One continuous power plane can be used to supply several LXT970 devices instead of dividing the power plane into many little pieces.
- The power plane can be supplied through one set of ferrite beads (up to 4 devices) which should be centrally located (refer to Figure 6A). Bulk caps should be located near each side of the ferrites, and should be sprinkled liberally throughout the plane with regular spacing.
- The power plane can also be supplied through multiple ferrite connections that are regularly spaced (Figure 6B). This configuration is recommended if the plane is supplying more than four devices.

Figure 6. Multi-PHY Decoupling



5.0 Twisted-Pair Interface

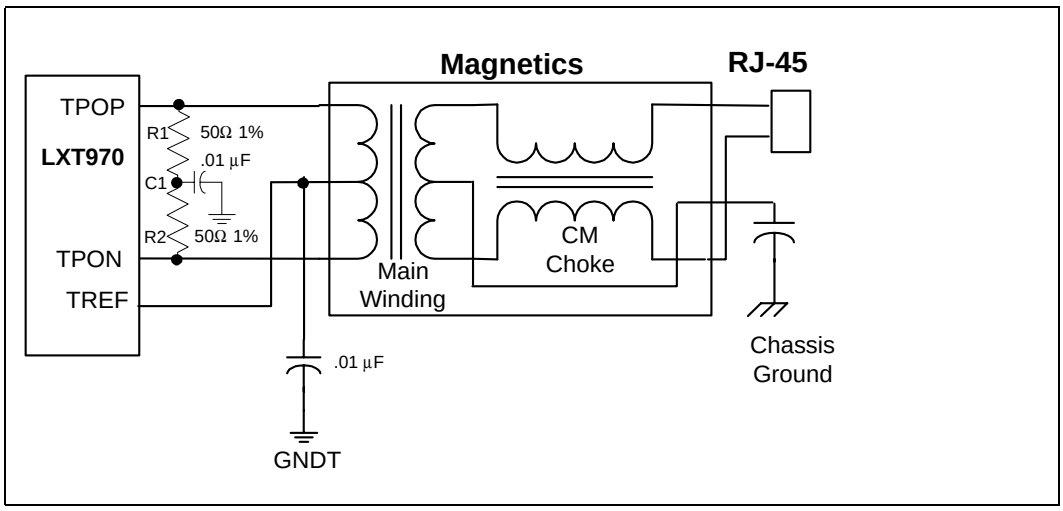
5.1 Transmit Interface Circuit

Figure 7 shows a typical transmit stage. Current is sourced by the TREF output, to the centertap of the primary side of the winding. Current flows from the centertap to TPOP and TPON. The centertap of the winding can also be directly attached to an analog VCC plane. Other components are described below:

- R1 and R2 are 50Ω, 1% termination resistors that provide impedance matching (return loss characteristics) to the line, which has a nominal impedance of 100Ω .
- C1 shunts any common-mode energy present in the output to ground. A quiet ground should be used for this.
- The magnetics consists of the main winding, a common-mode choke, and possibly a third winding called an “auto-transformer” (not shown) on the output.
- The common-mode choke stops common mode energy from reaching the line. It works together with capacitor C1 to direct common-mode energy away from the line.
- The auto-transformer (if present) provides a line-side centertap for further sinking of common-mode energy. This centertap should be referenced to chassis ground.
- TREF can be bypassed to either VCCT or GNDT.

Note: Always place the transmit termination circuit (R1, R2, C1) as close to the LXT970 as possible, even if the distance between the LXT970 and the magnetic is long.

Figure 7. Transmit Interface Circuitry



5.2 Receive Interface Circuit

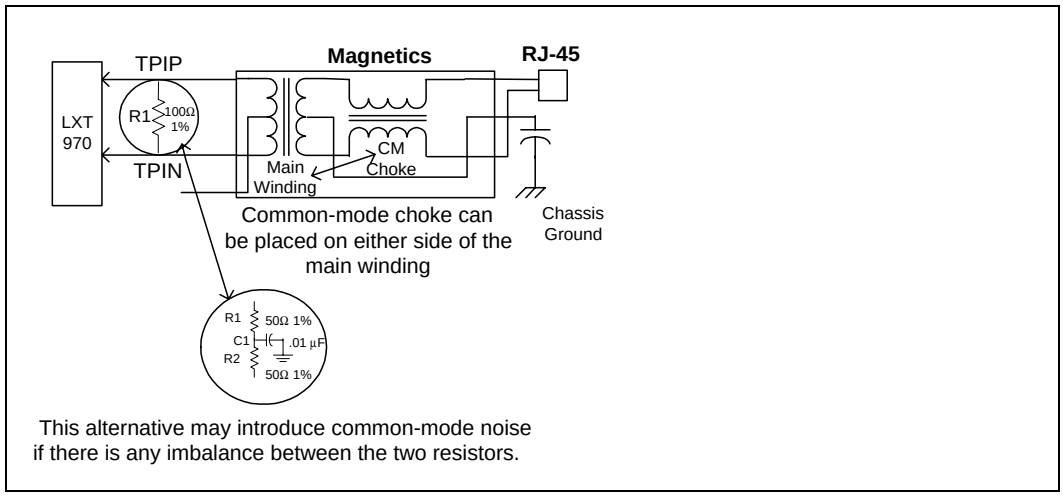
The receive circuit consists of magnetics, which include a main winding and a common-mode choke, and termination resistance to match the line impedance.

5.2.1 Common-Mode Choke

The common-mode choke can be located on either the primary or secondary side of the winding. Some vendors place the receive common-mode choke on the line-side (primary) of the main winding while others place it on the device side (secondary). Either location is acceptable.

If using a magnetic with the common-mode choke on the device side, do not attach a bypass cap from the device-side centertap to ground. Noise from the ground can couple through the cap into the centertap, bypassing the common-mode choke, causing EMI problems.

Figure 8. Receive Interface Circuitry



5.2.2 Termination Circuitry

Two options exist for the receive termination circuit as shown in Figure 8. The first option is to place a simple 100Ω, 1% resistor across the TPIP/TPIN pair. The second option is to divide the resistor in two and place a common-mode bypass cap (.01 µF) to ground. In either case, always place the receive termination circuit as close to the magnetics as possible.

Testing done to date has shown neither option is consistently better. Results are strongly dependent on the specific application. Some guidelines to consider are:

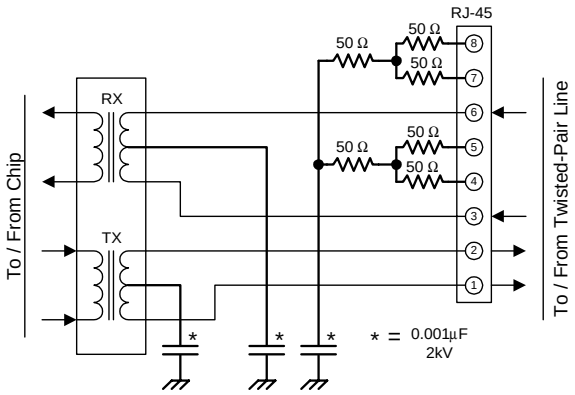
- The advantage of the two resistor approach is that the bypass cap can provide additional common-mode shielding if the ground is quiet.
- The disadvantage of the two resistor approach is that mis-matched impedance between the two resistors can create common-mode noise.

5.3 Bob Smith Termination

Many designers provide what is known as a “Bob Smith” termination for the unused pairs on the twisted-pair interface. The termination basically looks like a 100Ω load, matched to the line, which is bypassed to chassis ground.

This termination is added for robustness, although some argue that it is only useful at frequencies below 1 MHz. A typical Bob Smith implementation is shown in Figure 9

Figure 9. Bob Smith Termination Circuit



NOTE: RJ-45 connections shown for standard NIC. Tx/Rx crossover may be required for repeater & switch applications.

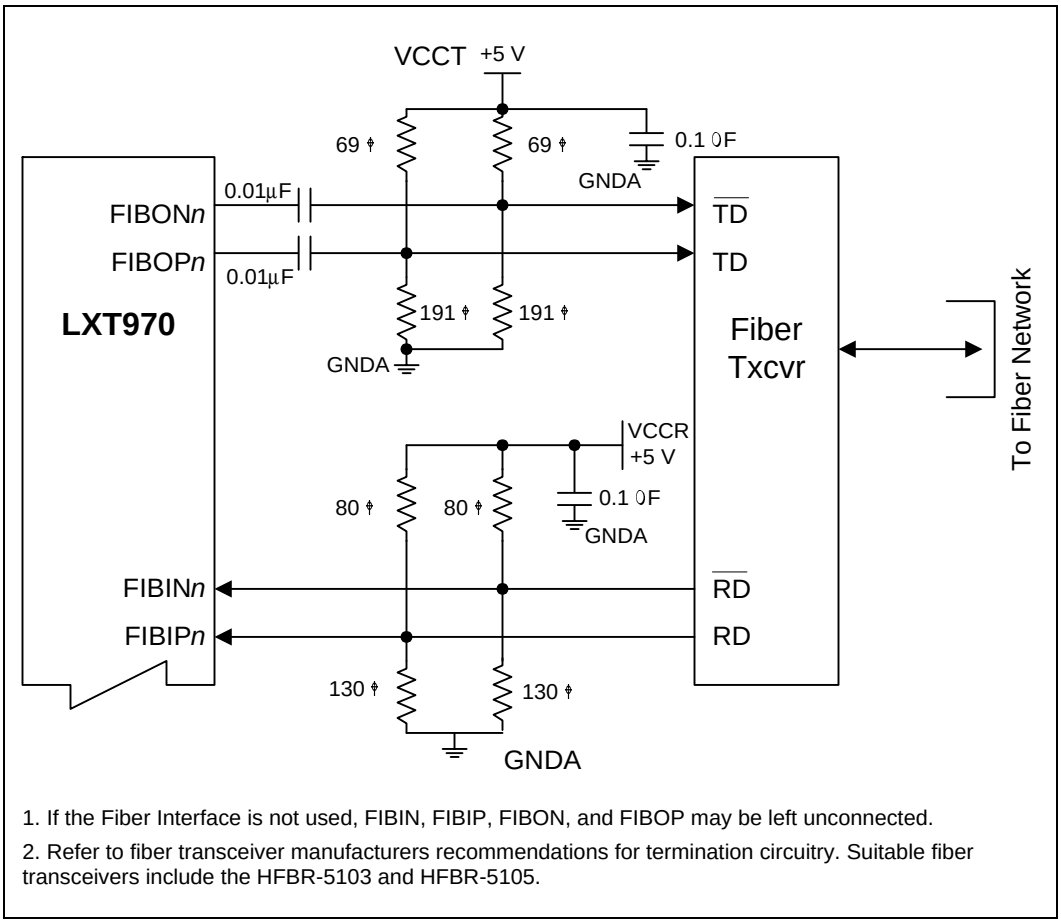
6.0 Fiber Interface

The Pseudo-ECL (PECL) interface to a fiber-optic transceiver is shown in Figure 10.

The LXT970 transmit output (FIBOP/N) is biased to a 1V level. Most fiber transceivers require that their inputs be biased between 3 and 4V. The optimal bias point for one leading manufacturer is 1.3V below VCC. The signals are AC-coupled to allow external biasing. The 69/191Ω combination shown provides a 3.5V, 50Ω bias to the fiber transceiver input.

Most fiber transceiver outputs are emitter-follower stages that must be biased to 3.0V. This is within the 2-5V range of the LXT970 FIBIP/N inputs, which means that DC-coupling can be used for these signals. The 80/130Ω resistor combination shown provides a 3.0V, 50Ω bias.

Figure 10. PECL Interface Circuitry



1. If the Fiber Interface is not used, FIBIN, FIBIP, FIBON, and FIBOP may be left unconnected.
2. Refer to fiber transceiver manufacturers recommendations for termination circuitry. Suitable fiber transceivers include the HFBR-5103 and HFBR-5105.

7.0 Magnetic and Crystal Reference

7.1 Magnetics Information

The LXT970 requires a 1:1 ratio for both the receive and the transmit transformers. Refer to Table 2 for magnetics requirements. Magnetics are available from various manufacturers. See *AN073 — Magnetic Manufacturers* for a complete cross reference list of manufacturers and part numbers. It is the responsibility of the system designer to ensure that all components, both individually and collectively, are suitable for the intended application

Table 2. Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Turns Ratio	–	1:1	–	–	
Insertion Loss	0.0	–	1.1	dB	
Primary Inductance	350	–	–	µH	
Transformer Isolation	–	2	–	kV	
Differential to common mode rejection	–	–	-40	dB	.1 to 60 MHz
	–	–	-35	dB	60 to 100 MHz
Return Loss	–	–	-10	dB	80 MHz
Rise Time	2.0	–	3.5	ns	10% to 90%

7.2 Crystal Information

The LXT970 requires a parallel-resonant fundamental-mode crystal that meets the specifications as shown in Table 3. Crystal manufacturers and part numbers are listed in Table 4. Designers should test and validate all crystals before committing to a specific component.

Table 3. Crystal Requirements

Parameter	Min	Nom	Max	Units
Frequency	–	25.0	–	MHz
Frequency Stability[1]	–	–	±100	ppm
1. Test Condition = -40°C - +85°C.				

Table 4. Crystal Manufacturers

Manufacturer	Part Number
Epson America	MA-505-25.000M
Caliber Electronics	AA18C1-25.000MHz

8.0 Additional Layout Considerations

8.1 Clock Circuit (XO/XI pins)

The LXT970 requires a stable clock reference, which may be accomplished three ways:

- Supply a 100 ppm, 25 MHz, fundamental-mode, parallel-resonant crystal to the XO (exciter) and XI (input) pins.
- Supply a digitally generated 25 MHz clock to the XI pin (XO is left open).
- Ground the XI input, leave the XO output open and supply a 2.5 MHz or 25 MHz clock to the TX_CLK pin on the MII interface. Normally TX_CLK is an output, however when XI is grounded, it becomes an input.

The following constraints apply when XI is used as the clock reference:

- A CMOS equivalent level (V_{IH} >3.2V) is required.
- The device will operate at 10 Mbps and 100 Mbps.
- Shunt capacitance of the XI and XO pin is 3 pF.
- To drive multiple 970s from the same crystal, excite the crystal using the XO output of the closest 970 (leave the other XO outputs unconnected).

The following constraints apply when using TX_CLK as the clock reference:

- A TTL voltage level (V_{IH} >2.0V) is required.
- Jitter less than 0.5 ns.
- With a 2.5 MHz input, the 970 will auto-negotiate and/or operate a 10 Mbps link.
- With a 25 MHz input, the 970 will auto-negotiate and/or operate a 10/100 Mbps link.

8.2 RBIAS

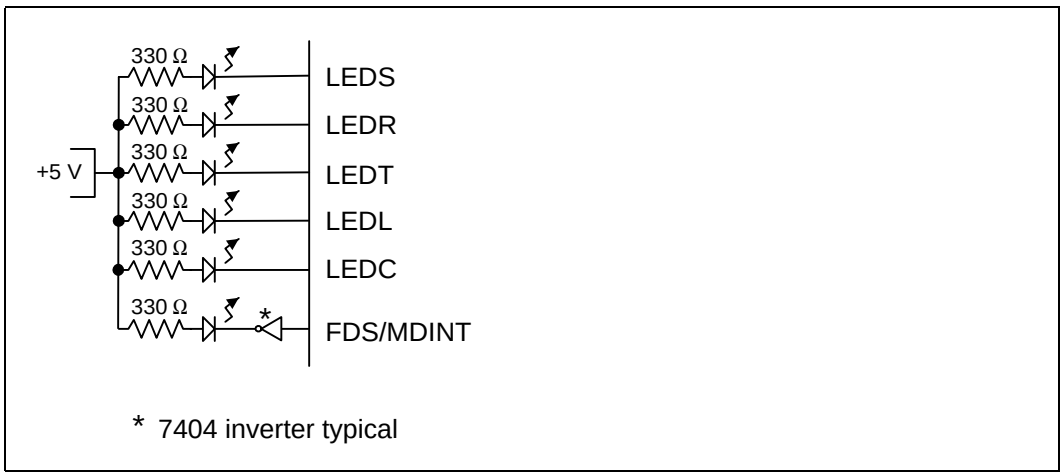
A 1%, 22.1 kΩ resistor must be attached to the RBIAS input of the LXT970. This resistor should be placed as close as possible to the RBIAS pin. One side of the resistor should be connected to the RBIAS pin with a short, direct trace without any vias. The other side of the resistor should be attached to ground. No high-speed signals should be run directly through this area.

8.3 LED Pins

The LXT970 provides five 10 mA LED drivers (transmit, receive, collision, link and speed). These outputs are not open drain and are active Low. The transmit, receive, and collision LEDs are automatically extended for 100 ms. Via software, the collision LED can be programmed to operate as an activity LED (bit 19.7:6).

The LXT970 also provides FDS/MDINT, which can directly drive a high-efficiency LED to indicate duplex status. See Figure 11 for LED and FDS termination circuitry. The 7404 inverter provides additional current to drive a standard LED and inverts the signal to activate the LED on full-duplex. When bit 17.1 = 0 (default), FDS/MDINT indicates duplex status. High = full-duplex, Low = half-duplex.

Figure 11. LED Termination Circuitry



8.4 Hardware Control Interface

Some of the inputs in this interface (MF<4:0>) are dual-function inputs that accept one of four (quaternary) voltage levels. These levels are 5.0V, 3.5V, 1.5V, and 0V. To generate the voltage levels for these inputs requires three resistors attached in a totem-pole configuration between V_{CC} and ground. Suitable values for the resistors can be anywhere from 1 kΩ to 10 kΩ. One totem-pole can be used to drive the MF inputs on an unlimited number of LXT970 devices. The rest of the inputs are simple binary inputs. Refer to the LXT970 data sheet for information on how to configure this interface.

8.5 MII Interface

The MII interface of the LXT970 was designed to drive an MII cable. Therefore the output circuits of all the signals driven by the LXT970 are fairly hefty and can easily source 50-60 mA. These include RX_DV, RX_CLK, RX_ER, RX_D<4:0>, CRS, COL, and TX_CLK.

Series termination resistors are strongly advised on all output signals, even if the signal trace is very short, in order to avoid undershoot and overshoot. The resistance value should be 13Ω less than the nominal trace impedance. If this is not known, use a 55Ω resistor value. A bulk 10 uF capacitor is also advised between $V_{CCI/O}$ and GND near the device.

By supplying the $V_{CCI/O}$ pin with the appropriate supply voltage (5V or 3.3V) the MII interface can be made to operate at either range. However, when the MII is operating at 3.3V, it is not 5V tolerant. Always power up $V_{CCI/O}$ before the MII inputs.

Be extremely cautious when laying out the MDC trace. Avoid “tree” configurations. In multi-port designs, glitches on the MDC signal can cause a read operation intended for one device to become a write operation for another device.