# Intel® StrongARM* SA-1110 Microprocessor

## Developer's Manual

*October 2001*

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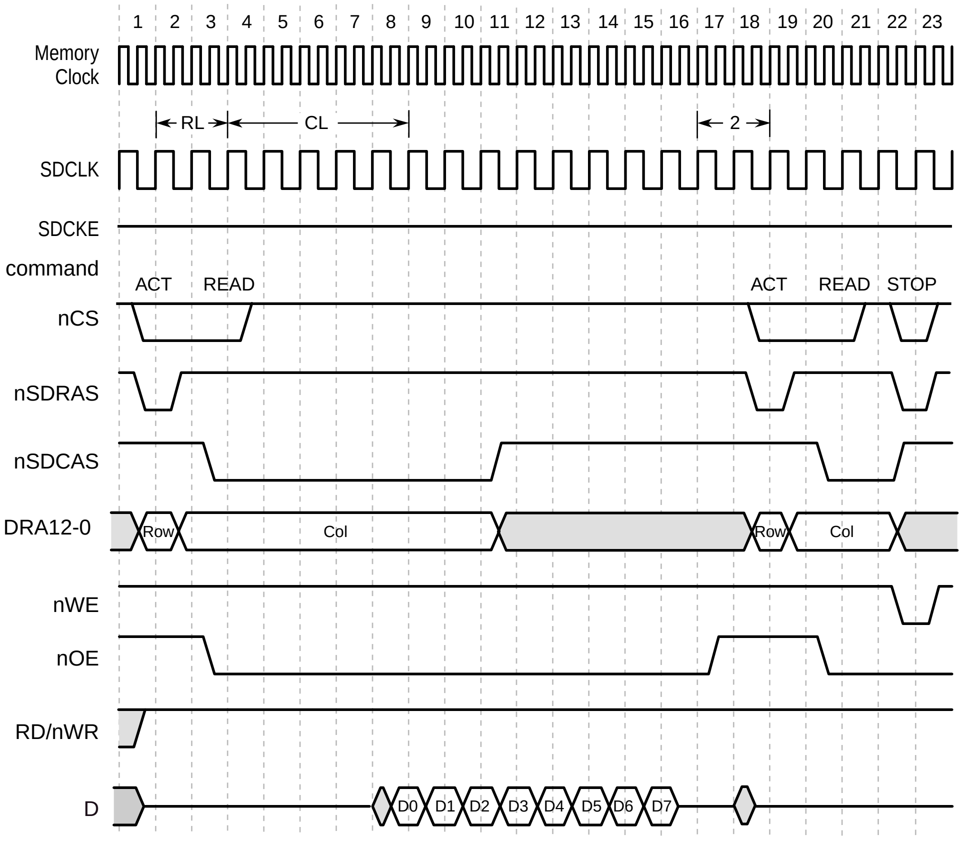
**Figure 10-18. SMROM Eight-Beat and Two-Beat Timing for 2 M x 16 Bit Organization (32 Mbit) at Half-Memory Clock Frequency (MDREFR:K0DB2=1)**



**Contents of SMROM/DRAM register fields:**

RL=2 cycle SMCNFG:CLO=4 (CL=5 cycle)
SMCNFG:RA0=4

last ← time first

MDCAS00=0101 0101 0101 0101 0101 0101 0111 1111(binary)
MDCAS01=0101 0101 0101 0101 0101 0101 0101 0101(binary)

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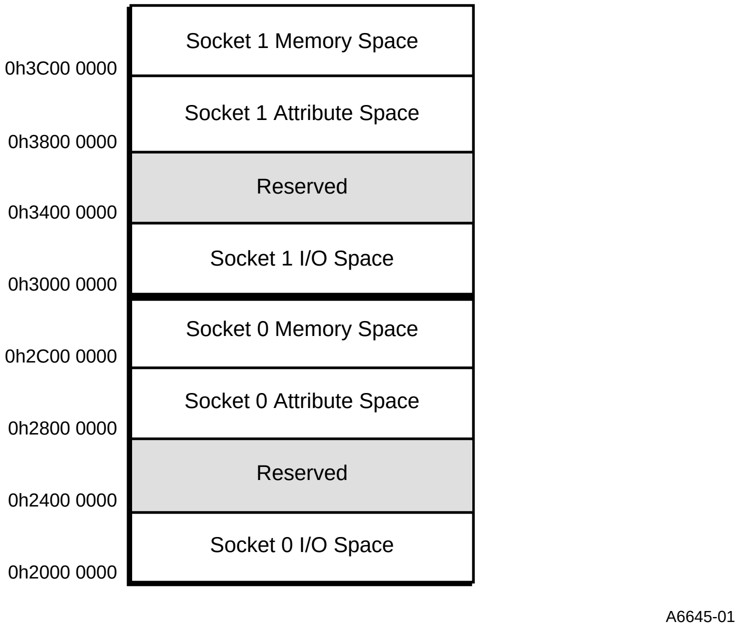
## 10.7 PC-Card Overview

The SA-1110 PC-Card interface provides controls for one PC-Card card slot with a PSKTSEL pin for support of a second slot. This 16-bit host interface supports 8- and 16-bit peripherals and handles common memory, I/O, and attribute memory accesses. The interface does not support the PC-Card DMA protocol. The duration of each access is based on an internally generated clock that is programmed per address space by fields within the MECR register. Figure 10-19 shows the memory map for the PC-Card space.

### Figure 10-19. PC-Card Memory Map



The PC-Card memory space is divided into eight partitions, four for each card slot. The four partitions for each card slot are common memory, I/O, attribute memory, and a reserved space. Each partition starts on a 64 Mbyte boundary. Pins A[25:0], nPREG, and PSKTSEL are driven at the same time. nPCE1 and nPCE2 are driven at address time for memory and attribute accesses. For I/O accesses, the value of nPCE1 and nPCE2 depends on the value of nIOIS16 and thus will be valid a finite time after nIOIS16 is valid.

Common memory and attribute accesses assert the nPOE or nPWE control signals. Memory and attribute space is 16 bits wide by definition.

I/O accesses assert the nIOR or nIOW control signals and use the nIOIS16 input signal to determine the bus width of the transfer (8 or 16 bits). Transfers always start assuming a 16-bit bus. After the address has been placed on the bus, an I/O device may respond by asserting nIOIS16 to indicate that it can perform the transfer in a single 16-bit transfer. If nIOIS16 is not asserted within the proper timeframe, the address is assumed to be to two 8-bit registers and the transfer is completed as two consecutive 8-bit transfers on the low byte lane, D[7:0], with:

1) nPCE2 deasserted,
2) nPCE1 asserted,
3) A0 = 0 for the first 8-bit transfer, and
4) A0 = 1 for the second 8-bit transfer.

***Note:*** The SA-1110 uses nPCE2 to indicate to the expansion device that the upper half of the data bus, D[15:8], will be used for the transfer and nPCE1 to indicate that the lower half of the data bus, D[7:0], will be used.

## 10.7.1 8-, 16-, and 32-Bit Data Bus Operation

The SA-1110 PC-Card interface supports only the 8- and 16-bit data bus operation outlined in the PC-Card specification; the 32-bit operation supported by the SA-1110 is outside the scope of the 32-bit operation described in the PC-Card specification. The SA-1110 PC-Card interface's 32-bit operating mode is intended for use as a nonstandard expansion bus for communication with customer-designed logic. The operation is fairly simple; if a word read or write is performed to PC-Card memory space, then the entire 32-bit bus is read or written.

Normal PC-Card operations should be performed using byte or half-word accesses only. 32-bit accesses should be word aligned and only to "16-bit" space, as opposed to 8-bit space. Memory and attribute space is 16 bits by definition. However, I/O space may be 8- or 16-bit depending upon the state of the nIOIS16 input pin. 32-bit accesses to I/O space require the target to assert nIOIS16.

For 32-bit accesses, the only size information present on the bus is the assertion of the nPCE1 and nPCE2 pins. This is the same information that is present during half-word accesses. As such, there is no way to determine by monitoring the SA-1110 pins whether the access is a half-word or word. This information can be derived only though a user-defined address decode external to the SA-1110. The following table shows the operation of the PC-Card interface and its relation to data width.

| Access Type | Data Bus Width<br>1 = 16 Bit<br>0 = 8 Bit | Address [1:0] | Resulting Operation |
|---|---|---|---|
| Word | 1 | 00 | Word read or write, nPCE1 and nPCE2 asserted (low). nIOIS16 must be asserted for I/O space. |
| | | 1x | Undefined operation. |
| | | x1 | Undefined operation. |
| | 0 | xx | Undefined operation. |
| Half-word | 1 | x0 (even) | Single half-word access, nPCE1 and nPCE2 asserted (low). nIOIS16 must be asserted for I/O space. |
| | | x1 (odd) | Undefined operation. |
| | 0 | x0 (even) | Two-byte accesses, both on the lower byte lane. Even access first (nPCE1 asserted and nPCE2 deasserted for both). |
| | | x1 (odd) | Undefined operation. |
| Byte | 1 | x0 (even) | Load or store byte on the lower byte lane (nPCE1 asserted, nPCE2 deasserted). |
| | | x1 (odd) | Load or store byte on the upper byte lane (nPCE1 deasserted, nPCE2 asserted). |
| | 0 | xx (even or odd) | Load or store byte on the low byte lane (nPCE2 deasserted and nPCE1 asserted). |

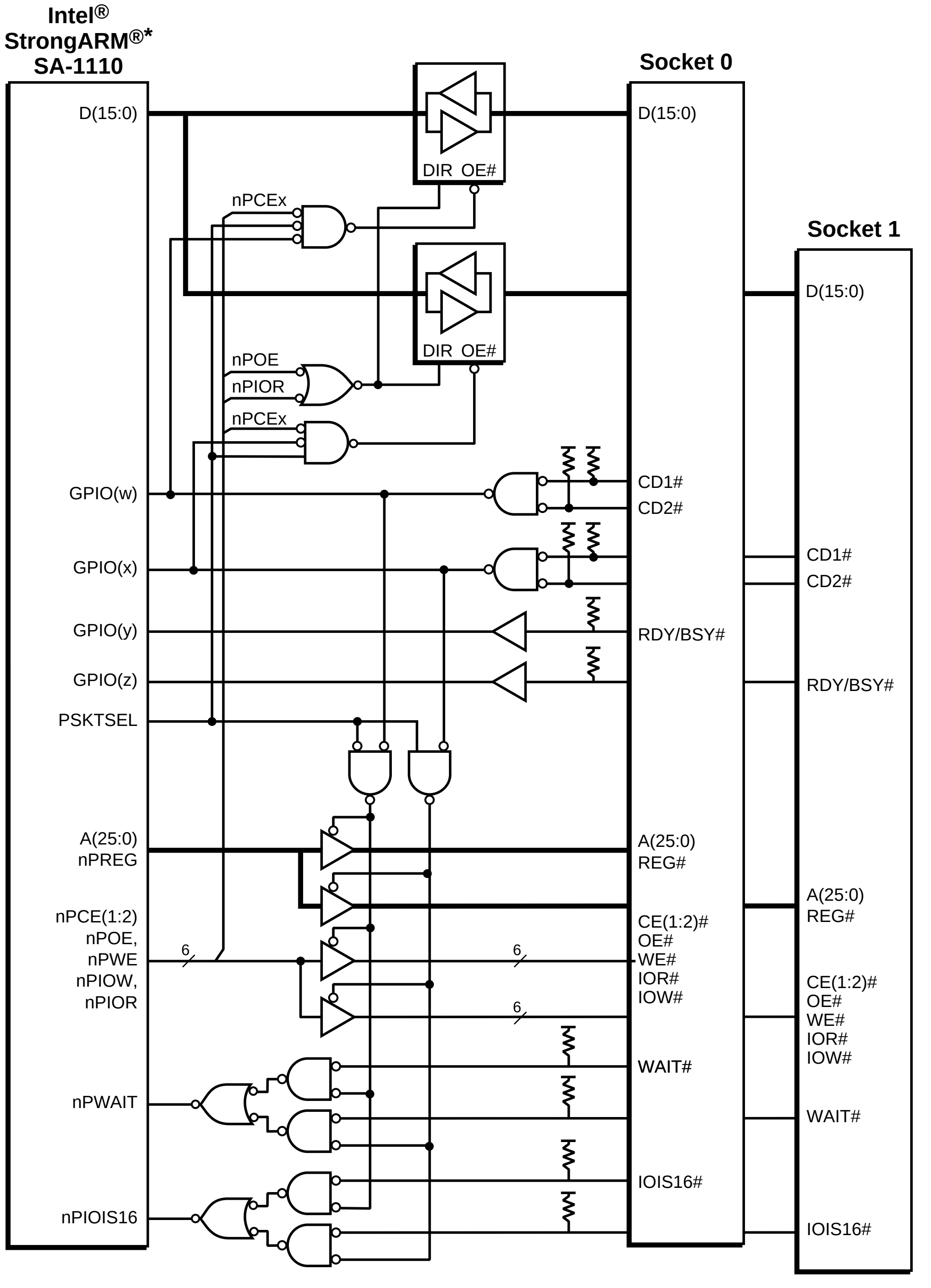
### 10.7.2 External Logic for PC-Card Implementation

The SA-1110 requires external logic to complete the PC-Card socket interface. Figure 10-20 and Figure 10-21 show general solutions for a two– and one–socket configuration. GPIO or memory-mapped external registers are used to control the PC-Card interface's reset, power selection (VCC and VPP), and driver enable lines. For dual–voltage support, level shifting buffers are required for all SA-1110 input signals. Each figure shows the logical connections necessary to support hot insertion capability. Hot insertion capability requires the sockets to be electrically isolated from each other and from the remainder of the memory system.

***Note:*** If one or both of these features (hot insertion and dual–voltage) is not required, then the logic related to the feature which is not required may be eliminated.

The pull-ups shown are included for compliance with *PC Card Standard - Volume 2 - Electrical Specification*. For low-power systems, it is recommended to remove power from these pull-ups during sleep to avoid unnecessary power consumption. The CD1# and CD2# signals have been "OR'ed" before being provided to the SA-1110. This signal is then routed into a GPIO pin for interrupt capability. Similarly, RDY/BSY# is routed to a GPIO pin. The INPACK# signal is not used. In the data bus transceiver control logic, it is recommended that nPCE1 control the enable for the low byte lane and nPCE2 control the enable for the high byte lane.

### Figure 10-20. PC-Card External Logic for a Two-Socket Configuration



Note: For pull-up resistors shown in this figure, recommend 10K ohm resisters connected to socket/card supply voltage.

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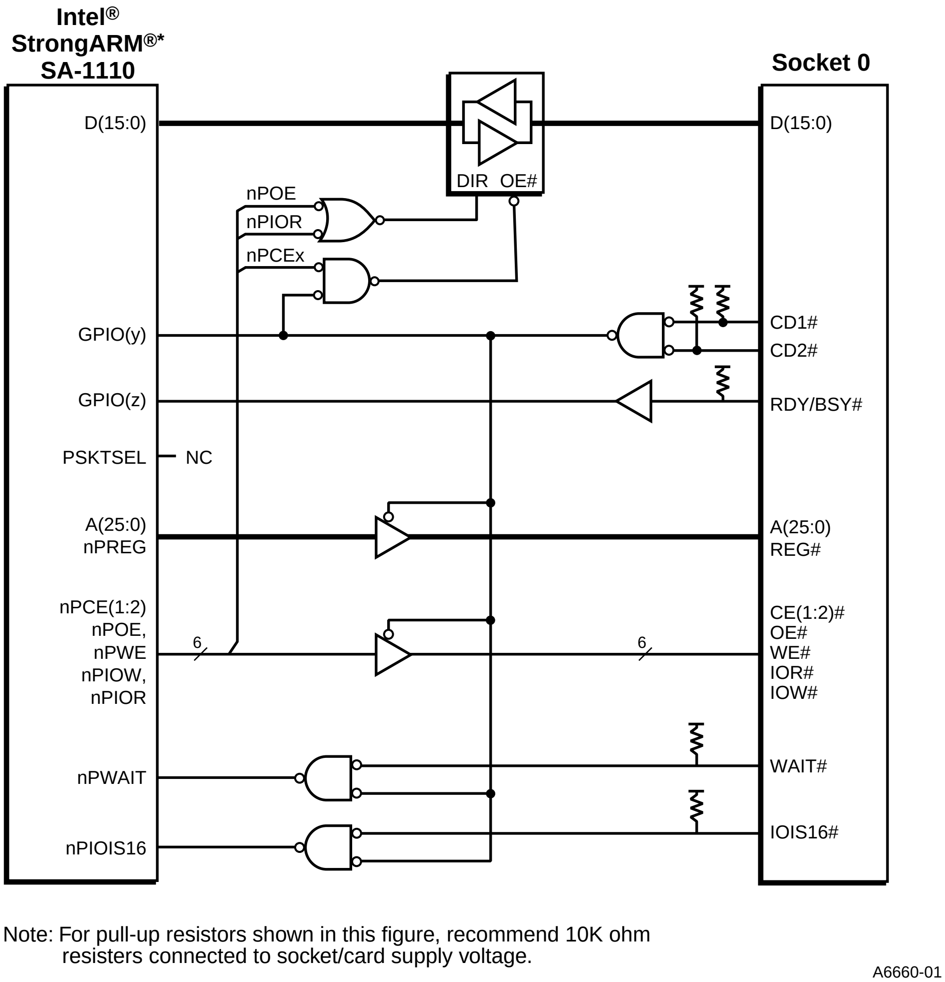
### Figure 10-21. PC-Card External Logic for a One-Socket Configuration

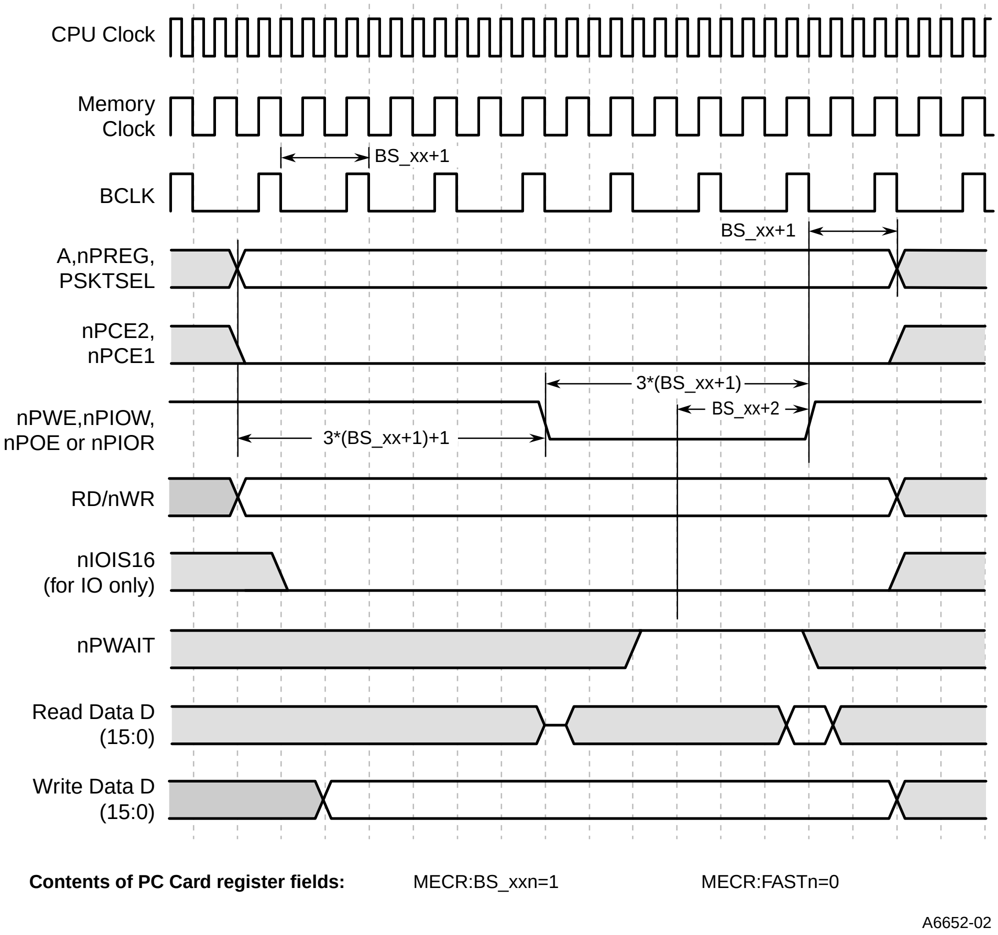


Note: For pull-up resistors shown in this figure, recommend 10K ohm resisters connected to socket/card supply voltage.

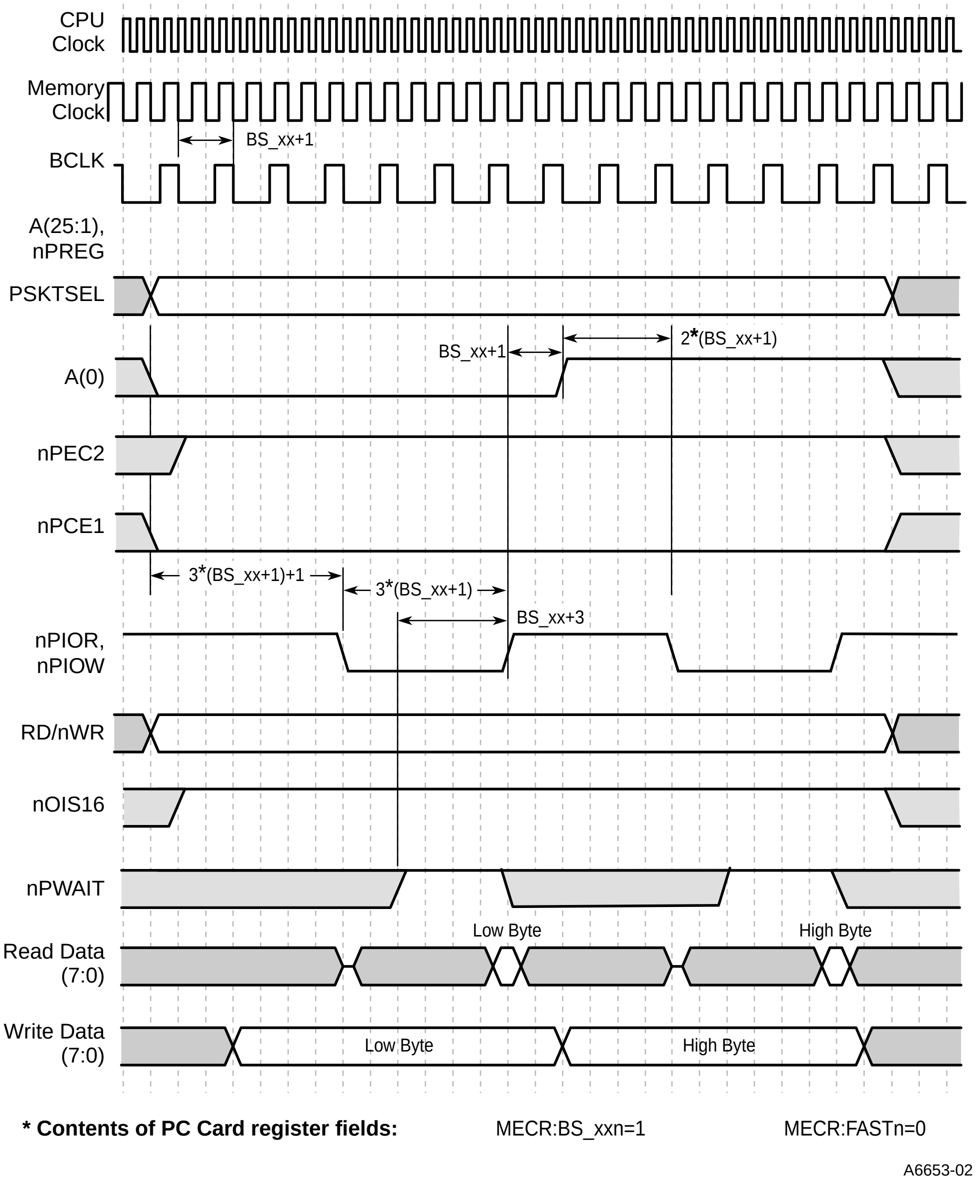
## 10.7.3 PC-Card Interface Timing Diagrams and Parameters

Figure 10-22 shows a 16-bit access to a 16-bit memory or I/O device. The parameter, BS, is programmed in the MECR register. When common memory is accessed, the MECR:BSM0 or MECR:BSM1 field is used, depending on whether card socket 0 or 1 is addressed. MECR:BSIO0,1 is used for I/O accesses and MECR:BSA0,1 is used for access to attribute memory. Figure 10-23 and Figure 10-24 show the appropriate setting of BS_xx = 0b00001.

**Figure 10-22. PC-Card Memory or I/O 16-Bit Access**



## Figure 10-23. PC-Card I/O 16-Bit Access to 8-Bit Device



*** Contents of PC Card register fields:** MECR:BS_xxn=1 MECR:FASTn=0

Timing parameters are in memory clock cycle units. All are minimums except as noted:

Address access time:

| | | |
|---|---|---|
| 6*(BS_xx+1) + 1 | half-word or first byte | FAST=0 |
| 5*(BS_xx+1) | second byte | FAST=0 |
| 4*(BS_xx+1) + 1 | half-word or first byte | FAST=1 |
| 4*(BS_xx+1) | second byte | FAST=1 |

Command (nPOE, nPWE, nPIOR, nPIOW) assertion time: 3*(BS_xx+1)

Address setup to command assert:

| | | |
|---|---|---|
| 3*(BS_xx+1) + 1 | half-word or first byte | FAST=0 |

| | | |
|---|---|---|
| 2*(BS_xx+1) | second byte | FAST=0 |
| 1*(BS_xx+1) + 1 | half-word or first byte | FAST=1 |
| 1*(BS_xx+1) | second byte | FAST=1 |

Address hold after command deassertion: BS_xx+1

nPWAIT valid after command assertion (max): 2*(BS_xx+1) - 2

Chip enable (nPCE1,2) setup to nPOE, nPWE assert:

| | |
|---|---|
| 3*(BS_xx+1) + 1 | FAST=0 |
| 1*(BS_xx+1) + 1 | FAST=1 |

Chip enable (nPCE1,2) setup to nPIOR, nPIOW assert:

| | | |
|---|---|---|
| 3*(BS_xx+1) + 1 - (nIOIS16 delay from address) | half-word or first byte | FAST=0 |
| 2*(BS_xx+1) - (nIOIS16 delay from address) | second byte | FAST=0 |
| 1*(BS_xx+1) + 1 - (nIOIS16 delay from address) | half-word or first byte | FAST=1 |
| 1*(BS_xx+1) - (nIOIS16 delay from address) | second byte | FAST=1 |

Chip enabled hold from command deassert: BS_xx+1

See Chapter 13, “AC Parameters” for actual AC timing.

## 10.8 Alternate Memory Bus Master Mode

The SA-1110 supports the existence of an alternate master on the DRAM memory bus. The alternate master is given control of the bus using a hardware handshake. This handshake is performed through MBREQ and MBGNT, which are invoked through the alternate functions on GPIO 22 and GPIO 21, respectively. When the alternate master wants to take control of the memory bus, it asserts MBREQ (GPIO 22). The SA-1110 will complete any pending or in-progress memory operation and any outstanding DRAM refresh cycle. It then deasserts SDCKE 1 and tristates all memory bus pins used with DRAM bank 0 (nRAS/nSDCS 0, A[25:0], nOE, nWE, nSDRAS, nSDCAS, SDCLK 1, D[31:0], nCAS/DQM[3:0]). All other memory and PC-Card pins remain driven, including SDCLK 2 is driven to 0, SDCLK 0 is driven to 0, and SDCKE 0 is driven to 1. The RD/nWR pin will remain low. Then the SA-1110 will assert MBGNT (GPIO 21), the alternate master should start driving all pins (including SDCLK 1), and the SA-1110 will re-assert SDCKE 1. The grant sequence and timing are as follows; the Tmem unit of time is the memory clock period (twice the CPU clock period):

- Alternate master asserts MBREQ
- SA-1110 deasserts SDCKE 1 at time (t)
- SA-1110 begins to tristate DRAM outputs at time (t + 1*Tmem)
- SA-1110 asserts MBGNT at time (t + 2*Tmem)
- Alternate master begins to drive DRAM outputs prior to time (t + 3*Tmem)
- SA-1110 asserts SDCKE 1 at time (t + 4*Tmem)

During the tristate period, both MBREQ and MBGNT remain high and an external device may take control of the tristated pins. The external device should drive all the tristated pins even if some are not actually used. Otherwise, floating inputs may cause excessive crossover current and/or erroneous SDRAM commands. Note that during the tristate period, the SA-1110 is unable to perform DRAM refresh cycles. The alternate master must assume the responsibility for DRAM integrity during this period. It is recommended that the system be designed such that the period of alternate mastership is limited to much less than the refresh period, or that the alternate master implement a refresh counter making it capable of performing refresh at the proper intervals.