Intel® StrongARM* SA-1111 Microprocessor Companion Chip

Developer's Manual

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PCMCIA Interface 12

The PCMCIA interface block provides control logic and a complete set of signal buffers for one PCMCIA card and one CF (Compact Flash) card. Alternatively, with an external address buffer it can support two PCMCIA cards. The control logic and built-in buffers eliminate ten or more external “glue” and buffer/transceiver components, providing a highly-integrated and lower power solution for the creation of complete systems.

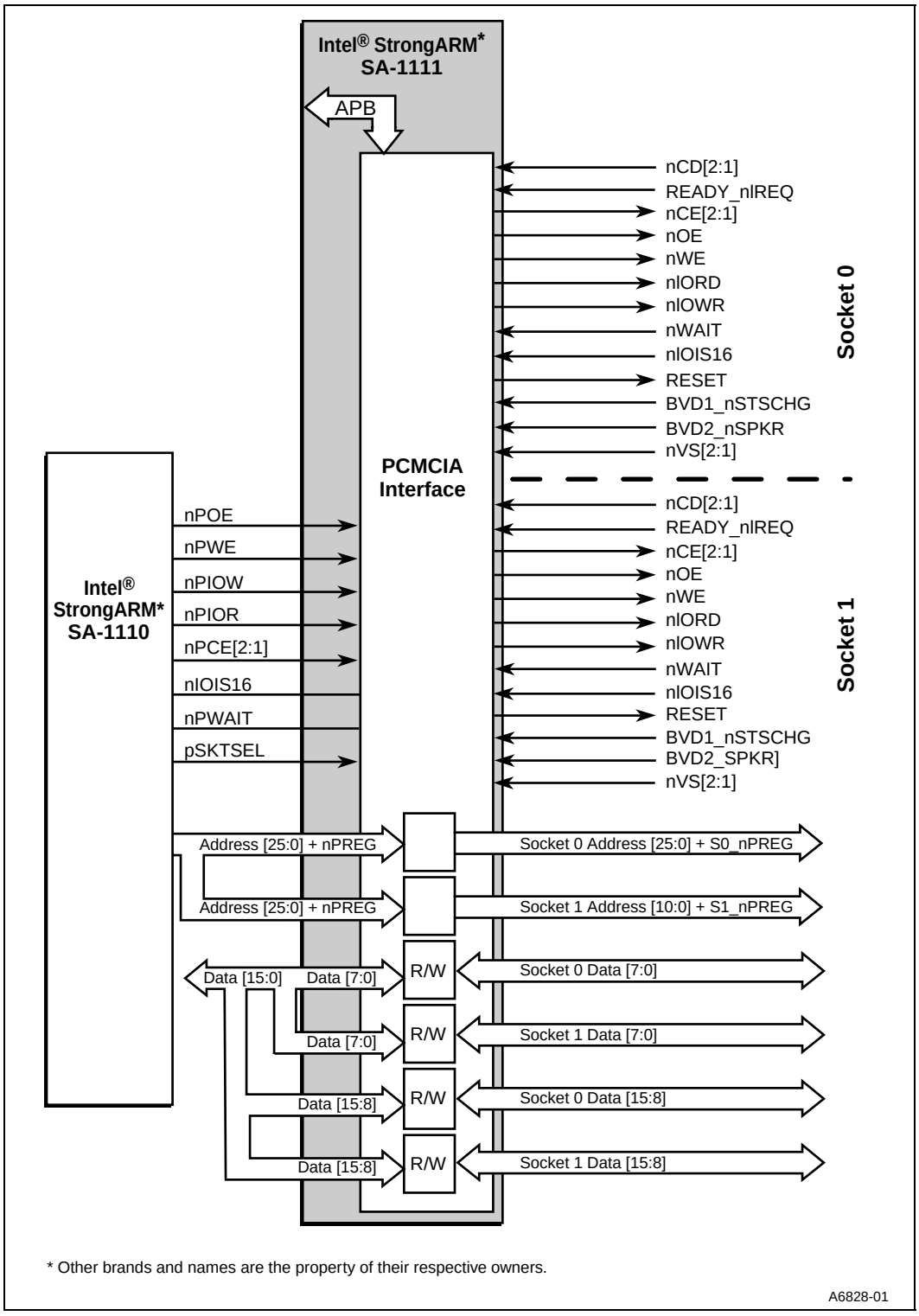
Four GPIOs are available to control an external power-selection and switching device, which supplies power to the card sockets.

The interface also provides facilities for controlling the state of the pins when the Intel® StrongARM* SA-1111 Microprocessor Companion Chip (SA-1111) is in *sleep* mode.

12.1 PCMCIA Interface Block Diagram

Figure 12-1 shows the block diagram for the PCMCIA interface.

Figure 12-1. PCMCIA Interface Block Diagram



12.2 Functional Description

12.2.1 PCMCIA/CF Address and Data Buffers

Buffers are built into the SA-1111 for all address and data signals to one PCMCIA slot and one CF slot. The PCMCIA slot supports both 3.3V and 5.0V PCMCIA cards.

When the device is in *Sleep* mode, the state of PCMCIA and CF address and data pins changes to a programmable value (Hi-Z or logic LOW).

12.2.2 Voltage Control

Four GPIO pins are provided for programming an external voltage source. This allows the interface to accommodate PCMCIA cards of different operating voltages. These pins are controlled by GPIO register writes (see Chapter 10).

12.2.3 Reset Signals

A single logic output is provided for each socket to allow resetting the PCMCIA or CF card. Both signals are active high, and are asserted when the SA-1111 is in *reset*, or the relevant bit in the Control Register is set (refer to Section 12.6.2).

When the SA-1111 is in *sleep* mode the reset signals are either tristated (off) or low, depending on the relevant bit in the sleep state register (refer to Section 12.6.3).

12.2.4 Control Signals

Seven control lines are driven to each socket: nPREG, nOE, nWE, nIOW, nIOR, nCE1, and nCE2. The control lines operate except when the SA-1111:

- Enters sleep mode.
  These lines can be tristated or driven high (refer to Section 12.6.3).
- Sets its float bits in the Control Register (PCCR).
  These control lines float in *normal* mode, when appropriately set via control register bits, and in and *sleep* mode.

Two signals are returned, through the SA-1111, from each card socket to the processor. These are:

- Sx_nIOIS16 (x = 0 or 1) is an acknowledgement from the card that the current address is a valid 16-bit address;
- Sx_nPWAIT (x = 0 or 1) is driven low by the card to extend the length of a transfer.

These pins are inputs on the card interface of the SA-1111; the signal from the selected card is routed to a pin on the SA-1111's processor interface, where it is an output, driven to the processor. Since they are inputs at the card interface, they are unaffected by *Sleep* mode or any register configuration.

12.2.5 Interrupts

Table 12-1 describes the interrupt sources provided by the PCMCIA interface.

Table 12-1. Interrupt Signals

Name	Function
S0_READY_nIREQ	Socket 0 READY_nIREQ pin
S1_READY_nIREQ	Socket 1 READY_nIREQ pin
S0_CDVALID	Socket 0 card detect 0 = Card fully inserted 1 = Card not fully inserted
S1_CDVALID	Socket 1card detect 0 = Card fully inserted 1 = Card not fully inserted
S0_BVD1_STSCHG	Socket 0 BVD1_STSCHG (voltage detect) pin
S1_BVD1_STSCHG	Socket 1 BVD1_STSCHG (voltage detect) pin

12.3 Detailed Signal Descriptions

This section provides detailed signal descriptions for the PCMCIA interface block diagram shown in Figure 12-1.

12.3.1 Intel® StrongARM* SA-1111 Interface Signals.

Table 12-2 describes the SA-1110 interface signals.

Table 12-2. SA-1110 Interface Signals (Sheet 1 of 2)

Signal Name	Description
PKTSEL	PCMCIA socket select. This signal is an input and used to route control, address and data. Signals to one of the PCMCIA sockets. When PSKTSEL is low, socket zero is selected. When PSKTSEL is high, Socket one is selected.
Address <25:0>	Address Inputs. This bus conveys the address for PCMCIA and Compact Flash slots.
Data <15:0>	Bi-directional Data Bus. This bus is driven by the PCCard/Compact Flash Block. Only when either one of nPCE<2:1> is asserted and either nPIOR or nPOE are asserted.
nPCE<2:1>	Card Enable. These signals are inputs, gated within the block, and used to select a PCMCIA card. Bit 2 enables the high byte lane and bit 1 enable the low byte lane.
nIOIS16	IO is 16 bit. This signal is an output and generated as following: IF PSKTSEL is low and Card is fully inserted in socket zero, then nPIOIS16 = S0_nIOIS16; Otherwise if PSKTSEL is high and Card is fully inserted in socket one, then nPIOIS16 = S1_nIOIS16. Otherwise nPIOIS16 = high.
nPIOR	IO Read. This signal is an input and used to generate Sx_nIORD signals.
nPIOW	IO Write. This signal is an input and used to create Sx_nIOW signals.
nPOE	Output Enable. This signal is an input and used to generate Sx_nOE signals.

Table 12-2. SA-1110 Interface Signals (Sheet 2 of 2)

Signal Name	Description
nPREG	REG Select. This signal is an input and used to generate Sx_nREG signals.
nPWAIT	Wait signal. This signal is an output and generated as following: IF PSKTSEL is low, and at least one of nPCE<2:1> is asserted, and Card is fully inserted in socket zero and PCCR<4> is set, then nPWAIT = S0_nWAIT; Otherwise if PSKTSEL is high, and at least one of nPCE<2:1> is asserted, and Card is fully inserted in socket one and PCCR<5> is set, then nPWAIT = S1_nWAIT. Otherwise nPWAIT = high.
NPWE	Write Enable. This signal is an input and used to generate Sx_nWE signals.

12.4 Socket 0 Signals

Table 12-3 lists the socket 0 signals.

Table 12-3. Socket 0 Signals (Sheet 1 of 4)

Signal Name	Description
S0_RESET	Reset. This signal is an output and used to reset the card. This signal needs a weak pull-up on board. The signal is active high and generated by the following way. **If** PCCR<2> = 1 **then** {if in sleep mode, {if PCSSR<0> =0, This signal is tri-stated, elseif This signal is forced to low.} else S0_RESET = PCCR<0> **Else** this signal is tristated.
S0_ADDRESS<25:0>	Address Bus. **If** one of the S0_nCD<2:1> signals is high or PCCR<2> is '0' **Then** The bus is tri-stated; **Else if** it is in sleep mode **Then** {if PCSSR<0> =0, This bus is tri-stated, elseif This bus is forced to low.} **Else If** PSKTSEL is high or both of nPCE<2:1> are high **Then** The whole bus is forced to low; **Else** S0_ADDRESS<25:0> = Address<25:0>.

Table 12-3. Socket 0 Signals (Sheet 2 of 4)

Signal Name	Description
S0_Data<15:0>	Data Bus. PC Card bi-directional data bus. Data is transferred from the PC Card socket to the CPU through this 16-bit bus. Only byte and 16 bit operations are supported. **If** PCCR<2> =1 Then {if in sleep mode {if PCSSR<0> = 0, output is tristated else driven low by SA-1111} else if nPIOR or nPOE is asserted and PSKTSEL is low, output is tristated else driven by SA-1111} **Else** output is tristated.
S0_nPREG	Output to PC Card socket nREG signal. This is an output. **If** PCCR<2> = 1 **Then** {if it is in sleep mode, {if PCSSR<0> =0, This signal is tri-stated, elseif This signal is forced to high.} elseif S0_nCD<2:1> =00 and PSKTSEL =0 then S0_nPREG = nPREG Else S0_nPREG =1} **Else** S0_nPREG is tri-stated.
S0_nCE<2:1>	Card Enable: Output to PC Card socket nCE<2:1> signals. **If** PCCR<2> = 1 **Then** {if it is in sleep mode, {if PCSSR<0> =0, This signal is tri-stated, elseif This signal is forced to high.} elseif S0_nCD<2:1> =00 and PSKTSEL =0 then S0_nCE<2:1>= nPCE<2:1> Else S0_nCE<2:1> =11b} **Else** S0_nCE is tri-stated.
S0_nOE	Output Enable. Output to PC Card socket nOE signal. If PCCR<2> = 1 **Then** {if it is in sleep mode, {if PCSSR<0> =0, This signal is tri-stated, elseif This signal is forced to high.} elseif S0_nCD<2:1> =00 and PSKTSEL =0 then S0_nOE = nPOE Else S0_nOE =1} Else S0_nOE is tri-stated.

Table 12-3. Socket 0 Signals (Sheet 3 of 4)

Signal Name	Description
S0_nWE	Write Enable. Output to PC Card socket nWE signal. **If** PCCR<2> = 1 **Then** {if it is in sleep mode, {if PCSSR<0> =0, This signal is tri-stated, elseif This signal is forced to high.} elseif S0_nCD<2:1> =00 and PSKTSEL =0 then S0_nWE= nPWE Else S0_nWE =1} **Else** S0_nWE is tri-stated.
S0_nIORD	IO Read. Output to PC Card socket nIOR signal. **If** PCCR<2> = 1 Then {if it is in sleep mode, {if PCSSR<0> =0, This signal is tri-stated, elseif This signal is forced to high.} elseif S0_nCD<2:1> =00 and PSKTSEL =0 then S0_nIORD = nPIOR Else S0_nIORD =1} **Else** S0_nIORD is tri-stated.
S0_nIOWR	IO Write. Output to PC Card socket nPIOW signal. **If** PCCR<2> = 1 **Then** {if it is in sleep mode, {if PCSSR<0> =0, This signal is tri-stated, elseif This signal is forced to high.} elseif S0_nCD<2:1> =00 and PSKTSEL =0 then S0_nIOWR = nPIOW Else S0_nIOWR =1} **Else** S0_nIOWR is tri-stated.
S0_nWAIT	Wait Signal. Input from PC Card Socket nWAIT. This signal generates the nPWAIT signal.
S0_nIOS16	IO is 16 bit. Input from PC Card Socket nIOIS16. This signal generates the nIOIS16 signal and can be read from Status Register.
S0_READY_nIREQ	Ready/Interrupt Request. Input from PC Card Socket RDY/nIRQ signal. This signal can be accessed through Status Register and used as an interrupt source.
S0_BVD2_nnSPKR	Socket 0 VDD voltage sense signal/audio digital speaker. This signal can be read from Status Register.
S0_BVD1_nSTSCHG	Socket 0 VDD voltage sense signal/card status changed. This signal can be read from Status Register and used as an interrupt source.
S0_nVS<2:1>	Socket 0 VSS voltage sense signals. These signals can be accessed through Status Register.

Table 12-3. Socket 0 Signals (Sheet 4 of 4)

Signal Name	Description
S0_nCD<2:1>	Card Detect. Input from PC Card Socket Card Detect signals nCD<2:1>. These signals are used to generate S0_CDVALID. When both of S0_nCD<2:1> are low, S0_CDVALID= 0; otherwise S0_CDVALID = 1. The S0_CDVALID is used as an interrupt source and can be read from Status Register.
PCMCIA_PWR<3:0>	Voltage Control. This allows the interface to accommodate PCMCIA cards of different operating voltages. This is done through GPIO_A<3:0> – see Chapter 10.

12.5 Socket 1 Signals

Table 12-4 lists the socket 1signals.

Table 12-4. Socket 1 Signals (Sheet 1 of 3)

Signal Name	Description
S1_RESET	Reset. This signal is an output and used to reset the card. This signal needs a weak pull-up on board. The signal is active high and generated as follows. **If** PCCR<3> = 1 **then** {if in sleep mode, {if PCSSR<1> =0, This signal is tristated, elseif This signal is forced to low.} else S1_RESET = PCCR<1> **Else** this signal is tristated.
S1_ADDRESS<10:0>	Address Bus. **If** one of the S1_nCD<2:1> signals is high or PCCR<3> is '0' **Then** The bus is tri-stated; **Elseif** it is in sleep mode **Then** {if PCSSR<1> =0, This bus is tri-stated, elseif This bus is forced to low.} **Else If** PSKTSEL is high or both of nPCE<2:1> are high **Then** The whole bus is forced to low; **Else** S1_ADDRESS<10:0> = Address<10:0>.
S1_Data<15:0>	Data Bus. PC Card bi-directional data bus. Data is transferred from the PC Card socket to the CPU through this 16-bit bus. Only byte and 16 bit operations are supported. **If** PCCR<3> =1 Then {if in sleep mode {if PCSSR<1> = 0, output is tristated else driven low by SA-1111} else if nPIOR or nPOE is asserted and PSKTSEL is low, output is tristated else driven by SA-1111} **Else** output is tristated.

Table 12-4. Socket 1 Signals (Sheet 2 of 3)

Signal Name	Description
S1_nPREG	Output to PC Card socket nREG signal. This is an output. **If** PCCR<3> = 1 **Then** {if it is in sleep mode, {if PCSSR<1> =0, This signal is tri-stated, elseif This signal is forced to high.} elseif S1_nCD<2:1> =00 and PSKTSEL =0 then S1_nPREG = nPREG Else S1_nPREG =1} **Else** S1_nPREG is tri-stated.
S1_nCE<2:1>	Card Enable: Output to PC Card socket nCE<2:1> signals. **If** PCCR<3> = 1 **Then** {if it is in sleep mode, {if PCSSR<1> =0, This signal is tristated, elseif This signal is forced to high.} elseif S1_nCD<2:1> =00 and PSKTSEL =0 then S1_nCE<2:1>= nPCE<2:1> Else S1_nCE<2:1> =11b} **Else** S1_nCE is tristated.
S1_nOE	Output Enable. Output to PC Card socket nOE signal. If PCCR<3> = 1 **Then** {if it is in sleep mode, {if PCSSR<1> =0, This signal is tristated, elseif This signal is forced to high.} elseif S1_nCD<2:1> =00 and PSKTSEL =0 then S1_nOE = nPOE Else S1_nOE =1} Else S1_nOE is tristated.
S1_nWE	Write Enable. Output to PC Card socket nWE signal. **If** PCCR<3> = 1 **Then** {if it is in sleep mode, {if PCSSR<1> =0, This signal is tristated, elseif This signal is forced to high.} elseif S1_nCD<2:1> =00 and PSKTSEL =0 then S1_nWE= nPWE Else S1_nWE =1} **Else** S1_nWE is tristated.

Table 12-4. Socket 1 Signals (Sheet 3 of 3)

Signal Name	Description
S1_nIORD	IO Read. Output to PC Card socket nIOR signal. **If** PCCR<3> = 1 Then {if it is in sleep mode, {if PCSSR<1> =0, This signal is tri-stated, elseif This signal is forced to high.} elseif S1_nCD<2:1> =00 and PSKTSEL =1 then S1_nIORD = nPIOR Else S1_nIORD =1} **Else** S1_nIORD is tri-stated.
S1_IOWR	IO Write. Output to PC Card socket nPIOW signal. **If** PCCR<3> = 1 **Then** {if it is in sleep mode, {if PCSSR<1> =0, This signal is tristated, elseif This signal is forced to high.} elseif S1_nCD<2:1> =00 and PSKTSEL =0 then S1_nIOWR = nPIOW Else S1_nIOWR =1} **Else** S1_nIOWR is tristated.
S1_nWAIT	Wait Signal. Input from PC Card Socket nWAIT. This signal generates the nPWAIT signal.
S1_nIOS16	IO is 16 bit. Input from PC Card Socket nIOIS16. This signal generates the nIOIS16 signal and can be read from Status Register.
S1_READY_nIREQ	Ready/Interrupt Request. Input from PC Card Socket RDY/nIRQ signal. This signal can be accessed through Status Register and used as an interrupt source.
S1_BVD2_nnSPKR	Socket 1 VDD voltage sense signal/audio digital speaker. This signal can be read from Status Register.
S1_BVD1_nSTSCHG	Socket 1 VDD voltage sense signal/card status changed. This signal can be read from Status Register and used as an interrupt source.
S1_nVS<2:1>	Socket 1 VSS voltage sense signals. These signals can be accessed through Status Register.
S1_nCD<2:1>	Card Detect. Input from PC Card Socket Card Detect signalsnCD<2:1>. These signals are used to generate S1_CDVALID. When both of S1_nCD<2:1> are low, S1_CDVALID= 0; otherwise S1_CDVALID = 1. The S1_CDVALID is used as an interrupt source and can be read from Status Register.

12.6 Programmer's Model

This section describes the three registers in the PCMCIA interface.

12.6.1 Status Register (PCSR)

This register allows the reading of various signals within the PCMCIA interface.

Table 12-5. PCSR Bit Descriptions

0x0001808	PCSR	SA-1111 Companion Chip

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																		Socket 1 BVD2	Socket 1 BVD1	Socket 0 BVD2	Socket 0 BVD1	Socket 1 WP	Socket 0 WP	Socket 1 VS2	Socket 1 VS1	Socket 0 VS2	Socket 0 VS1	Socket 1 card detect	Socket 0 card detect	Socket 1 ready	Socket 0 ready
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Type	Description
0	Socket 0 ready	RO	Status of S0_READY_nIREQ
1	Socket 1 ready	RO	Status of S1_READY_nIREQ
2	Socket 0 card detect	RO	0 = Socket 0 card detect 1 and 2 valid
3	Socket 1 card detect	RO	0 = Socket 1 card detect 1 and 2 valid
4	Socket 0 VS1	RO	Socket 0 VS1 - socket 0 voltage sense 1
5	Socket 0 VS2	RO	Socket 0 VS2 - socket 0 voltage sense 2
6	Socket 1 VS1	RO	Socket 1 VS1 - socket 1 voltage sense 1
7	Socket 1 VS2	RO	Socket 1 VS2 - socket 1 voltage sense 2
8	Socket 0 WP	RO	Socket 0 WP (S0_nIOIS16)
9	Socket 1 WP	RO	Socket 1 WP (S1_nIOIS16)
10	Socket 0 BVD1	RO	Socket 0 BVD1_nSTSCHG
11	Socket 0 BVD2	RO	Socket 0 BVD2_nSPKR
12	Socket 1 BVD1	RO	Socket 1 BVD1_nSTSCHG
13	Socket 1 BVD2	RO	Socket 1 BVD2_nSPKR
31:14	—	—	Reserved.

12.6.2 Control Register (PCCR)

This register controls the setting of various output pins in the PCMCIA interface and also allows tristating the control lines. Note that control of the external PCMCIA/Compact Flash power controller is done through GPIO_A<3:0> - see Chapter 10 for details on controlling those pins.

Two bits <5:4> control assertion of nPWAIT on a per-slot basis.

Table 12-6. PCCR Bit Descriptions

0x0001800 PCCR SA-1111 Companion Chip

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								S0PSE	S0PSE	S1_PWAITEN	S0_PWAITEN	S1_FLT	S0_FLT	S1_RST	S0_RST
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Type	Description
0	S0_RST	RW	Socket 0 reset: 1 = assert reset
1	S1_RST	RW	Socket 1 reset: 1 = assert reset
2	S0_FLT	RW	S0 float 0 = Float all S0 control lines
3	S1_FLT	RW	S1 float 0 = Float all S1 control lines
4	S0_PWAITEN	RW	S0_nPWAIT enable
5	S1_PWAITEN	RW	S1_nPWAIT enable
6	S0PSE	RW	If using a 3 V card, set to 0; if using a 5 V card, set to 1.
7	S0PSE	RW	If using a 3 V card, set to 0; if using a 5 V card, set to 1.
31:8	—	—	Reserved.

12.6.3 Sleep State Register (PCSSR)

This register allows setting the state of PCMCIA/CF output pins during *sleep* mode. Note the four voltage control pins are controlled via the regular GPIO control facilities provided by the GPIO registers.

Table 12-7. PCSSR Bit Descriptions

0x0001804 **PCSSR** **SA-1111 Companion Chip**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																														Socket 1	Socket 0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Type	Description
0	Socket 0	RW	Socket 0 control, data, and address pin states in SLEEP mode For more information on sleep state control, see Table 12-8
1	Socket 1	RW	Socket 1 control, data, and address pin states in SLEEP mode For more information on sleep state control, see Table 12-8
31:2	—	—	Reserved.

In sleep state, PCMCIA or CF signal pins are put into a state dependent on the value in the S0CONT or S1CONT bits, as shown in Table 12-8. Bit PCSSR<0> specifies the sleep state of Socket 0 (PCMCIA) output pins, while bit PCSSR<1> controls Socket 1 (CF) pins.

Table 12-8. S0 (PCMCIA) and S1 (CF) Sleep State Control

PCMCIA Signal (x = 0 or 1)	Socket 0: PCSSR<0> = 0	Socket 0: PCSSR<0> = 1	Socket 1: PCSSR<1> = 0	Socket 1: PCSSR<1> = 1
Sx_DATA	Tristate	0	Tristate	0
Sx_ADDRESS	Tristate	0	Tristate	0
Sx_NOE	Tristate	1	Tristate	1
Sx_nIORD	Tristate	1	Tristate	1
Sx_nIOWR	Tristate	1	Tristate	1
Sx_nCE1	Tristate	1	Tristate	1
Sx_nCE2	Tristate	1	Tristate	1
Sx_nWE	Tristate	1	Tristate	1
Sx_Reset	Tristate	0	Tristate	0

12.6.4 Memory Map

Table 12-9 shows the read and write locations in the PCMCIA interface register memory map. See Section 3.2.1 for the PCMCIA interface base address.

Table 12-9. PCMCIA Interface Register Memory Map

Address	Read Location	Write Location
0x0001800	PCCR register	PCCR register
0x0001804	PCSSR register	PCSSR register
0x0001808	PCSR register	Reserved