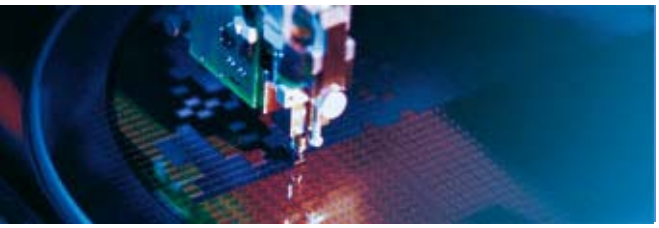
USER MANUAL



APOLLO

Intel Celeron M/Pentium M based EBX Single Board Computer

Rev. 7.0 - April 2009 - ETH_APOLLO_USM

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Revision history

Issue no.	*PCB*	*Date*	*Comments*
A	V1I3	14th June 2005	First full release of manual.
B	V1I4	15th November 2005	Added detailed hardware description.
C	V1I4/V2I1	31st July 2007	Updates for V1Ix and V2Ix board versions.
D	V1I4/V2I1	1st October 2007	Eurotech rebranding.
E	V1I4/V2I1	5th June 2008	Minor updates.
F	V1I4/V2I1	8th December 2008	Minor updates.
G	V1I4/V2I1	2nd April 2009	Minor updates and new branding.

For contact details, see page 144.

Contents

Introduction

The APOLLO is an EBX format, high-performance, high-functionality PC-compatible processor board designed for embedding into OEM equipment. The board is based on the Intel 855GME/ICH4 chipset and supports a range of Intel Pentium M and Celeron M mobile processors to offer a combination of high performance computing features with low power dissipation.

It offers all standard features and connectors found on a PC motherboard including:

- Multiple video ports.
- Audio.
- Two Ethernet ports.
- CF+ CompactFlash® Type II socket.
- Four serial ports, parallel port, IrDA port.
- Primary IDE interface.
- Six USB 2.0 compliant ports.
- Two IEEE1394a-2000 compliant (Firewire) ports.
- General purpose IO and user defined jumpers.

Gigabit Ethernet is a build option on the V1Ix board and a standard feature on the V2Ix boards.

The board is able to run all popular operating systems including Windows XP/ XP Embedded and Linux.

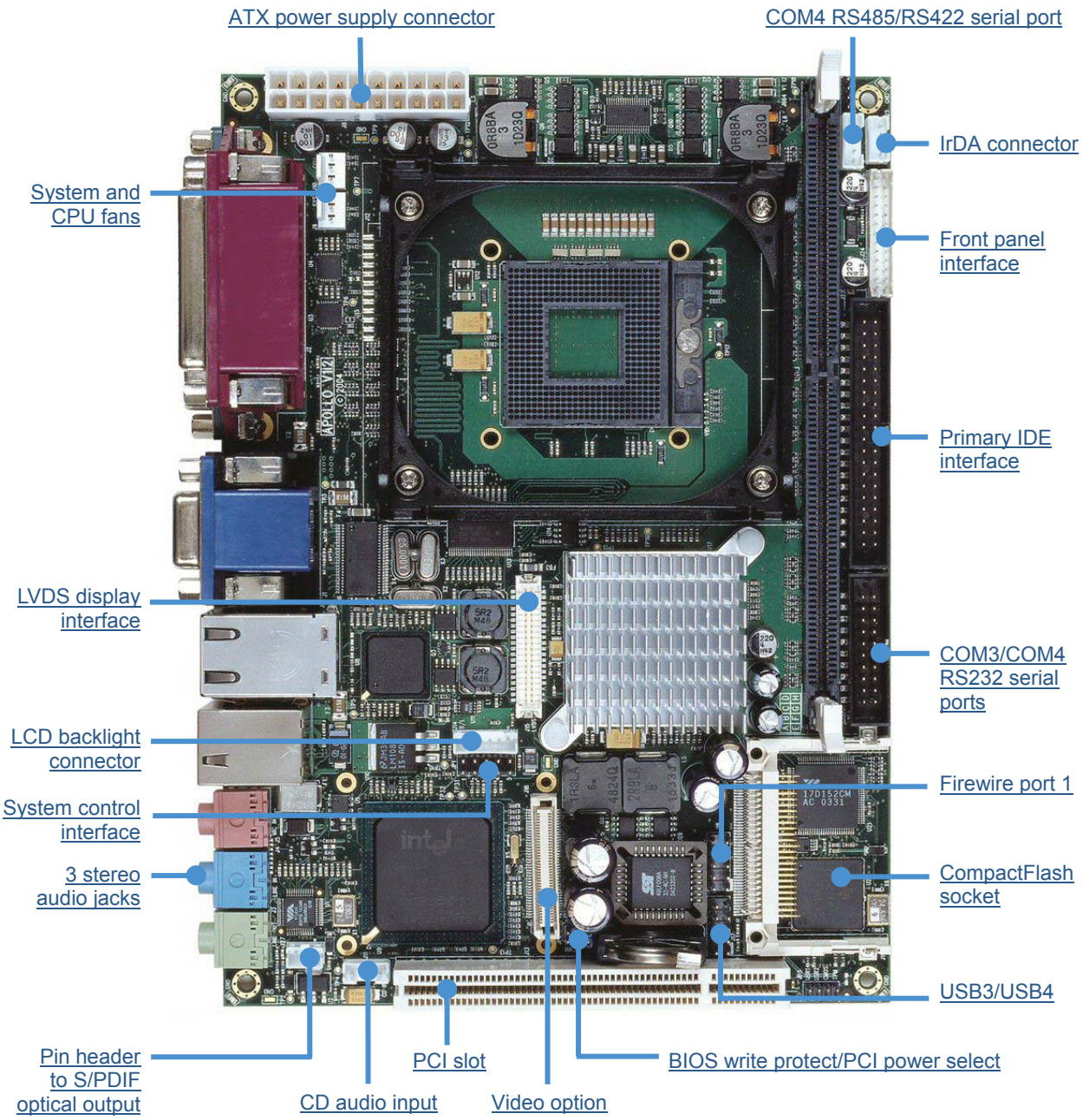
Typical applications for the APOLLO include:

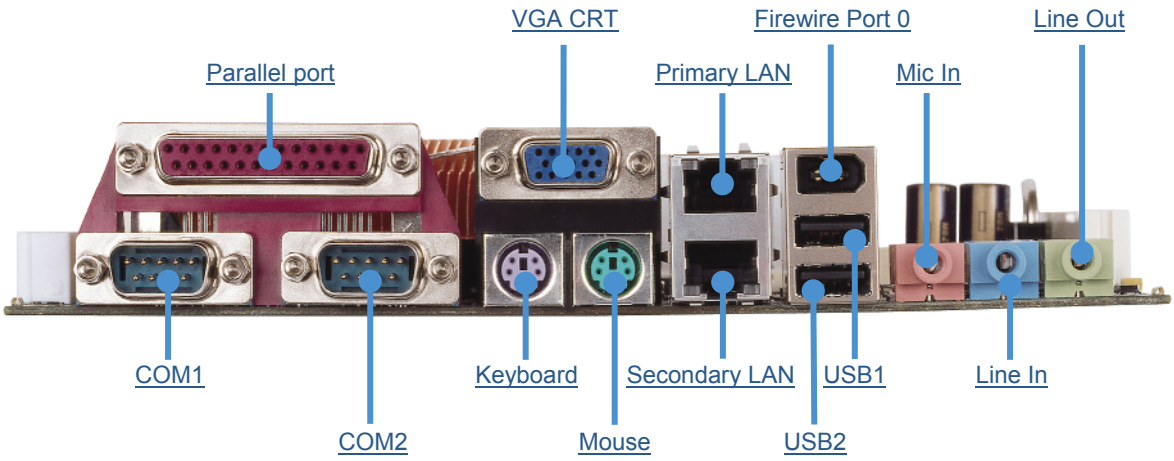
- Low power, high density server racks.
- 1U or 2U systems with passive cooling for fan-less operation.
- Systems requiring high levels of hardware/software security.
- Server/client systems using Trusted Computing.
- Compact kiosk systems.

The V1Ix board can be purchased in the following standard variants:

- Standard (two 10/100 Ethernet).
- Gigabit (one 10/100 Ethernet and one 10/100/1000 Ethernet).
- The V2Ix board is available as a single variant offering Gigabit Ethernet (1x 10/100 and one 10/100/1000 Ethernet, this also has a Trusted Platform module (TPM 1.2) fitted as standard.

APOLLO ‘at a glance’





Side view showing connectors

Features

Processor

- Intel Pentium M and Celeron M processor options.

Chipset

- North Bridge: Intel 82555GME.
- South Bridge: Intel 82801DB/ICH4.
- 400MHz processor side bus speed.

System memory

- Up to 1024MB PC2700 DDR DIMM.

BIOS

- PhoenixBIOS boot from HDD, FDD, CDROM, CompactFlash®, USB device or network boot.

Video

- Integrated Intel Extreme Graphics 2.
- VGA CRT interface - 2048 x 1536 at 75Hz.
- LVDS interface (single/dual channel) -1600 x 1200 at 60Hz.
- Dual graphics controller - allows for two independent video displays.
- Additional DVI and CRT add-on modules are also available.

Audio

- AC97 codec with support for six channel 5.1 speaker output.
- S/PDIF (Sony/Philips Digital Interface) compressed digital output to optical transmitter.

Network support

- Dual 10/100baseTx Ethernet ports or a build variant for 10/100 and 10/100/1000 Ethernet ports.

USB interface

- Six USB 2.0 channels: four on-board; two via an add-on module.

Serial ports

- Two RS232.
- One RS232/IrDA.
- One RS232/422/485.

Other ports, connectors and sockets

- Printer, mouse, keyboard and floppy drive ports. (Slimline floppy via flat flex connector.)
- Auxiliary connector for LCD character display, GPIO, LED drivers and SMBus.
- Two IEEE1394a-2000 Firewire ports (100/200/400Mbps).
- PCI Rev 2.2 expansion with support for three PCI bus master cards via a riser card.
- IDE ATA hard drive port (Ultra ATA100/66/33, PIO).
- CompactFlash® (CF+) version 2.0 Type II socket for memory and I/O cards.

Integrated security features

- Unique ID, tamper detection circuitry.
- Trusted platform module using Atmel AT97SC3203 (TPM 1.2) V2Ix APOLLO only.
- Provides hardware-based authentication of platform trust level, a secure store for private keys and an inbuilt encryption engine (compliant to TCG Spec. 1.2).

New features in the V2 APOLLO

- Trusted platform module TPM 1.2 using Atmel AT97SC3203.
- Enhanced watchdog support.
- Improved SuperIO functionality.
- RoHS compliant design.
- Standby and BIOS boot LEDs.
- Ethernet outputs are fixed as 1 x 10/100 and 1 x 10/100/1000 Ethernet.

Support products

The APOLLO is supported by the following optional products:

- **1U 19" wide APOLLO ICE (Industrial Compact Enclosure)**
  Provides easy-to-use system solutions for embedded SBC applications. It is manufactured from 0.9mm (20 SWG) finished mild steel. The enclosure conforms to the 19" 1EC6O297-1/2 DIN 41494 and MEP IEC 60917-2-1 standards and therefore meets the 19" 1U specification in height and width. Depth is approximately 13.8 inches (350mm).

  The APOLLO ICE contains:

  - 180W AC ATX PSU: Auto-ranging 100-240V AC at 47 - 63Hz.
  - DC input ATX PSU options available, please contact Eurotech sales.
  - Standard I/O connections from rear panel.
  - On/off switch, power and HDD activity LEDs.
  - Front panel connections for USB ports and IEEE1394 port.
  - Access to a front panel reset switch.
  - PCI riser card with two card expansion slots.
  - Floppy disk, hard disk drive and CD/DVD writeable drive.
  - Front panel LCD display with navigation/input switches and user LEDs.
  - Tamper detect switch for enclosure lid.

- **LCD display**
  An AU Optronics 15" XGA (1024x768) colour TFT LCD display interfaces directly with the LVDS signals provided by the APOLLO. The display has a 400:1 contrast ratio, 16ms response time and a dual CCFL backlight providing 350nits of screen brightness.

- **TSC1 (touchscreen controller)**
  The Eurotech TSC1 can be used to provide analogue resistive touchscreen support for the APOLLO. The TSC1 is designed to directly interface between four-, five- or eight-wire analogue touchscreens and a serial connection. A 1:1 ribbon cable can be used to connect directly to one of the RS232 ports on the APOLLO. A separate +5V connection is also required.

- **15" touchscreen**
  Glass-backed 15" touchscreens are available for use in conjunction with the 15" LCD display. Two touchscreens are available: a four-wire option and an eight-wire option. These interface directly with the Eurotech TSC1 touchscreen controller.

For more details about any of the above options, please go to www.eurotech.com or contact the Eurotech sales team (see page 144).

Development kits

Eurotech offers development kits for the APOLLO board. A choice of three different configurations is available:

- Windows XP Embedded contained on Flash disk module for the APOLLO V2Ix board and Windows XP Embedded contained on a CompactFlash® card for the APOLLO V1Ix board.
- Linux contained on USB flash disk.
- No operating system, no CompactFlash card.

All three configurations are supplied with a Pentium M 1.6GHz processor, 512MB PC2700 DDR SDRAM and are based on the Gigabit Ethernet APOLLO variant.

A range of options are available with all three development kits. Please contact the Eurotech sales team (see page 144) to discuss your requirements.

Handling your board safely

Anti-static handling

This board contains CMOS devices that could be damaged in the event of static electricity being discharged through them. At all times, please observe anti-static precautions when handling the board. This includes storing the board in appropriate anti-static packaging and wearing a wrist strap when handling the board.

Battery

The board contains a lithium non-rechargeable battery. Do not short circuit the battery or place on a metal surface where the battery terminals could be shorted. When disposing of the board or battery, take appropriate care. Do not incinerate, crush or otherwise damage the battery.

Packaging

Please ensure that, should a board need to be returned to Eurotech, it is adequately packed, preferably in the original packing material.

Electromagnetic compatibility (EMC)

The APOLLO is classified as a component with regard to the European Community EMC regulations and it is the user's responsibility to ensure that systems using the board are compliant with the appropriate EMC standards.

RoHS compliance

The European RoHS Directive (Restriction on the use of certain Hazardous Substances – Directive 2002/95/EC) limits the amount of 6 specific substances within the composition of the product. The APOLLO and associated accessory products are available as RoHS-6 compliant options and are identified by a -R6 suffix in the product order code.

A full *RoHS Compliance Materials Declaration Form* for the APOLLO is included as Appendix I – RoHS-6 Compliance - Materials Declaration Form, page 143. Further information regarding RoHS compliance is available on the Eurotech web site at www.eurotech-ltd.co.uk/RoHS_and_WEEE.

Conventions

The following symbols are used in this guide:

Symbol	Explanation
	Note - information that requires your attention.
	Caution – proceeding with a course of action may damage your equipment or result in loss of data.
	Jumper is fitted.
	Jumper is not fitted.
	Jumper fitted on pins 1-2.
	Jumper fitted on pins 2-3.

Getting started with your APOLLO

Once you have a working APOLLO system, you can start adding other peripherals to enable you to start development. In this section we guide you through setting up and using peripherals and some of the features of the APOLLO.

The APOLLO uses a PhoenixBIOS (Basic Input-Output System) to provide support for the board as standard. BIOS defaults have been selected to enable the board to operate with a minimum of devices connected. If you want to change these default settings, you use the PhoenixBIOS setup program. See PhoenixBIOS features and setup, page 51 for details.

The setup parameters are stored in the CMOS RAM and are retained when the power is switched off, providing the battery backup supply is connected. If no battery is installed or the CMOS settings are corrupted then the BIOS will restore them from an onboard CMOS EEPROM.

Identifying your APOLLO version

To comply with the EU RoHS regulations, the APOLLO has been updated to version 2.x. Overall, the changes to the APOLLO functionality are minimal. However some of the component changes require new software to be loaded.

You can identify the version of your APOLLO board in three ways:

- *Visually*. All APOLLO PCBs are marked on the top side with the APOLLO name and a board version and issue.
- *Using a software utility*. An APOLLO identification program is available from Eurotech support. This DOS-based application reads the values of the installed SuperIO and from this information determines and displays the APOLLO version.
- *From the BIOS*. To see the APOLLO version from the BIOS:

  1. Boot the APOLLO board
  2. As the BIOS Phoenix splash screen appears, press the **Esc** key, immediately followed by the **Pause/Break** key. The BIOS version is then displayed as follows:

     ```
     APOLLO V1Ix        X1.xx or V1.xx
     ```

     or

     ```
     APOLLO V2Ix        X2.xx or V2.xx
     ```

CPU configuration

The APOLLO board has been specifically designed to support a range of Intel Pentium M and Celeron M mobile processors. The appropriate voltage and speed selections are configured during the boot process. No user configuration is required.

Installing memory

The APOLLO has one DIMM socket for an unbuffered ECC or non-ECC double data rate (DDR) SDRAM 184-pin DIMM module. DIMM modules supported are:

- 128MB, 256MB, 512MB and 1024MB.
- PC1600 (200MHz), PC2100 (266MHz) and PC2700 (333MHz).

The APOLLO supports a single 184-pin DIMM module. If your board was supplied without memory, or if you wish to upgrade your memory, then you need to source an appropriate module. See Memory interface, page 92, for details.

No link settings are required to enable the board to support different memory sizes. The BIOS automatically detects the memory and configures the board appropriately. Always ensure that the power is switched off before attempting to insert a memory module. The module should be inserted in an ESD safe area, and you should be wearing an earth strap or touching a grounded surface to protect the device. The memory module is designed to ensure that it can only be plugged in with the correct orientation. If the module does not fit, check the key locations and ensure the memory is the correct type.

To install memory, insert the memory module vertically into the socket. The memory module and socket are keyed to ensure the correct orientation of the module in the socket. Once fully inserted into the socket, the module can be pressed down towards the board. The tabs on the socket automatically latch onto the module and secure it in place.

To remove the memory, gently pull the two tabs sideways. The module releases and can be removed easily.

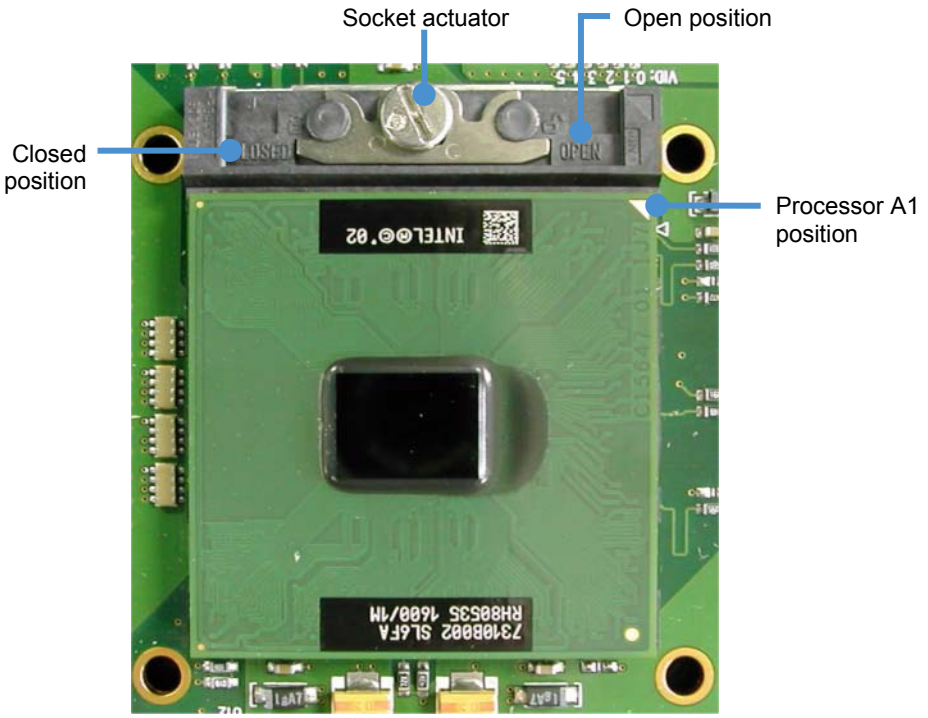
Once power is applied to the board, the BIOS automatically configures the memory. During the memory check, a message is displayed showing the amount of memory found.

Installing a processor

The standard and Gigabit variants of the APOLLO board have a zero insertion force PGA socket soldered to the board that accepts a range of Pentium M and Celeron M µFC-PGA processors. For a list of PGA processors, see page 91.

To install a processor into the socket, follow these steps:

1 Check that the socket actuator is in the OPEN position, as shown by an open padlock symbol:



2 Align the small triangle on the top side of the processor with the A1 pin position on the socket. A small triangle on the socket shows this position, as does the APOLLO board silkscreen.

The µFC-PGA processors are designed to only fit into the socket in one way.

You should not have to press down on the processor to get it to fit into the socket. If the processor does not drop completely into the socket, check the orientation. If orientation is correct, turn the actuator on the socket until the processor drops in completely.

3 Gently hold the processor down and secure it in the socket by using a screwdriver to turn the actuator to the Closed position. This is shown by a closed padlock symbol.

4 Mount a suitable cooling solution to contact the exposed processor die before the board is powered on. The BIOS automatically determines the processor installed and adjusts the settings accordingly. No BIOS modifications are required.

Connecting a floppy disk drive

The APOLLO supports one slimline floppy drive via a flat flex connector. A 26-way flat flex cable is used to provide a direct connection between the APOLLO board connector (see J27 – Slimline floppy drive interface on page 50) and the slimline floppy drive. Power for the floppy drive is provided over the cable.

The BIOS default configuration assumes that a 1.44MB floppy disk is connected. You can use the PhoenixBIOS setup to change this to other floppy drive formats. See page 54 for details.

Connecting a hard disk drive

The APOLLO provides a single primary IDE controller, enabling up to two IDE devices to be connected. For optimum performance, ATA66 drives and above should use an 80-way IDE ribbon cable with 40-way connectors. An 80-way cable has additional ground lines to improve the signal integrity at the higher ATA66 and ATA100 operating speeds.

If you add two drives to a single channel, one should be set up as a ‘master’ and the other as a ‘slave’. The BIOS automatically detects the hard disk drive(s) during the POST processes and configures the hardware correctly. The PhoenixBIOS allows either a master or slave device to be the boot device. See page 54 for further details.

For further details about the IDE interface, see page 103.

The standard APOLLO cable kit provides an 80-way IDE ribbon cable for use with ATA66 and ATA100 drives.

Connecting a CD-ROM (IDE type)

If a CD-ROM drive is required in the system, it may be connected in place of a secondary drive (as detailed above). The CD-ROM should be configured as a ‘slave’ device.

Drivers are required to support a CD-ROM drive under DOS. If a bootable CD is inserted in the drive, the BIOS can be configured to automatically boot from this CD.

Connecting a CompactFlash® card

The APOLLO has a single CF+ version 2.0 Type II CompactFlash® socket that supports both Type I and Type II CompactFlash cards. This provides support for magnetic disk drive data storage and I/O cards such as Ethernet, serial, fax/modem, barcode scanner, Bluetooth, 802.11b wireless LAN, wireless digital cell phone cards and so on.

The CompactFlash socket is connected to the CardBus/PCMCIA controller. If a CompactFlash card is plugged into the socket it acts as a normal hard disk drive and is detected by the BIOS during the POST process. If the card has an operating system loaded and is correctly configured to be bootable, it can be selected as a boot device from the BIOS boot menu.

The CompactFlash card can only be inserted into the socket one way. The correct orientation is for the top of the card (i.e. the normal printed side) to be furthest from the PCB.

For further details about the CompactFlash socket, see CompactFlash® CF+ socket, page 112.

Connecting a keyboard

A PS/2 keyboard can be connected to the PS/2 MiniDIN Connector. See page 36 for more information.

Connecting a mouse

A PS/2 mouse can be connected to the PS/2 MiniDIN Connector. See page 36 for more information.

Turning on your APOLLO

By default, the APOLLO BIOS is set to enter a standby state when power is applied. This therefore requires the operator to turn the unit ON via a remote switch connected to the board. The APOLLO power button connection should be connected to a momentary ON push button switch; this is described in System control interface on page 105.

To set the APOLLO board into a mode whereby it automatically starts when AC power is applied, change the *After Power Failure* setting in the *Power* screen within the BIOS Setup. See Power menu, page 84, for more information.

Using the serial interfaces (RS232/RS485/IrDA)

The four serial port interfaces on the APOLLO are fully PC compatible:

- COM1 and COM2 are decoded at standard PC address locations. PC applications can use these ports without any special configuration.
- COM3 and COM4 are interfaced via a PCI based dual UART. The Windows and Linux drivers provided on the APOLLO CD allow for the configuration of these devices as standard serial ports.

The BIOS setup screens are used to configure the operation of each of the serial ports.

Connections to COM1 and COM2 are via standard DB9 connectors. COM3 and COM4 are interfaced via a 10-way boxed header. The pin assignment of these headers is arranged to enable a 9-way IDC D-Type plug to be connected directly to pins 1-9 on the cable. The D-type connector is compatible with the standard 9-way connector on a desktop machine. A suitable cable is provided in the development kit.

See Serial ports, page 109 for further details about the serial port interface, and page 38 for pin details.

Connecting a printer

An enhanced printer port is incorporated into the APOLLO. This port can be used to support a Centronics-compatible printer or ECP/EPP bi-directional device. The port signals are routed to directly to a female DB25 connector. This socket is compatible with a standard printer port connector on a desktop machine.

See Parallel port, on page 110, for further details about the parallel port interface, and page 37 for pin details.

Using the audio features

The APOLLO provides an AC97 audio codec that supports standard line in, line out, mic in functionality, or alternatively can be configured in software to support the 5.1 speaker output format. The audio outputs are made available through board-mounted 3.5mm stereo jacks. Interfaces are also available to support an optical S/PDIF (Sony Philips Digital Interface) connector and CD audio input.

See pages 32 and 38 for further details.

Using the flat panel interface

The APOLLO provides a dual channel LVDS LCD display header that can be used to directly interface to LVDS LCD displays up to a maximum resolution of 1600x1200. The display type is selected from the PhoenixBIOS Intel IGD video setup menu. See Video (Intel IGD) control settings, page 76, for further details.

Using the USB ports

The standard USB connector is a 4-way socket, which provides power and data signals to the USB peripheral. It is a USB Type A connector.

USB ports 1 and 2 are standard USB Type A connectors (J4B and J4C). USB Ports 3 and 4 are provided on a 10-way header (J18) designed to be compatible with PC expansion brackets that support two USB sockets. USB ports 5 and 6 are supported via a board interfaced through the video option connector (J16). The 10-way header provided on the video option board or USB5/6 breakout (see page 97) has a pinout corresponding to J18.

See pages 34, 42 and 45 for further details.

Using the Ethernet interface

The APOLLO V1Ix board provides two 10/100 Ethernet ports as standard. A factory build option on the V1Ix board is also available that provides one 10/100 Ethernet port and one 10/100/1000 Ethernet port, thus providing Gigabit Ethernet capability.

The APOLLO V2Ix board provides one 10/100 Ethernet port and one 10/100/1000 Ethernet port, there is no variant supporting two 10/100 Ethernet ports.

Both Ethernet interfaces are capable of supporting network boot features. Two rear panel RJ-45 pin connectors provide the Ethernet interface. To support Gigabit Ethernet capabilities, a cable rated to CAT5e or above with four signals pairs should be used.

Further information on the Ethernet interfaces is available on page 101.

Using the 1394/Firewire ports

The APOLLO provides two IEEE1394a ports capable of supporting connection speeds of 100, 200 and 400Mbps; each port also provides a fused and diode protected 12V bus power rail.

The IEEE1394 Port 0 (J4A) is a 6-pin 1394 connector. The IEEE1394 Port 1 supports the connection of a 6-pin 1394 connector and is interfaced via a 10-way pin header. See page 34 for further information.

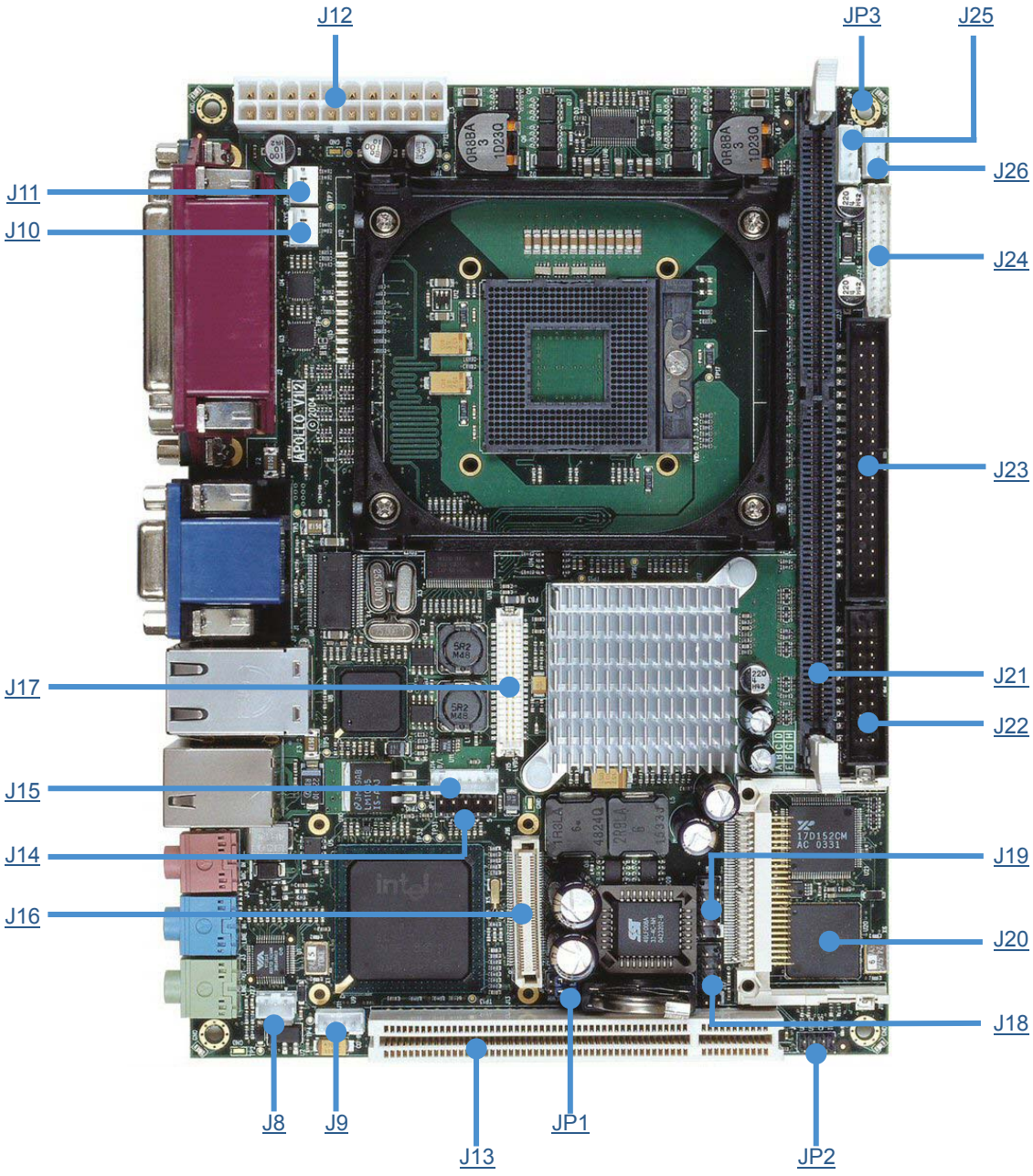
LED indicators

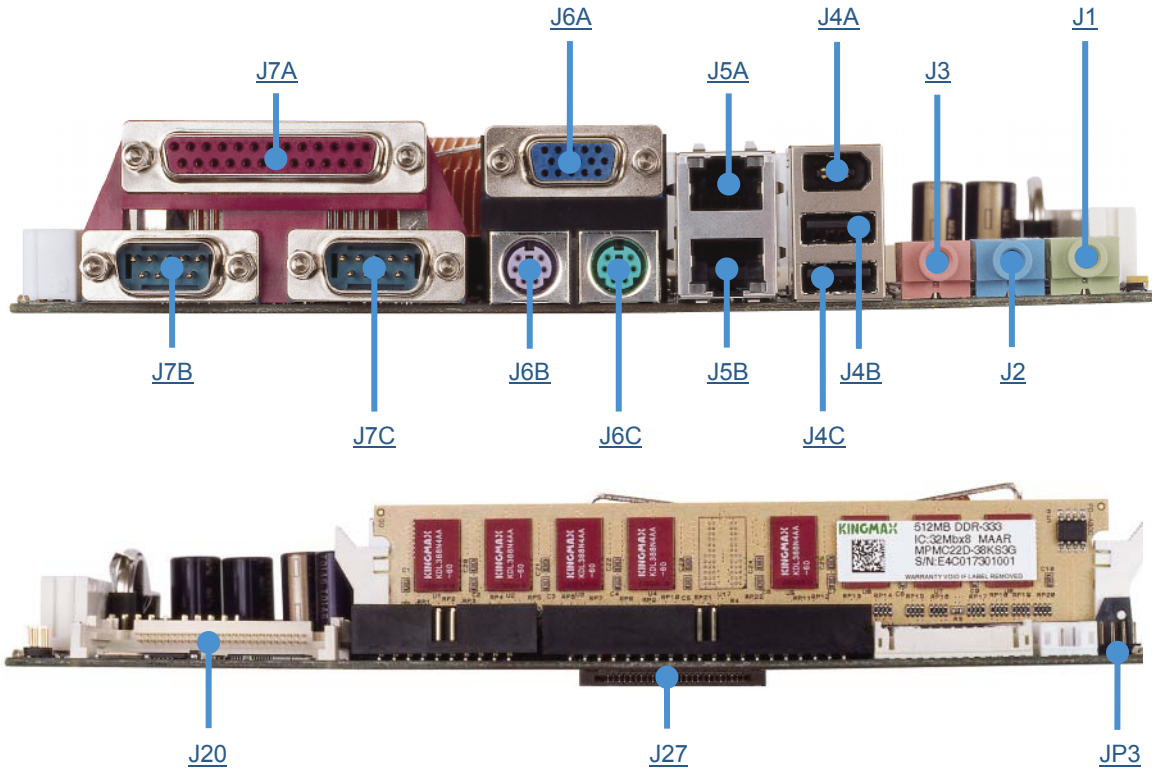
Two new LEDs have been added to the APOLLO V2Ix board, these are used for a visual indication of the board status:

LED	Colour and position	Purpose
STANDBY POWER LED	Orange, situated next to the PCI connector.	Provides a visual indication to the user when 5V standby power is present on the board to prevent PCI cards being inserted while power is applied.
BOOT LED	Red, situated next to IEEE1394 connector (J19).	Shows the boot status of the board. Flashing signifies that the BIOS is booting or the BIOS setup screen is active. The BOOT LED is cleared at the time the BIOS hands over control to the operating system. This can be used to help determine BIOS/OS related boot issues.

Jumpers and connectors

The following diagrams show the jumpers and connectors on the APOLLO. Click on any jumper or connector name for information.




J6A
J4A
J1
J7A
J5A
J3
J7B
J6B
J5B
J4B
J2
J7C
J6C
J4C
KINGMAX
512MB DDR-333
IC:32Mbx8 MAAR
MPMC22D-38KS3G
S/N:E4C017301001
J20
J27
JP3

Jumpers

There are three jumper blocks on the APOLLO with a total of eight user-selectable jumper positions. These are summarized in the following table:

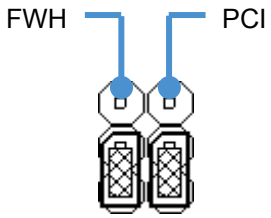
Jumper	Description
JP1	Performs two functions: • PCI Grant/PCI Auxiliary power selection. • BIOS write protection.
JP2	Includes four positions, as follows: • Two user-defined positions. • CMOS memory reset. • Tamper detect (TPM).
JP3	RS485/RS422 termination resistor enable/disable.

Further details are provided about each of these in the following sections.

Diagrams are used to illustrate jumper settings. For an explanation of the symbols used, see Conventions on page 13.

JP1 – PCI power selection and BIOS write protection

This jumper has two functions. Use it to select the function of PCI slot pin A14 and also to enable or disable BIOS write protection. The jumper is illustrated in the following diagram:



The jumper positions are explained in more detail on the next page.

JP1 PCI – PCI Grant/PCI auxiliary power selection

Used to select the functionality of PCI slot pin A14. There are two options available: 3.3V PCI auxiliary voltage routed to the PCI slot, or GNT4 signal. GNT4 is made available to support a third PCI slot (via a riser card); the default jumper setting should be used with a two-slot PCI riser.

JP1 PCI	Description
	3.3V PCI Auxiliary power to PCI slot. Default setting: 
	GNT4 to PCI slot.

JP1 Firmware hub – BIOS write protection

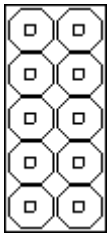
To enable BIOS write protection the jumper must be placed in position 2-3.

BIOS ECSD data cannot be updated when the write protect is in place. Any devices added to the system with write protection enabled will not be reported by the BIOS.

JP1 FWH	Description
	BIOS firmware hub writeable. Default setting: 
	BIOS firmware hub write protected.

JP2 on APOLLO V1Ix – User-configurable, CMOS reset and tamper detect

This consists of four individual jumper positions. Two of these are user-configurable (USR1 and USR2). The third (CMOS) is used to clear the battery backed CMOS memory, whilst the fourth (TPM) provides a tamper detect option. This is illustrated in the following diagram:



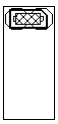
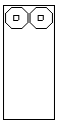
JP2 – APOLLO V1Ix

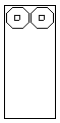
The individual positions are explained further in the following sections.

APOLLO V1Ix: USR1 – User-defined jumper 1/CMOS Reload

This jumper is user-configurable and can be used by an application program to signify a configuration setting. The status of this jumper is read through the firmware hub general purpose inputs, located at memory location FFBC0100H bit 1. This is an 8-bit read and a read-only memory location; writing to this bit has no effect.

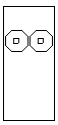
The USR1 jumper has an alternate function to reload the default CMOS values from the system BIOS; care should be taken to ensure that this jumper is not fitted at power on.

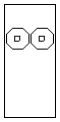
USR1	Description
	Bit is low ‘0’.
	Bit is high ‘1’.

Default setting: 

APOLLO V1Ix: USR2 – User-defined jumper two

This jumper is user-configurable and can be used by an application program to signify a configuration setting. The status of this jumper is read through the firmware hub general purpose inputs, located at memory location FFBC0100H bit 2. This is an 8-bit read and a read-only memory location; writing to this bit has no effect.

USR2	Description
	Bit is low ‘0’.
	Bit is high ‘1’.

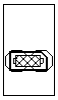
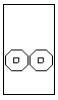
Default setting: 

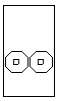
APOLLO V1Ix: CMOS reset jumper

Used to clear the contents of the battery backed CMOS memory.

Please note:

- Because CMOS values are backed up in an onboard EEPROM, clearing the CMOS results in the CMOS values being reloaded from the EEPROM.
- To restore the CMOS to factory default settings the USR1 jumper should be used.
- Changes to this jumper setting must only be made with board power completely removed. To do this you must remove the power cable.

CMOS	Description
	Reset CMOS memory.
	CMOS unchanged.

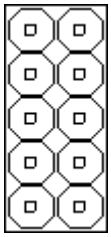
Default setting: 

APOLLO V1Ix: TPM functionality jumper

This position is used with the APOLLO TPM to provide future functionality.

JP2 on APOLLO V2Ix – User-configurable, CMOS reset and tamper detect

This consists of five individual jumper positions. Two of these are user-configurable (USR1 and USR2). The third (CMOS) is used to clear the battery backed CMOS memory, whilst the fourth (TPM) provides a tamper detect option. This is illustrated in the following diagram:

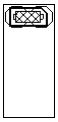
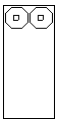


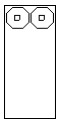
JP2 – APOLLO V2Ix

The individual positions are explained further in the following sections.

APOLLO V2Ix: USR1 – User-defined jumper one

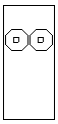
This jumper is user-configurable and can be used by an application program to determine a configuration setting. The status of this jumper is read through the firmware hub general purpose inputs, located at memory location FFBC0100H bit 1. This is an 8-bit read and a read-only memory location; writing to this bit has no effect.

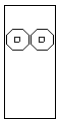
USR1	Description
	Bit is low ‘0’.
	Bit is high ‘1’.

Default setting: 

APOLLO V2Ix:- USR2 – User-defined jumper two

This jumper is user-configurable and can be used by an application program to signify a configuration setting. The status of this jumper is read through the firmware hub general purpose inputs, located at memory location FFBC0100H bit 2. This is an 8-bit read and a read-only memory location; writing to this bit has no effect.

USR2	Description
	Bit is low ‘0’.
	Bit is high ‘1’.

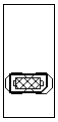
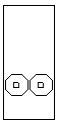
Default setting: 

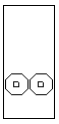
APOLLO V2Ix: -CMOS reset jumper

Used to clear the contents of the battery backed CMOS memory.

Please note:

- Because CMOS values are backed up in an onboard EEPROM, clearing the CMOS results in the CMOS values being reloaded from the EEPROM.
- To restore the CMOS to factory default settings the Reset EE jumper position should be used.
- Changes to this jumper setting must only be made with board power completely removed. To do this you must remove the power cable.

CMOS	Description
	Reset CMOS memory.
	CMOS unchanged.

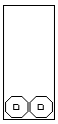
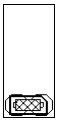
Default setting: 

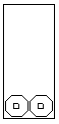
APOLLO V2Ix: TPM jumper

This position is used with the APOLLO TPM to provide future functionality.

APOLLO V2Ix: Reset EE jumper

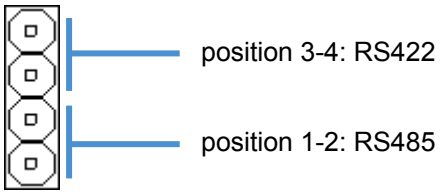
This position is used to reload the default CMOS values from the system BIOS into the backup EEPROM and onboard CMOS. The CMOS and EEPROM updates are only performed during a power cycle so setting this jumper during normal board operation will have no effect.

CMOS	Description
	Reload CMOS EEPROM.
	CMOS EEPROM unchanged.

Default setting: 

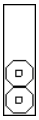
JP3 – RS485/422 configuration

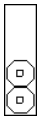
This jumper is used to configure the RS485/422 serial interface. It can be used to enable/disable the RS485/422 termination resistors. See RS485/422 interfaces, page 107, for more details. The JP3 jumper is illustrated in the following diagram:



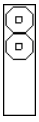
Jumper settings are detailed in the following sections.

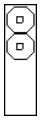
RS485 termination resistor

RS485	Description
	RS485 termination resistor connected.
	RS485 termination resistor disconnected.

Default setting: 

RS422 termination resistor

RS422	Description
	RS422 termination resistor connected.
	RS422 termination resistor disconnected.

Default setting: 

Connectors

There are 34 connectors on the APOLLO that let you connect external devices such as keyboards, floppy disk drives, hard disk drives, printers etc.

Connector	Function	See ...
J1	Audio Line Out.	Page 32.
J2	Audio Line In.	Page 32.
J3	Audio Mic In.	Page 32.
J4A	IEEE1394 port 0.	Page 34.
J4B, J4C	USB ports 1 to 2.	Page 34.
J5A	Primary LAN.	Page 35.
J5B	Secondary LAN.	Page 35.
J6A	VGA connector.	Page 36.
J6B	Keyboard.	Page 36.
J6C	Mouse.	Page 36.
J7A	Parallel port (LPT1).	Page 37.
J7B, J7C	Serial ports 1 to 2.	Page 38.
J8	S/PDIF output.	Page 38.
J9	CD audio input.	Page 38.
J10	System fan.	Page 39.
J11	CPU fan.	Page 39.
J12	ATX power connector.	Page 39.
J13	PCI slot.	Page 40.
J14	System control interface.	Page 41.
J15	LCD backlight interface.	Page 42.
J16	Video option and USB ports 5/6 connector.	Page 42.
J17	LVDS display interface.	Page 44.

continued…

Connector	Function	See ...
J18	USB ports 3 to 4.	Page 45.
J19	IEEE1394 port 1.	Page 45.
J20	CompactFlash® socket.	Page 46.
J21	184-pin DDR SDRAM DIMM Socket.	N/A
J22A, J22B	Serial ports 3 to 4.	Page 47.
J23	Primary IDE.	Page 48.
J24	Front panel interface.	Page 49.
J25	RS485/RS422 port	Page 49.
J26	IrDA connector.	Page 50.
J27	Slimline floppy drive interface.	Page 50.

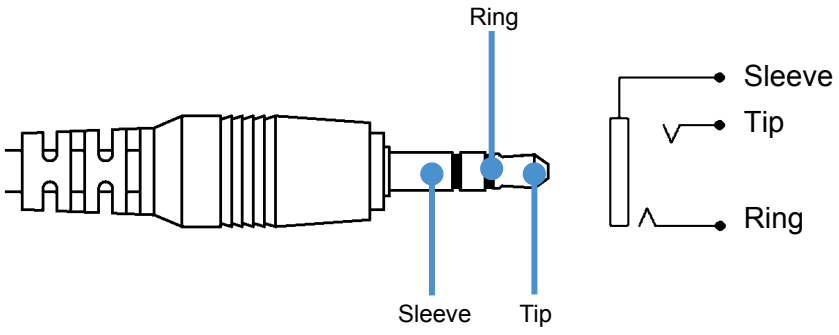
J1, J2, J3 – Audio connectors

3.5mm stereo audio jacks are used for audio connection. The audio codec can operate in either of the following modes:

- 2.0 mode, which allows for microphone in, line in and line out operation.
- 5.1 mode, which provides six-channel surround sound output. The microphone input and line in are not available during six channel mode.

Selection of 2.0 or 5.1 mode is made using software.

The audio connectors are illustrated in the following diagram:



The pin settings for each connector are described in the following tables:

J1 - 3.5mm audio jack

PC99 Colour: lime

Pin	Connector: 2.0 mode	Connector: 5.1 mode
Tip	Line out left	Surround out left
Ring	Line out right	Surround out right
Sleeve	Ground	Ground

J2 - 3.5mm audio jack

PC99 Colour: light blue

Pin	Connector: 2.0 mode	Connector: 5.1 mode
Tip	Line in left	Rear surround left
Ring	Line in right	Rear surround right
Sleeve	Ground	Ground

J3 - 3.5mm audio jack

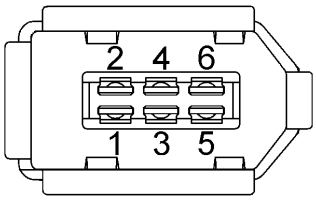
PC99 Colour: pink

Pin	Connector: 2.0 mode	Connector: 5.1 mode
Tip	Microphone In	Surround centre
Ring	No connect	Low frequency effects
Sleeve	Ground	Ground

J4A – IEEE1394 (Firewire) connector port 0

6-pin IEEE1394 connector.

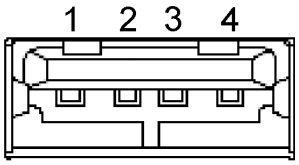
Pin	Signal name
1	+12V (fused)
2	Ground
3	TPB0-
4	TPB0+
5	TPA0-
6	TPA0+



J4B and J4C – USB ports 1 and 2

USB type A connector.

Pin	Signal name
1	VBUS
2	Data-
3	Data+
4	Ground

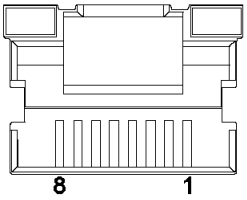


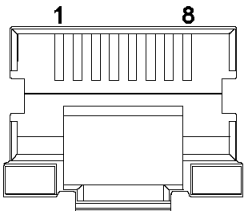
J5A – Primary LAN

APOLLO V1Ix: RJ-45 10/100Mb/s or optional 10/100/1000Mb/s.

APOLLO V2Ix: RJ-45 10/100/1000Mb/s.

Pin	Signal name (10/100)	Signal name (10/100/1000)
1	TX+	MD0+
2	TX-	MD0-
3	RX+	MD1+
4	No Connect	MD2+
5	No Connect	MD2-
6	RX-	MD1-
7	No Connect	MD3+
8	No Connect	MD3-



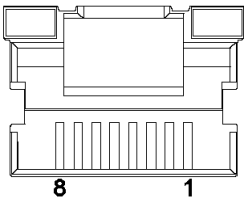


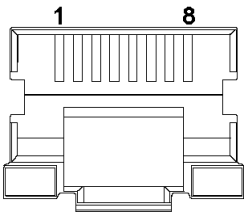
For a Gigabit Ethernet (10/100/1000) connection the network cable should be a CAT5 or above and include all four pairs.

J5B – Secondary LAN

RJ-45 10/100Mb/s.

Pin	Signal name
1	TX+
2	TX-
3	RX+
4	No Connect
5	No Connect
6	RX-
7	No Connect
8	No Connect



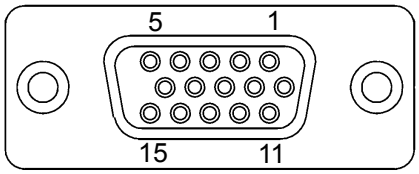


J6A – VGA CRT connector

DB15 Female

PC99 Colour: Blue

Pin	Signal name	Pin	Signal name
1	Red	2	Green
3	Blue	4	No Connect
5	Ground	6	Ground
7	Ground	8	Ground
9	+5V (Fused)	10	Ground
11	No Connect	12	DDCSDA
13	HSYNC	14	VSYNC
15	DDCSCL		

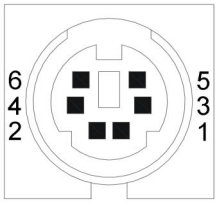


J6B – PS/2 keyboard

Connector: 6-pin Mini-DIN

PC99 Colour: Purple

Pin	Signal name
1	KB DATA
2	No Connect
3	Ground
4	+5V
5	KB CLOCK
6	No Connect

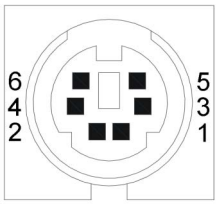


J6C – PS/2 mouse

Connector: 6-pin Mini-DIN.

PC99 Colour: Green

Pin	Signal name
1	MS DATA
2	No Connect
3	Ground
4	+5V
5	MS CLOCK
6	No Connect

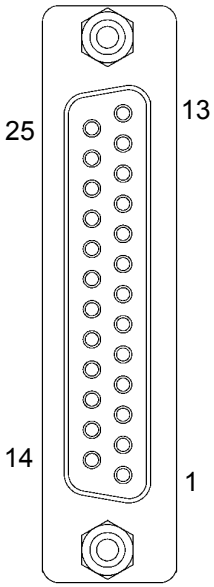


J7A – Parallel port (LPT1)

DB25 female

PC99 Colour: Maroon

DB25 D-type socket	Signal name
1	STROBE
2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7
10	ACKNOWLEDGE
11	BUSY
12	PAPER EMPTY
13	SELECT
14	AUTOFEED
15	ERROR
16	INIT
17	SELECT IN
18	Ground
19	Ground
20	Ground
21	Ground
22	Ground
23	Ground
24	Ground
25	Ground

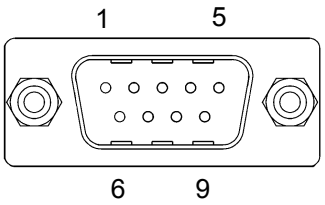


J7B and J7C – COM1 and COM2 RS232 serial ports

DB9 male

PC99 Colour: Aqua

Pin	Signal name	Pin	Signal name
1	Data Carrier Detect (DCD)	2	Receive Data (RX)
3	Transmit Data (TX)	4	Data Terminal Ready (DTR)
5	Ground	6	Data Set ready (DSR)
7	Request To Send (RTS)	8	Clear To Send (CTS)
9	Ring Indicator (RI)		



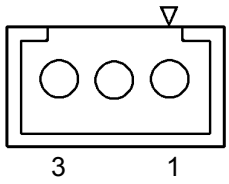
J8 – S/PDIF digital output

3-way 2mm pitch shrouded header.

Mating connector: JST PHR-3

Mating connector crimps: JST SPH-004T-P0.5S

Pin	Signal name
1	+5V
2	S/PDIF output to optical transmitter
3	GND



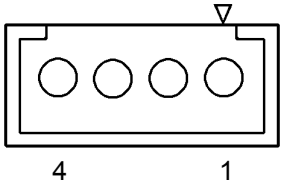
J9 – CD audio input

4-way 2mm pitch shrouded header.

Mating connector: JST PHR-4

Mating connector crimps: JST SPH-004T-P0.5S

Pin	Signal name
1	Left channel
2	Ground
3	Right channel
4	Ground

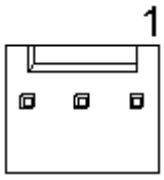


J10, J11 – system fan, CPU fan

Both are 3-way 2.54mm (0.1") friction lock pin headers. The APOLLO supports PWM fan control and fan tachometer feedback.

Connector: MOLEX 22-04-1031.

Pin	Signal name
1	Ground - PWM
2	+12V
3	Tachometer



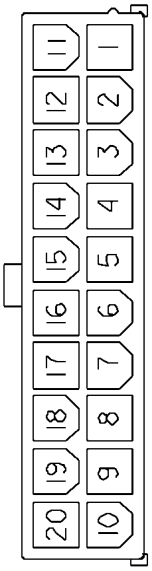
J12 – ATX power supply

Molex 87427-2043, 20-way, 4.20mm (0.165") x 4.20mm (0.165") dual row header.

Mating connector: Molex 39-01-2200, 20-way crimp housing.

Mating connector crimps (x20): Molex.

Pin	Signal name	Pin	Signal name
1	+3.3V	11	+3.3V
2	+3.3V	12	-12V
3	Ground	13	Ground
4	+5V	14	/PS_ON
5	Ground	15	Ground
6	+5V	16	Ground
7	Ground	17	Ground
8	PWR_OK	18	-5V (NC)
9	+5VSB	19	+5V
10	+12V	20	+5V



J13 – PCI connector

32-bit card edge connector. Three grant/request lines routed.

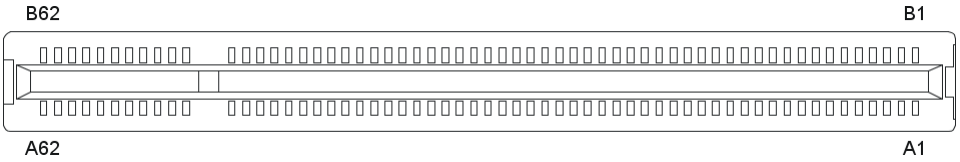
Connector: 120-way PCI card edge connector (5V 32-bit 33MHz PCI socket).

Pin	Side B	Side A	Pin	Side B	Side A
1	-12V	/TRST	32	AD17	AD16
2	TCK (GND)	+12V	33	/CBE2	+3.3V
3	Ground	TMS (+5V)	34	Ground	/FRAME
4	No Connect	TDI (+5V)	35	/IRDY	Ground
5	+5V	+5V	36	+3.3V	/TRDY
6	+5V	/INTE	37	/DEVSEL	Ground
7	/INTF	/INTG	38	Ground	/STOP
8	/INTH	+5V	39	/LOCK	+3.3V
9	No Connect	/REQ4	40	/PERR	SMB CLK
10	/ REQ3	+5V(I/O)	41	+3.3V	SMB DATA
11	No Connect	/GNT3	42	/SERR	Ground
12	Ground	Ground	43	+3.3V	PAR
13	Ground	Ground	44	/CBE1	AD15
14	No Connect	VAUX (/GNT4)	45	AD14	+3.3V
15	Ground	/RST	46	Ground	AD13
16	CLK	+5V(I/O)	47	AD12	AD11
17	Ground	/GNT1	48	AD10	Ground
18	/REQ1	Ground	49	Ground	AD09
19	+5V(I/O)	/PME	50	Key	Key
20	AD31	AD30	51	Key	Key
21	AD29	+3.3V	52	AD08	/CBE0
22	Ground	AD28	53	AD07	+3.3V
23	AD27	AD26	54	+3.3V	AD06
24	AD25	Ground	55	AD05	AD04
25	+3.3V	AD24	56	AD03	Ground
26	/CBE3	IDSEL (AD27)	57	Ground	AD02

continued…

Pin	Side B	Side A
27	AD23	+3.3V
28	Ground	AD22
29	AD21	AD20
30	AD19	Ground
31	+3.3V	AD18

Pin	Side B	Side A
58	AD01	AD00
59	+5V(I/O)	+5V(I/O)
60	/ACK64	/REQ64
61	+5V	+5V
62	+5V	+5V



Slot	IDSEL	GNT/RQT
0	AD27	1
1	AD29	3
2	AD31	4 (JP1 jumper selected)

J14 – System control interface

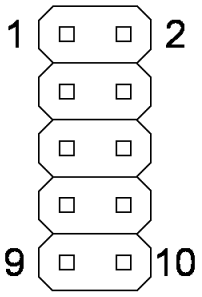
10-way, 2.54mm (0.1") x 2.54mm (0.1") dual row header.

Mating connector: Harwin M20-1070500

Mating connector crimps: Harwin M20-1180022

Pin	Signal name
1	Tamper
3	Power Button
5	System Reset
7	+5V
9	PC speaker

Pin	Signal name
2	Ground
4	Ground
6	Ground
8	HDD LED
10	Ground



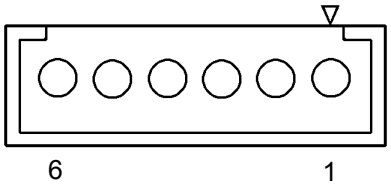
J15 – Backlight connector

6-way 2mm pitch shrouded header.

Mating connector: JST PHR-6

Mating connector crimps: JST SPH-004T-P0.5S

Pin	Signal name
1	+12V
2	Ground
3	+5V
4	Backlight control
5	Backlight En
6	Ground

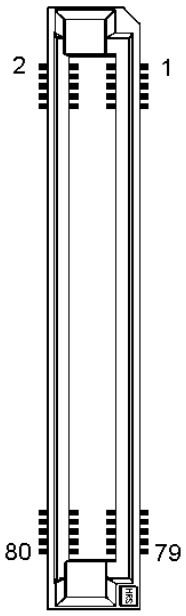


J16 – Video option and USB ports 5/6 connector

Hirose FX8C-80S-SV5.

Pin	Signal name	Pin	Signal name
1	+3.3V PCIVAUX	2	Ground
3	+3.3V	4	DVOBD11
5	+3.3V	6	DVOBD10
7	+3.3V	8	DVOBD9
9	+5V	10	DVOBD8
11	USB POWER	12	DVOBD7
13	USB POWER	14	DVOBD6
15	USB POWER	16	DVOBD5
17	Ground	18	DVOBD4
19	USB4 D+	20	DVOBD3
21	USB4 D-	22	DVOBD2
23	Ground	24	DVOBD1
25	USB5 D+	26	DVOBD0
27	USB5 D-	28	Ground

continued…



Pin	Signal name	Pin	Signal name
29	Ground	30	DVOBCLK#
31	USB overcurrent	32	DVOBCLK
33	DVO_REF	34	DVOBHSYNC
35	/RESET	36	DVOBVSYNC
37	Ground	38	DVOBBLANK#
39	ADDID7	40	DVOBFLDSTL
41	ADDID6	42	Ground
43	ADDID5	44	DVOCD11
45	ADDID4	46	DVOCD10
47	ADDID3	48	DVOCD9
49	ADDID2	50	DVOCD8
51	ADDID1	52	DVOCD7
53	ADDID0	54	DVOCD6
55	DVODETECT	56	DVOCD5
57	DVOCFLDSTL	58	DVOCD4
59	DVOBCINTR#	60	DVOCD3
61	DVOBCCLKINT	62	DVOCD2
63	Ground	64	DVOCD1
65	+1.5V	66	DVOCD0
67	+1.5V	68	Ground
69	+1.5V	70	DVOCCLK#
71	+1.5V	72	DVOCCLK
73	MI2CDATA	74	DVOCHSYNC
75	MI2CCLK	76	DVOCVSYNC
77	MDVIDATA	78	DVOCBLANK#
79	MDVICLK	80	Ground

J17 – LVDS display interface (Dual channel)

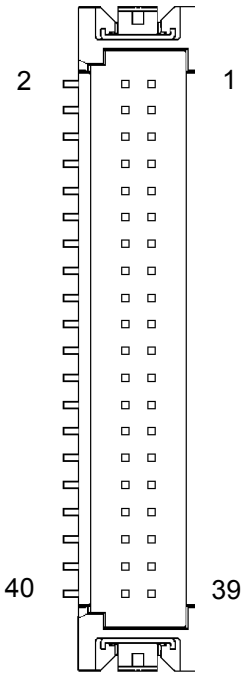
40-way 2mm Hirose DF13-40DP-1.25V.

Mating connector: Hirose DF13-40DS-1.25C

Crimps: Hirose: DF13-2630SCFA

For optimum performance of the LVDS interface a shielded twisted pair cable should be used.

Pin	Signal name	Pin	Signal name
1	+3.3V	2	+3.3V
3	+3.3V	4	+3.3V
5	Ground	6	Ground
7	IYA0-	8	IYA1-
9	IYA0+	10	IYA1+
11	Ground	12	Ground
13	IYA2-	14	IYA3-
15	IYA2+	16	IYA3+
17	Ground	18	Ground
19	ICLKA-	20	IYB0-
21	ICLKA+	22	IYB0+
23	Ground	24	Ground
25	IYB1-	26	IYB2-
27	IYB1+	28	IYB2+
29	Ground	30	Ground
31	IYB3-	32	ICLKB-
33	IYB3+	34	ICLKB+
35	Ground	36	Ground
37	Ground	38	Ground
39	DDC CLK	40	DDC DATA



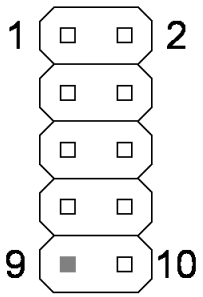
J18 – USB ports 3 and 4

10-way, 2.54mm (0.1") x 2.54mm (0.1") dual row header.

Mating connector: Harwin M20-1070500

Mating connector crimps: Harwin M20-1180022

Pin	Signal name	Pin	Signal name
1	VBUS (port 3)	2	VBUS (port 4)
3	D- (port 3)	4	D- (port 4)
5	D+ (port 3)	6	D+ (port 4)
7	Ground	8	Ground
9	Key (no pin)	10	Ground



For error free data transmission, cable certified for USB 2.0 operation should be used.

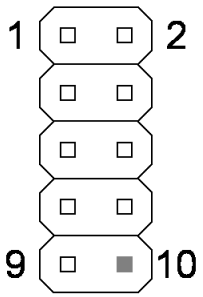
J19 – IEEE1394 connector port 1

10-way, 2.54mm (0.1") x 2.54mm (0.1") dual row header.

Mating connector: Harwin M20-1070500.

Mating connector crimps: Harwin M20-1180022.

Pin	Signal name	Pin	Signal name
1	TPA1+	2	TPA1-
3	Ground	4	Ground
5	TPB1+	6	TPB1-
7	+12V (fused)	8	+12V (fused)
9	Shield ground	10	Key (no pin)



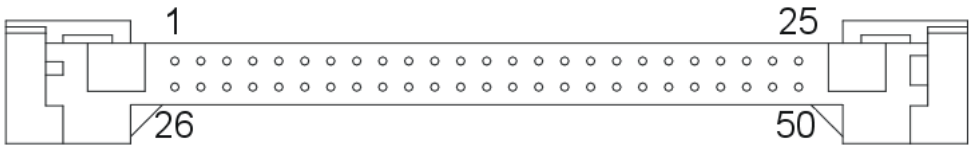
For error free data transmission, cable certified for IEEE1394 operation should be used.

J20 – CompactFlash® socket

Compact Flash CF+ type I/II socket.

Connector: 50 pin right angle CompactFlash®.

Pin	Signal name	Pin	Signal name
1	Ground	2	D03
3	D04	4	D05
5	D06	6	D07
7	/CE1	8	A10
9	/OE	10	A09
11	A08	12	A07
13	CF VCC	14	A06
15	A05	16	A04
17	A03	18	A02
19	A01	20	A00
21	D00	22	D01
23	D02	24	/IOCS16
25	/CD2	26	/CD1
27	D11	28	D12
29	D13	30	D14
31	D15	32	/CE2
33	/VS1	34	/IORD
35	/IOWR	36	/WE
37	/INTRQ	38	CF VCC
39	A25	40	/VS2
41	RESET	42	/WAIT
43	/INPACK	44	/REG
45	/BVD2	46	/BVD1
47	D08	48	D09
49	D10	50	Ground

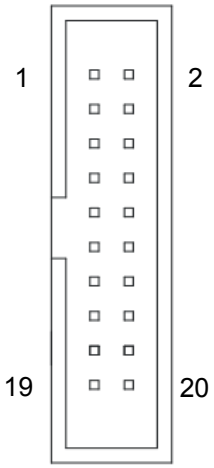


J22A and J22B – COM3 and 4 RS232 serial ports

20 way, 2.54mm (0.1") x 2.54mm (0.1") boxed header.

Mating connector: FCI 71600-020.

Pin (20-way header)	Signal name	Pin (9-way D-type plug)
1	Data Carrier Detect (DCD) COM3	1
2	Data Set Ready (DSR) COM3	6
3	Receive Data (RX) COM3	2
4	Request To Send (RTS) COM3	7
5	Transmit Data (TX) COM3	3
6	Clear To Send (CTS) COM3	8
7	Data Terminal Ready (DTR) COM3	4
8	Ring Indicator (RI) COM3	9
9	Ground COM3	5
10	No Connect	-
11	Data Carrier Detect (DCD) COM4	1
12	Data Set Ready (DSR) COM4	6
13	Receive Data (RX) COM4	2
14	Request To Send (RTS) COM4	7
15	Transmit Data (TX) COM4	3
16	Clear To Send (CTS) COM4	8
17	Data Terminal Ready (DTR) COM4	4
18	Ring Indicator (RI) COM4	9
19	Ground COM4	5
20	No Connect	-

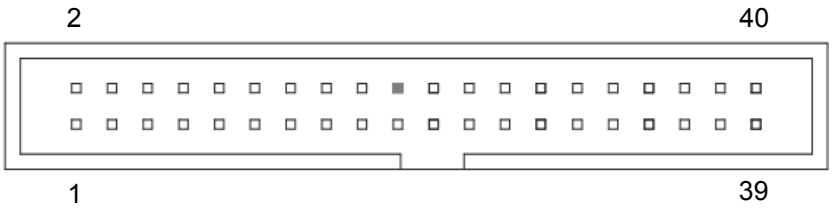


J23 – Primary IDE interface

40-way, 2.54mm (0.1") x 2.54mm (0.1") boxed header.

Mating connector: FCI 71600-040.

Pin	Signal name	Pin	Signal name
1	/RESET	2	Ground
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	Ground	20	Key (No pin)
21	DREQ	22	Ground
23	/IOW	24	Ground
25	/IOR	26	Ground
27	/IOCHRDY	28	Ground
29	DACK	30	Ground
31	INTR	32	No Connect
33	SA1	34	/PDIAG
35	SA0	36	SA2
37	/CS0	38	/CS1
39	HDD ACT	40	Ground



As viewed from the connector pins

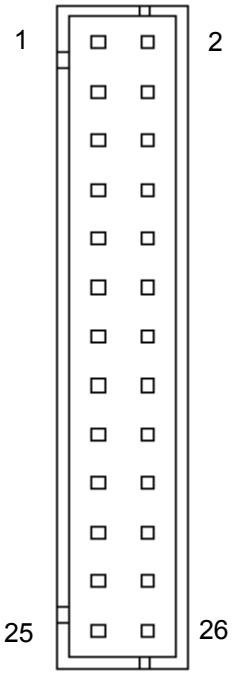
J24 – Front panel interface connector

26-way 2mm pitch shrouded header.

Mating connector: Neltron 2417HJ-26-PHD

Mating crimps: Neltron 2417TJ-PHD

Pin	Signal name	Pin	Signal name
1	+5V	2	Ground
3	RS	4	CONTRAST
5	ENABLE	6	/IOW
7	D1	8	D0
9	D3	10	D2
11	D5	12	D4
13	D7	14	D6
15	Ground (K)	16	VCC_LCD (A)
17	USER LED1	18	LED1 RES
19	USER LED2	20	LED2 RES
21	Ground	22	+5V standby
23	SMBUS Clk	24	GPIO1
25	SMBUS Data	26	GPIO2



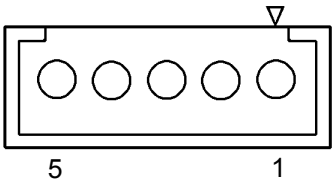
J25 – COM4 RS485/RS422 serial port

5-way 2mm pitch shrouded header.

Mating connector: JST PHR-5

Mating connector crimps: JST SPH-004T-P0.5S

Pin	Signal name (RS422)	Signal name (RS485)
1	TX-	TX-/RX-
2	TX+	TX+/RX+
3	RX-	No connect
4	RX+	No connect
5	Ground	Ground



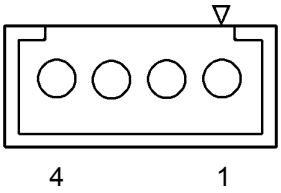
J26 – IrDA connector

4-way 2mm pitch shrouded header.

Mating connector: JST PHR-4

Mating connector crimps: JST SPH-004T-P0.5S

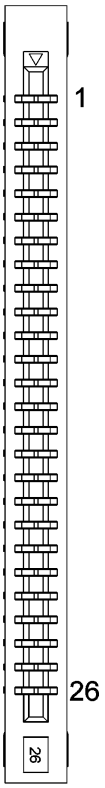
Pin	Signal name
1	TX data
2	Ground
3	RX data
4	+5V



J27 – Slimline floppy drive interface

26-way 1mm pitch FPC connector to support slimline floppy drive.

Pin	Signal name	Pin	Signal name
1	+5V	2	/INDEX
3	+5V	4	/DS0
5	+5V	6	/DSKCHG
7	NC	8	NC
9	NC	10	/MTR0
11	/DRVDEN0	12	/DIR
13	NC	14	/STEP
15	Ground	16	/WDATA
17	Ground	18	/WGATE
19	Ground	20	/TRK0
21	NC	22	/WP
23	Ground	24	/RDATA
25	Ground	26	/HDSEL



PhoenixBIOS features and setup

The APOLLO is supplied with an embedded BIOS from Phoenix. The BIOS provides the following features :

- Phoenix FirstBIOS Embedded Pro 4.0 Release 6.1.
- Plug & Play (PCI, ISA) with full legacy IO support.
- PCI Auto Configuration (PCI 2.2).
- Automatic DRAM (DDR) configuration.
- Extended system configuration data (ESCD) memory located inside flash.
- Automatic CPU detection.
- Advanced Power Management 1.2.
- ACPI, implementation compatible with ACPI V2.0, supported power states: S0, S2, S3, S4 and S5.
- SMBIOS.
- BIOS update including ‘Crisis Recovery’.
- Flash-BIOS Bootblock support for BIOS reprogramming (recovery), supported recovery-media: Floppy, USB-Floppy, CD (bootable CD with image of the crisis-floppy in boot section).
- PIO Mode 4 and Ultra DMA Mode for IDE drives.
- Support for fixed disk drives greater than 128GB (EIDE).
- USB legacy support (keyboard, mouse).
- USB advanced boot (floppy disk, hard disk, CD-ROM).
- USB 2.0 high-speed boot.
- Quick boot.
- MultiBoot (FD, HDD, CD-ROM, LAN, USB mass storage, CompactFlash®).
- System and setup password.
- Quiet Boot with customizable boot logo.
- WfM (Wired for Management) support.
- Hardware voltage, temperature and fan speed monitoring.
- Security features including tamper detection and Unique ID.

PhoenixBIOS configuration

This section explains how to use the PhoenixBIOS setup program to modify BIOS settings and control the special features of your computer.

To launch the PhoenixBIOS setup program:

1 Turn on the computer. The Power On Self Test (POST) routine starts. A short while into this routine the following message is displayed:

```
Press <F2> to enter SETUP
```

2 Press the **F2** key.

If the message disappears before you respond and you still wish to enter setup, restart the computer to try again by pressing the 'reset' button, turning it off and back on, or pressing the **Ctrl**, **Alt** and **Del** keys simultaneously.

General use

When you launch the PhoenixBIOS setup program, the *Main* menu is displayed (see page 54).

Use the ← and → keys to choose the menu you require, and then use the ↑ and ↓ keys to highlight the item or sub-menu you require on that menu. Press **Enter** to select the highlighted item or sub-menu.

The menus available are summarized in the following table:

Menu	Explanation
Main	Used for basic system configuration. See page 54.
Advanced	Used to configure the advanced features available on your system's chipset. See page 60.
Security	Used to control access to the system. See page 81.
Power	Used to configure power-management features. See page 84.
Boot	Used to specify the order in which devices are used to load the operating system when you turn on the computer. See page 86.
Exit	Provides options to save or discard changes, exit the PhoenixBIOS setup program and load default values. See page 88.

Please note:

- Information about the item currently highlighted is displayed on the right-hand side of the screen.
- The BIOS settings are stored in battery-backed RAM that retains the system configuration information when the power is turned off. An onboard EEPROM is also provided to allow for batteryless operation and to reinitialize the CMOS settings if they become corrupted. The system BIOS automatically restores the BIOS settings if it sees that the CMOS values are corrupted.

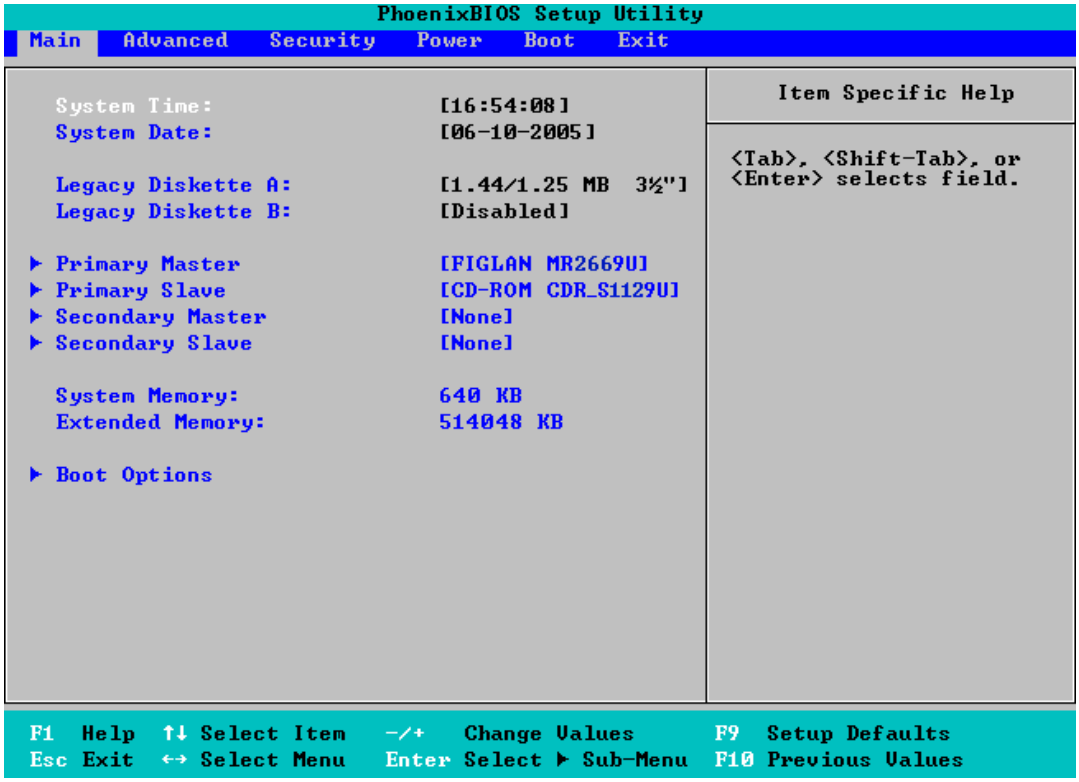
Control keys

In addition to the arrow keys, the following keys are available while using the PhoenixBIOS setup program:

Key	Explanation
Esc	From a top-level menu (e.g. *Main*, *Advanced* and *Security*), this takes you to the *Exit* menu. From any other screen, this takes you back up to the previous menu.
F1 or **ALT**-**H**	Displays help about the item currently highlighted, the keys available and the selections that can be made for this item.
F5 or **-**	Selects the previous value or selection for the item currently highlighted.
F6, **+** or **spacebar**	Selects the next value or selection for the item currently highlighted.
F9	Reverts the settings on the current sub-menu to the original factory-assigned settings
F10	Saves all changes you've made and closes the setup program.
ALT-**R**	Refreshes the current screen.

Main menu

The *Main* menu is used to specify your basic system configuration:



You can make the following selections from the *Main* menu:

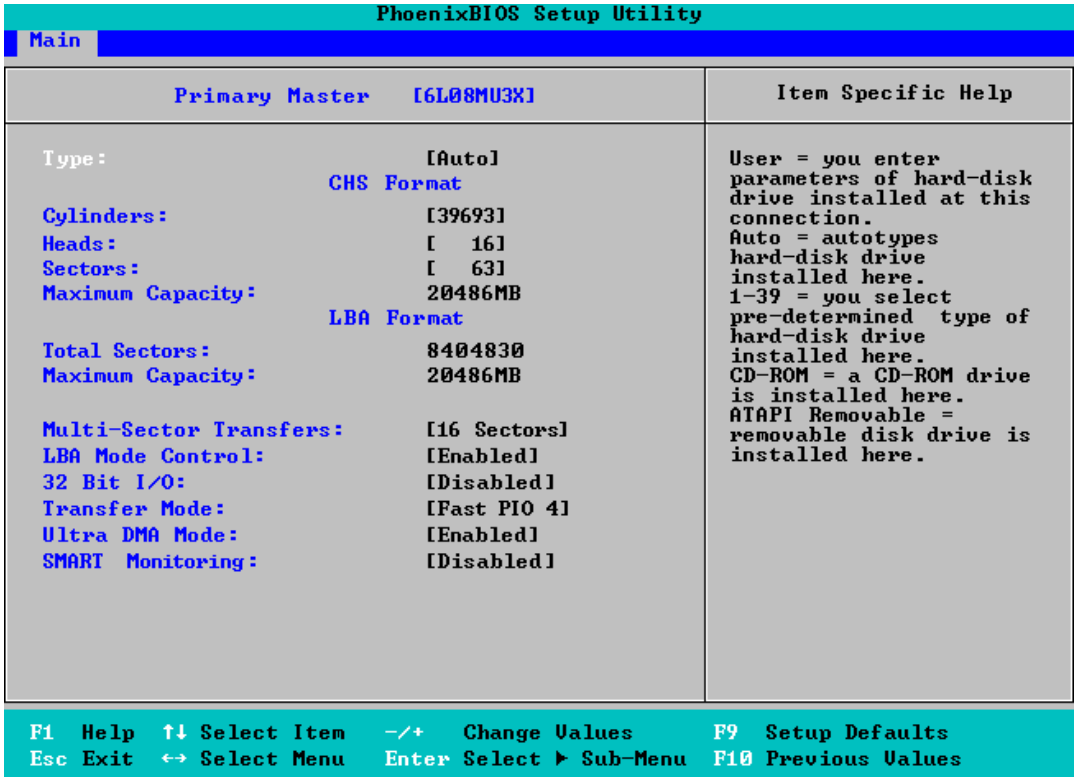
Field	Explanation
System Time, System Date	Used to set the system time and date.
Legacy Diskette A, Legacy Diskette B	Select the type of floppy disk drive(s) installed in your system. 1.25MB is a Japanese format that requires a 3½" three-mode diskette drive.
Primary Master, Primary Slave, Secondary Master, Secondary Slave	Used to specify which drives of the following types you have installed: • Hard disk drives. • Removable disk drives, e.g. Zip drives. • CD-ROM and DVD-ROM drives. See the following page for details.

Field	Explanation
System memory, Extended memory	The amount of conventional and extended memory (respectively) detected during boot-up. These values cannot be changed.
Boot Options	Used to determine what happens when the computer is turned on. For example, you can choose to boot up more quickly by skipping certain tests.

Specifying master and slave drive settings

PhoenixBIOS 4.0 supports up to two IDE disk adapters, called primary and secondary adapters. Each adapter supports one master drive and one slave drive. All combinations of master and slave drives are supported.

To specify settings for a drive, highlight it in the *Main* menu and press **Enter**. The following screen is displayed:



The details displayed vary, depending on the drive attached and its **Type**. Refer to the table on the following page for more information.

The details you are prompted to specify for the drive are explained in the following table:

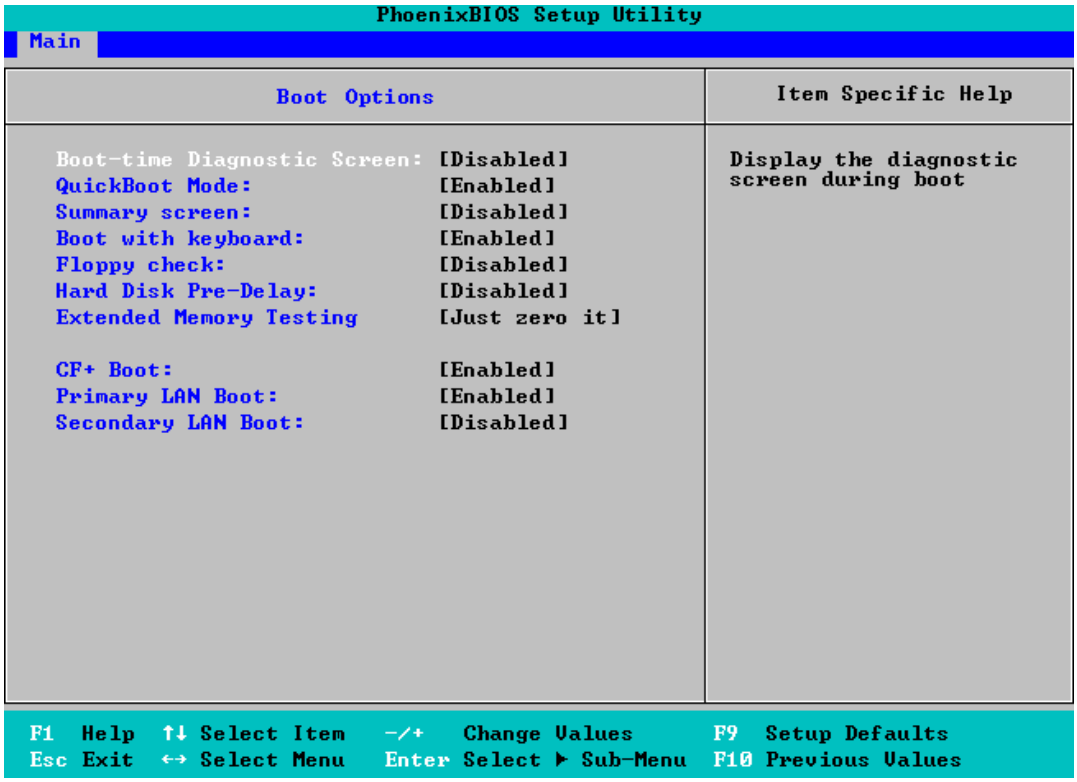
Field	Explanation
Type	Specify the type of drive installed as the selected master or slave drive. Use the **+** and **-** keys to choose a drive type. You can choose: • User. Enables you to enter details of the drive's cylinders, heads and sectors yourself. • Auto. Details of the device are completed for you automatically. This is offered by default when a drive is attached. • None. Displayed automatically if no device is attached. • ATAPI Removable. To indicate a removable ATAPI drive. • CD-ROM. To indicate a CD-ROM drive. • IDE Removable. To indicate a removable IDE drive. • Other ATAPI. To indicate any other ATAPI drive.
CHS format	If you chose **User** in the *Type* field, specify information about the drive in Cylinder/Head/Sector format, as follows: • *Cylinders*. The number of cylinders. This can be between 1 and 65,535. • *Heads*. The number of read/write heads. This must be between 1 and 16. • *Sectors*. The number of sectors per track. This must be between 1 and 63. *Maximum Capacity* shows the amount of space on the drive, in MB. Use the **+** and **-** keys to choose the numbers you require. Drives greater than 8GB operate in LBA format only.
LBA Format	If you chose **User** in the *Type* field, information is shown about the drive in Logical Block Address format: • *Total Sectors*. The total number of sectors on the drive. • *Maximum Capacity*. The maximum capacity of this drive as part of this system.

Field	Explanation
Multi-Sector Transfers	Specify the number of sectors transferred per block, if required. You can choose 2, 4, 8 or 16 sectors. Alternatively, leave this **Disabled** if you don't want to specify the number of sectors transferred.
LBA Mode Control	If you want to use LBA rather than CHS settings, set this to **Enabled**. Otherwise, leave it **Disabled**.
32 Bit I/O	Choose whether you want to enable 32bit communication between the CPU and the IDE card. You choose either **Disabled** or **Enabled**.
Transfer Mode	Choose how you want data to be transferred between the drive and the system. You are offered the options supported by the drive and platform.
Ultra DMA Mode	Select the Ultra DMA mode to be used when transferring data to and from the drive. You can choose: • Disabled • Mode 0, 1, 2, 3, 4 or 5. Ultra DMA mode supports 33/66/100MB/sec transfer rate for fixed disk drives.
SMART Monitoring	This is **Enabled** automatically if Self Monitoring Analysis and Reporting Technology is available on the drive. You cannot select it. SMART receives information from the hard drive, and provides a warning if hard drive failure is imminent.

Specifying boot options

Each time the computer is switched on, a set of checks and procedures are carried out. You can control some of the events that take place as part of this sequence. For example, if speed of booting is a primary concern, you can minimize the number of tests carried out.

To specify boot settings, highlight **Boot options** in the *Main* menu and press **Enter**. The following screen is displayed:



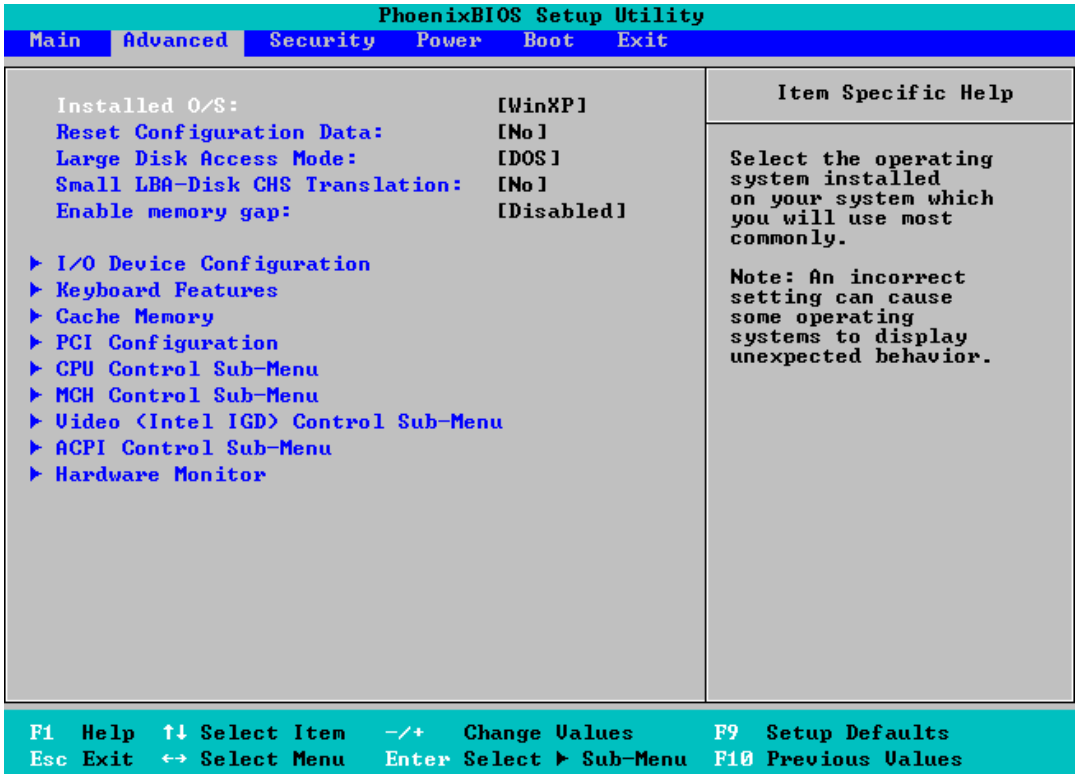
The following table explains the boot options you can choose:

Field	Explanation
Boot-time Diagnostic Screen	Choose **Enabled** if you want the diagnostic screen to be displayed during boot.
Quickboot Mode	Choose **Enabled** to skip certain tests when booting, in order to speed up the boot process.
Summary screen	Choose **Enabled** to display details of the system configuration during boot. When the summary screen is displayed press the Pause/Break key to hold the screen for closer inspection, when complete press the backslash “/” key to continue the boot.
Boot with keyboard	Choose **Enabled** if you want the Power On Self Test (POST) routine to check for attached keyboards during boot.

Field	Explanation
Floppy check	Choose **Enabled** if you want the system to check diskette drives during boot. The boot process will take longer as a result.
Hard Disk Pre-Delay	Used to introduce a delay before the BIOS first accesses the hard disk. This ensures the hard disk has time to initialize before being accessed by the BIOS. You can choose **Disabled** if you don't want to include a delay, or select one of the delay times offered. These range between 3 and 30 seconds.
Extended Memory Testing	Choose the type of tests you want to be carried out on extended memory (i.e. memory above 1M) during boot. You can choose **Normal**, **Just zero it** or **None**.
CF+ Boot	Choose **Enabled** if you want to provide CompactFlash® boot support.
Primary LAN Boot, *Secondary LAN Boot*	Choose **Enabled** if you want the LAN Controller option ROM to appear in the boot setup screen after a reboot. Network boot can then be selected from the BIOS Boot menu. On the APOLLO V2Ix boards, this option has been moved to the *IO Device Configuration → Ethernet Configuration* screen, available from the *Advanced* menu

Advanced menu

The *Advanced* menu is used to configure the advanced features available on your system's chipset:



The following table explains the settings you can choose:

Field	Explanation
Installed O/S	Choose the operating system that is to be used, e.g. WinXP. ACPI configuration settings are adjusted for each selected OS to provide optimum system performance.
Reset Configuration Data	Used to clear the Extended System Configuration Data (ESCD) area. Select either **Yes** (to clear the area) or **No**. When you select **Yes**, the BIOS reinitializes the ECSD data on the next boot.
Large Disk Access Mode	Indicate whether the operating system you're using is DOS or not. You are offered **DOS** by default. Change this to **Other** if you have an operating system other than DOS, e.g. UNIX. If the drive configuration shown in BIOS is incorrect when you attempt to install new software, try changing this setting. A large disk is one with more than 1024 cylinders, 16 heads or 63 tracks per sector.

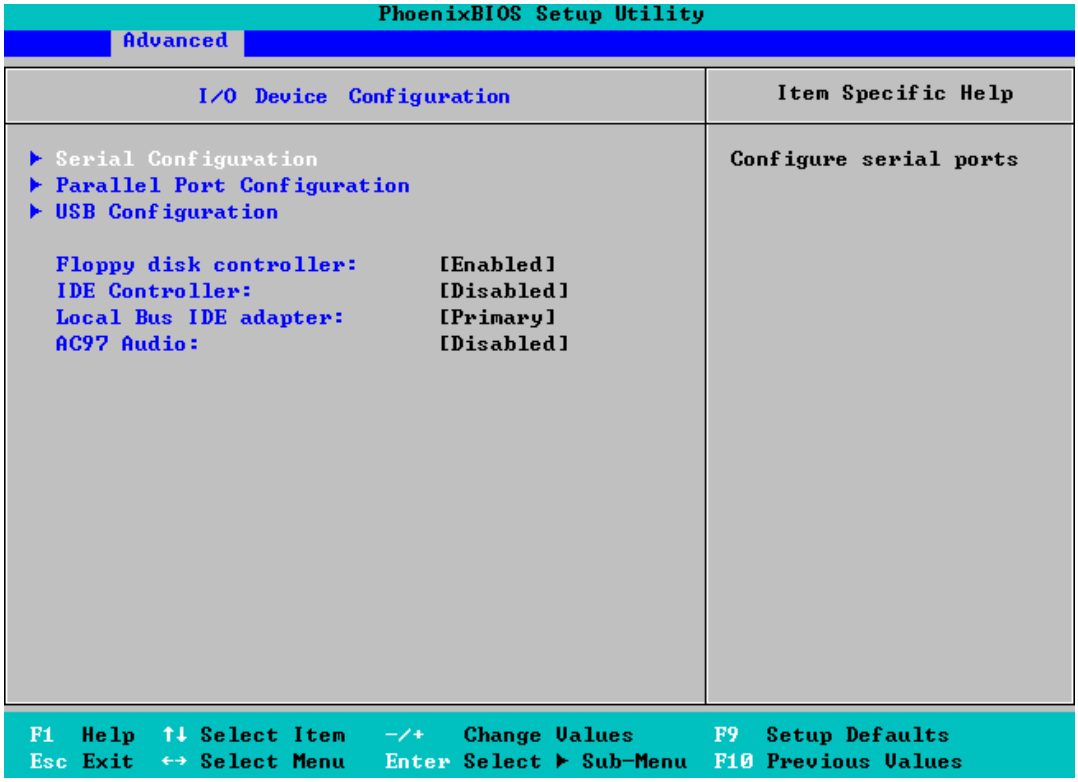
Field	Explanation
Small LBA-Disk CHS Translation	Determines whether CHS translation is made for LBA-capable hard disks with less than 1024 cylinders. You can choose either **Yes** (translate CHS for all LBA-capable disks) or **No** (translate CHS only if the hard disk drive has more than 1024 cylinders). Try changing this if you have problems booting from a CompactFlash®.
Enable memory gap	Used to free up address space for use with an option card. Choose **Enabled** to create a 1MB extended memory gap in the system RAM, starting at 15MB.
I/O Device Configuration	Displays a sub-menu containing options you can use to set up Input/Output ports. See page 62 for details.
Keyboard Features	Displays a sub-menu containing options you can use to control aspects of how the keyboard works. See page 68 for details.
Cache Memory	Displays a sub-menu containing options you can use to specify cache memory settings. See page 69 for details.
PCI Configuration	Displays a sub-menu containing options you can use to configure PCI devices. See page 70 for details.
CPU Control Sub-Menu	Displays a sub-menu containing options you can use to control how the CPU operates. See page 73 for details.
MCH Control Sub-Menu	Displays a sub-menu containing options you can use to control how the Memory Controller Hub operates. See page 75 for details.
Video (Intel IGD) Control Sub-Menu	Displays a sub-menu containing options you can use to configure the Internal Graphics Device. See page 76 for details.
ACPI Control Sub-Menu	Displays a sub-menu containing options you can use to configure ACPI settings. See page 78 for details.
Hardware Monitor	Displays a sub-menu where you can view details of system hardware temperature and voltages, as well as controlling the system and CPU fans. See page 79 for details.

Specifying I/O device configuration settings

The system communicates with external devices (such as printers) through Input/Output ports (I/O ports). You can configure the settings of these ports. For example, you can specify the I/O address or the interrupt line to be used by the I/O port.

These settings are often configured automatically by the BIOS or the operating system. Sometimes, however, you must set them up manually. This is often because a device is not 'plug and play'.

To specify I/O device configuration settings, highlight **I/O Device Configuration** in the *Advanced* menu and press **Enter**. The following screen is displayed:



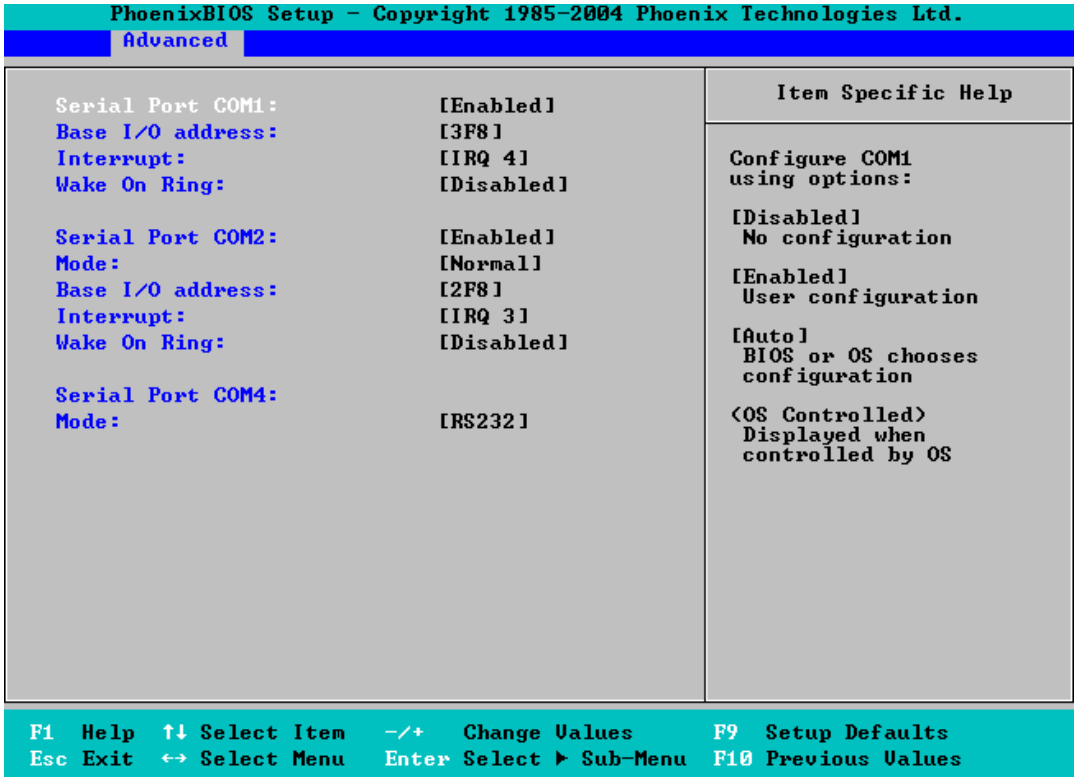
The details you are prompted to specify are explained in the following table:

Field	Explanation
Serial Configuration	Displays a sub-menu containing options you can use to configure serial ports. See page 64 for details.
Parallel Port Configuration	Displays a sub-menu containing options you can use to configure parallel ports. See page 66 for details.
USB Configuration	Displays a sub-menu containing options you can use to configure USB ports. See page 67 for details.

Field	Explanation
Floppy disk controller	Used to configure the floppy disk controller. The options available are: • Disabled. The port is not configured at all - it is turned off. • Enabled. You are going to configure the port (by completing the following fields). • Auto. The port is configured automatically by the BIOS or the operating system. **OS Controlled** is displayed if configuration of the port is controlled by the operating system.
IDE Controller	Choose whether to enable or disable the IDE controller. This should be **Enabled** for CompactFlash® boot, even if the onboard IDE is not being used.
Local Bus IDE adapter	Choose which IDE adapter (or adapters) is to be enabled. You can select **Primary** channel, the **Secondary** channel, **Both** or neither (choose **Disabled**). The APOLLO supports only a single IDE hard drive connection, which is the primary IDE adapter. However, the secondary IDE adapter must be enabled for the CompactFlash boot functionality to operate correctly. This means that, for correct operation of the CompactFlash boot feature, you should ensure that the secondary IDE adapter is enabled (i.e. that you select either **Secondary** or **Both**).
AC97 Audio	Choose whether to enable or disable the onboard AC97 audio device.

Configuring serial ports

To specify serial configuration settings, highlight **Serial Configuration** in the *I/O Device Configuration* menu and press **Enter**. The following screen is displayed:



The details you are prompted to specify are explained in the following table:

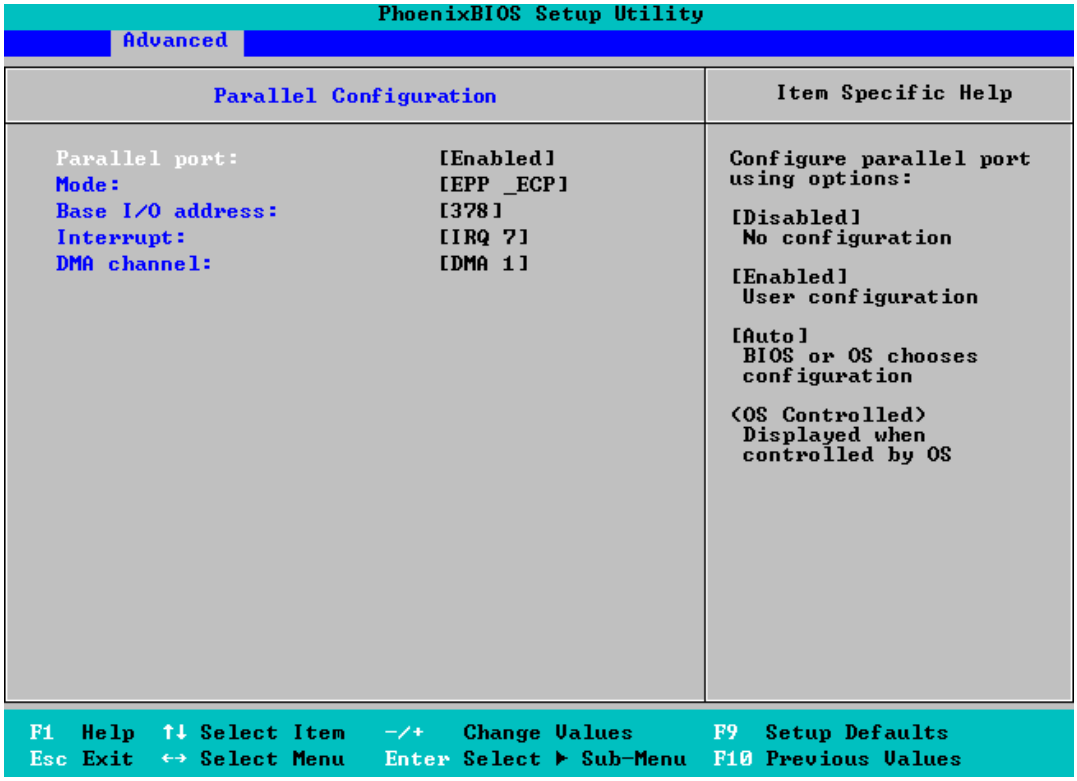
Field	Explanation
Serial Port COM1	Choose how this port is to be configured by selecting one of the following: • Disabled. The port is not configured at all - it is turned off. • Enabled. You are going to configure the port (by completing the following fields). • Auto. The port is configured automatically by the BIOS or the operating system. **OS Controlled** is displayed if configuration of the port is controlled by the operating system.
Base I/O Address	Specify the I/O address to be used by serial port COM1. This can be 2E8, 3E8, 2F8 or 3F8.
Interrupt	Specify the interrupt line to be used by serial port COM1. This can be IRQ3 or IRQ4.

Field	Explanation
Wake On Ring	Choose whether the computer is to wake from standby/hibernation in response to a Ring Indicator (RI) signal from serial port COM1.
Serial port COM2	Choose how this port is to be configured. The options available are the same as for *Serial Port COM1*, above.
Mode	Set the mode for this port. This can be: • Normal: Standard RS232 mode. • ASK-IR: Sharp Amplitude Shift Keying mode. • **IRDA**: IrDA 1.0 infrared communications mode.
Base I/O Address	Specify the I/O address to be used by serial port COM2. This can be 2E8, 3E8, 2F8 or 3F8.
Interrupt	Specify the interrupt line to be used by serial port COM2. This can be IRQ3 or IRQ4.
Wake On Ring	Choose whether the computer is to wake from standby/hibernation in response to a Ring Indicator (RI) signal from serial port COM2.
Serial Port COM4	This serial port is based on a PCI UART, so has no I/O address or interrupt line configuration options. You can, however, specify the interface mode for this port (see below).
Mode	Set the mode for serial port COM4. You are offered **RS232** by default. You can change this, if required, to **RS485** or **RS422**, which provide additional flow control options related to auto RTS. Auto RTS flow control provides a mechanism whereby the serial port automatically switches the RS485/422 transceiver from being a transmitter to a receiver once the last byte has been transmitted. This means the user can simply read and write to the device as if it were a normal serial port.

Serial Port COM3 has no BIOS configuration options as it based on a PCI UART and provides only RS232 output.

Configuring parallel ports

To specify parallel port configuration settings, highlight **Parallel Port Configuration** in the *I/O Device Configuration* menu and press **Enter**. The following screen is displayed:

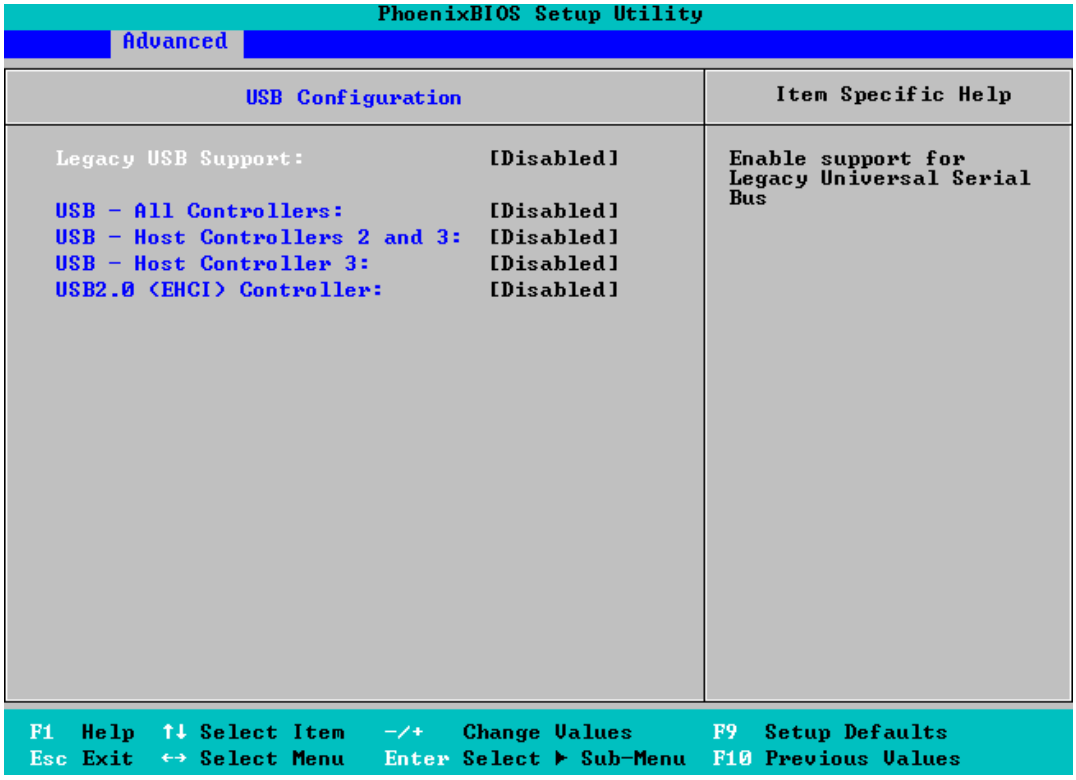


The details you are prompted to specify are explained in the following table:

Field	Explanation
Parallel port	Choose how this port is to be configured. The options available are: • Disabled. The port is not configured at all - it is turned off. • Enabled. You are going to configure the port (by completing the following fields). • Auto. The port is configured automatically by the BIOS or the operating system. **OS Controlled** is displayed if configuration of the port is controlled by the operating system.
Mode	Set the mode for the parallel port. The options you can choose are listed in the **Item Specific Help** panel on the right.
Base I/O Address	Specify the I/O address to be used by the parallel port. This can be 378 or 278.
Interrupt	Specify the interrupt line to be used by the parallel port. This can be IRQ5 or IRQ7.
DMA channel	Set up the DMA channel for the parallel port. You can choose **DMA 1** or **DMA 3**.

Configuring USB ports

To specify USB configuration settings, highlight **USB Configuration** in the *I/O Device Configuration* menu and press **Enter**. The following screen is displayed:



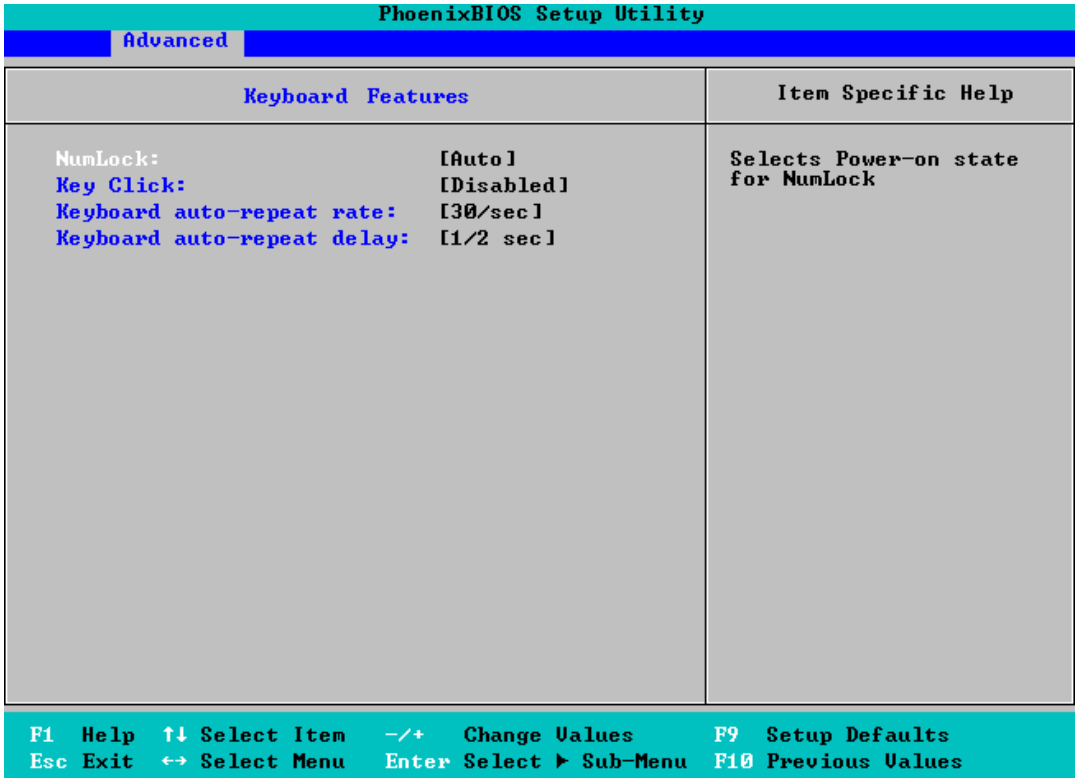
The details you are prompted to specify are explained in the following table:

Field	Explanation
Legacy USB Support	Choose **Enabled** to include support for Legacy USB.
USB – All Controllers	Choose whether to enable or disable all USB functions.
USB – Host Controllers 2 and 3	Choose whether to enable or disable these USB functions.
USB – Host Controller 3	Choose whether to enable or disable this USB function.
USB2.0 (EHCI) Controller	Choose whether to enable or disable USB 2.0 functionality.

Specifying keyboard feature settings

You can control some aspects of the way a keyboard that is connected to the computer will work. For example, you may want users to hear a sound each time they press a key, or you might choose to switch on **Num Lock** by default each time they turn the computer on.

To specify keyboard feature settings, highlight **Keyboard Features** in the *Advanced* menu and press **Enter**. The following screen is displayed:



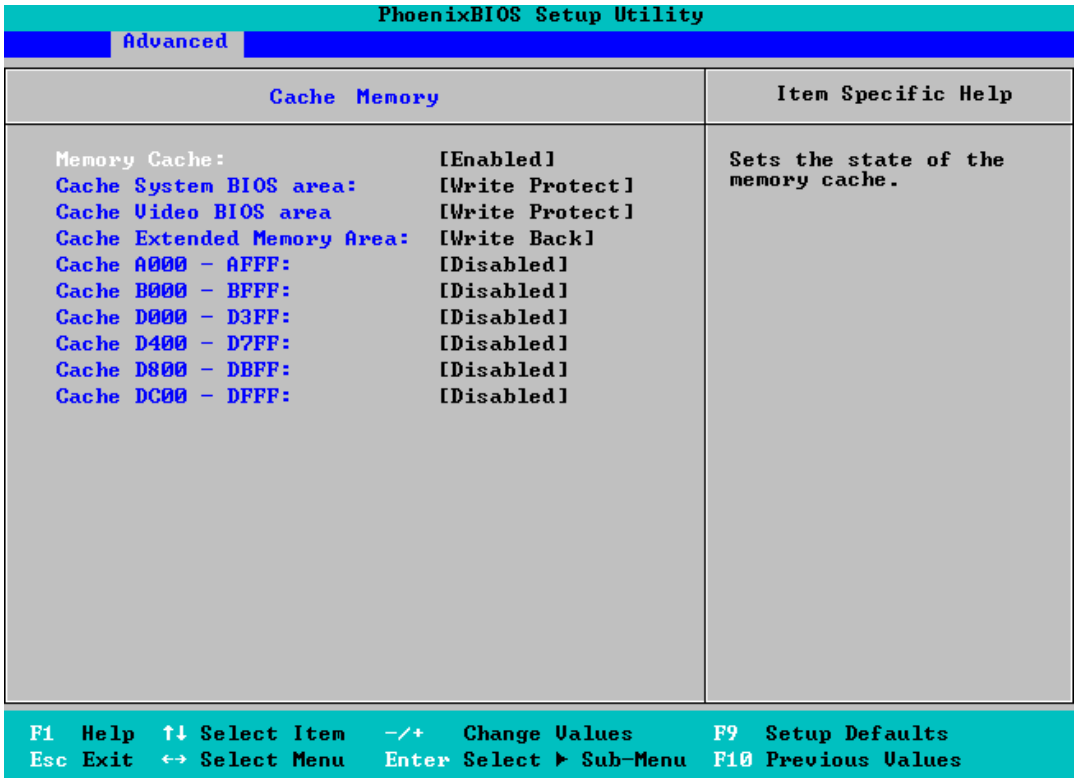
The details you are prompted to specify for the keyboard are explained in the following table:

Field	Explanation
NumLock	Determine whether **Num Lock** is to be turned on or off by default when the computer is switched on. You can choose: • On. Num Lock is switched on when the computer starts up. • Off. Num Lock is switched off when the computer starts up. • Auto. If a numeric keypad is detected, Num Lock is turned on automatically. Otherwise, it is turned off.
Key Click	Choose whether users should be able to hear a sound each time they press a key. You can choose **Enabled** or **Disabled**.
Keyboard auto-repeat rate	Choose how many times per second a keystroke is to be repeated if the key is held down. You can choose **2**, **6**, **10**, **13.3**, **18.5**, **21.8**, **26.7** or **30** times per second.
Keyboard auto-repeat delay	Choose how long a key must be held down before auto-repeat begins. This can be ¼, ½, ¾ or 1 second.

Specifying cache memory settings

Using the memory cache can increase speed of access to data. When the memory cache is enabled, recently accessed data is stored in SRAM, which is faster than regular memory. Before accessing data in the regular memory, the CPU checks the cache. If the data is not held in the cache, the CPU accesses regular memory as usual.

To specify cache memory settings, highlight **Cache Memory** in the *Advanced* menu and press **Enter**. The following screen is displayed:



The details you are prompted to specify for the memory cache are explained in the following table:

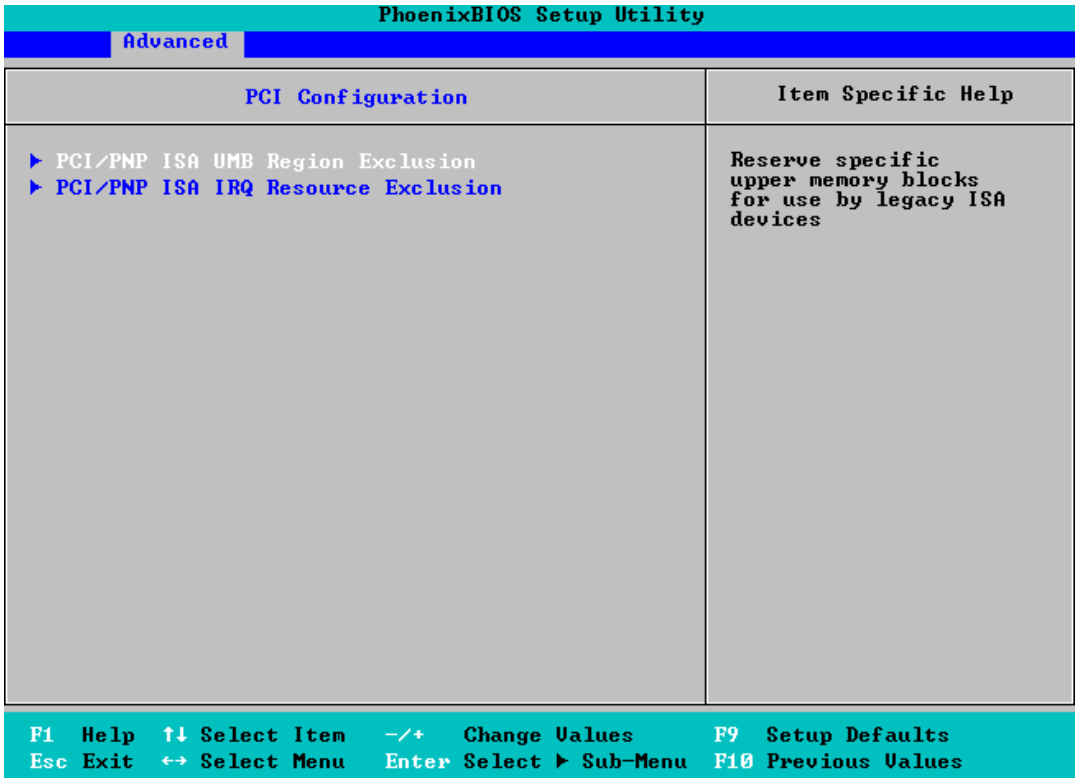
Field	Explanation
Memory Cache	Choose to enable or disable all memory caching.
Cache System BIOS area	Choose whether to cache the system BIOS. Doing so is likely to improve system performance significantly. You are offered **Write Protect** by default. This means the system BIOS is cached. (The system BIOS is always write protected.) If you don't want to cache the system BIOS, choose **uncached**. Please note that system performance may decrease rapidly as a result.

Field	Explanation
Cache Video BIOS area	Choose whether to cache the video BIOS to improve performance. You are offered **Write Protect** by default. This means the video BIOS is cached. (The video BIOS is always write protected.) If you don't want to cache the video BIOS, choose **uncached**. Please note that performance may decrease rapidly as a result.
Cache Extended Memory Area	Choose whether to cache system memory above 1MB. You can choose **uncached**, **Write Through**, **Write Protect** or **Write Back**.
Cache A000 - AFFF to Cache DC00 - DFFF	Used to control caching of individual segments of memory. The options you can choose for each segment are listed in the **Item Specific Help** panel on the right.

Specifying PCI configuration settings

PCI devices are those that communicate with the CPU via the PCI bus. You can reserve memory blocks and IRQ for use by installed PCI devices.

To specify PCI configuration settings, highlight **PCI Configuration** in the *Advanced* menu and press **Enter**. The following sub-menu is displayed:

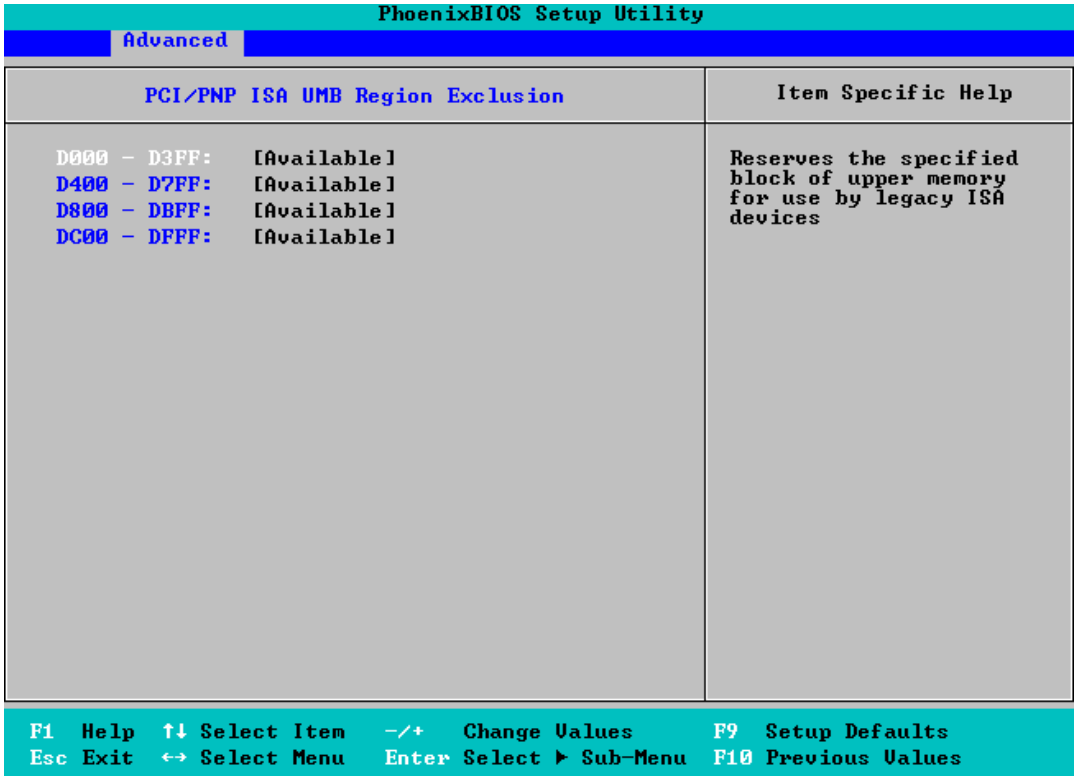


The options available to select from the *PCI Configuration* sub-menu are explained in the following table:

Field	Explanation
PCI/PNP ISA UMB Region Exclusion	Displays a sub-menu containing options you can use to reserve blocks of memory for use by legacy ISA devices. See the following page for details.
PCI/PNP ISA IRQ Resource Exclusion	Displays a sub-menu containing options you can use to reserve IRQs for use by legacy ISA devices. See page 72 for details.

PCI/PNP ISA UMB region exclusion settings

When you select *PCI/PNP ISA UMB Region Exclusion* from the *PCI Configuration* menu, the following screen is displayed:

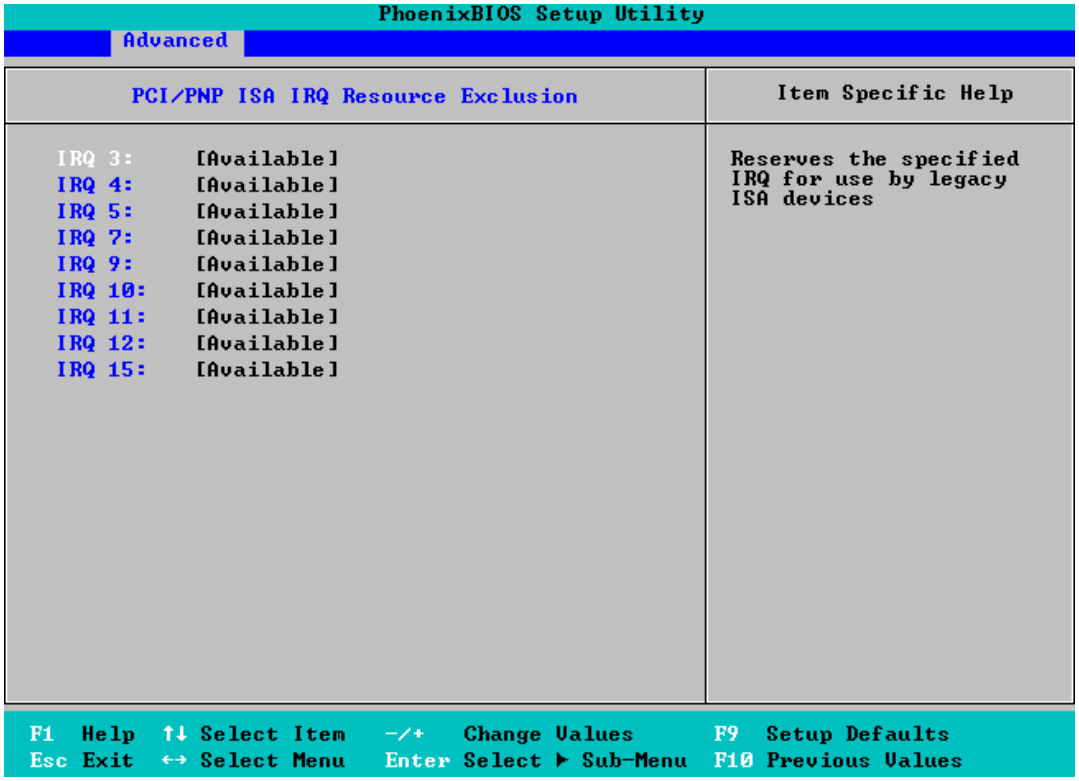


The blocks of memory in the system are listed. They are all **Available** by default. To reserve a block of memory, simply change the corresponding selection from **Available** to **Reserved**.

If you no longer want to reserve a block of memory (e.g. you reserved the wrong block by mistake), change the selection back to **Available**.

PCI/PNP ISA IRQ resource exclusion settings

When you select *PCI/PNP ISA IRQ Resource Exclusion*, the following screen is displayed:



The IRQs in the system are listed. They are all **Available** by default. To reserve an IRQ, simply change the corresponding selection from **Available** to **Reserved**.

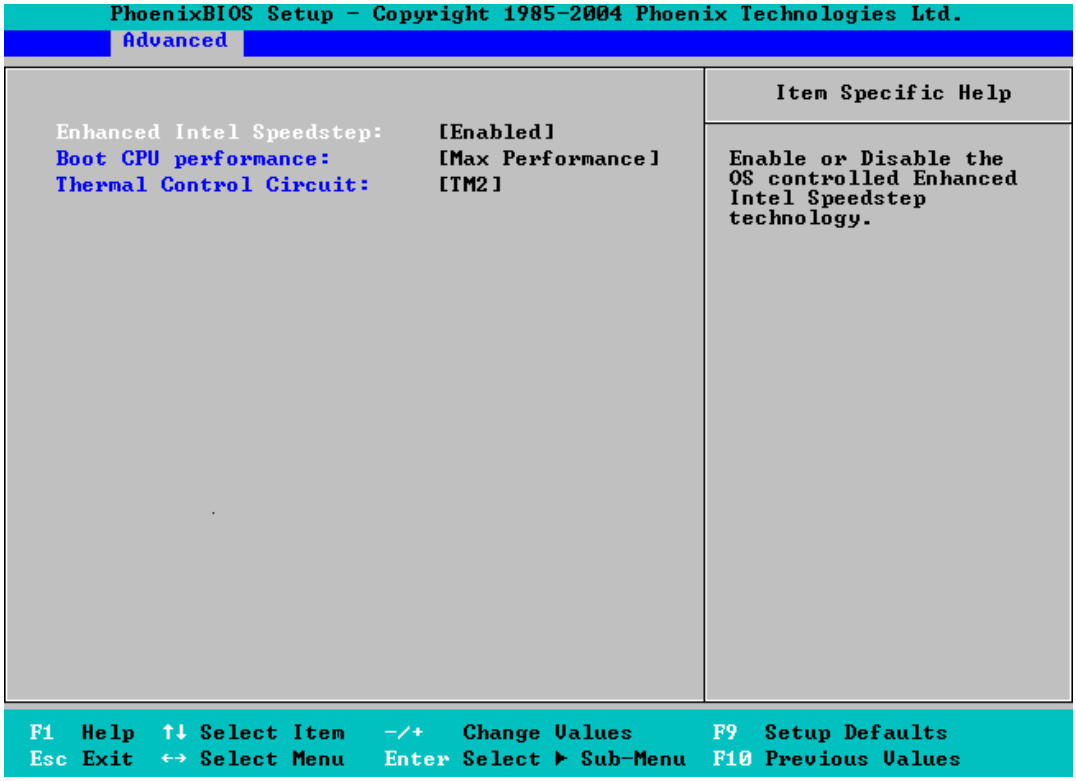
If you no longer want to reserve an IRQ (e.g. you reserved the wrong one by mistake), change the selection back to **Available**.

IRQ 15 is used for CompactFlash® boot. This cannot be changed.

CPU control settings

You can specify settings that affect how the CPU operates.

To specify CPU control settings, highlight **CPU Control Sub-Menu** in the *Advanced* menu and press **Enter**. The following screen is displayed:



The details you are prompted to specify are explained in the following table:

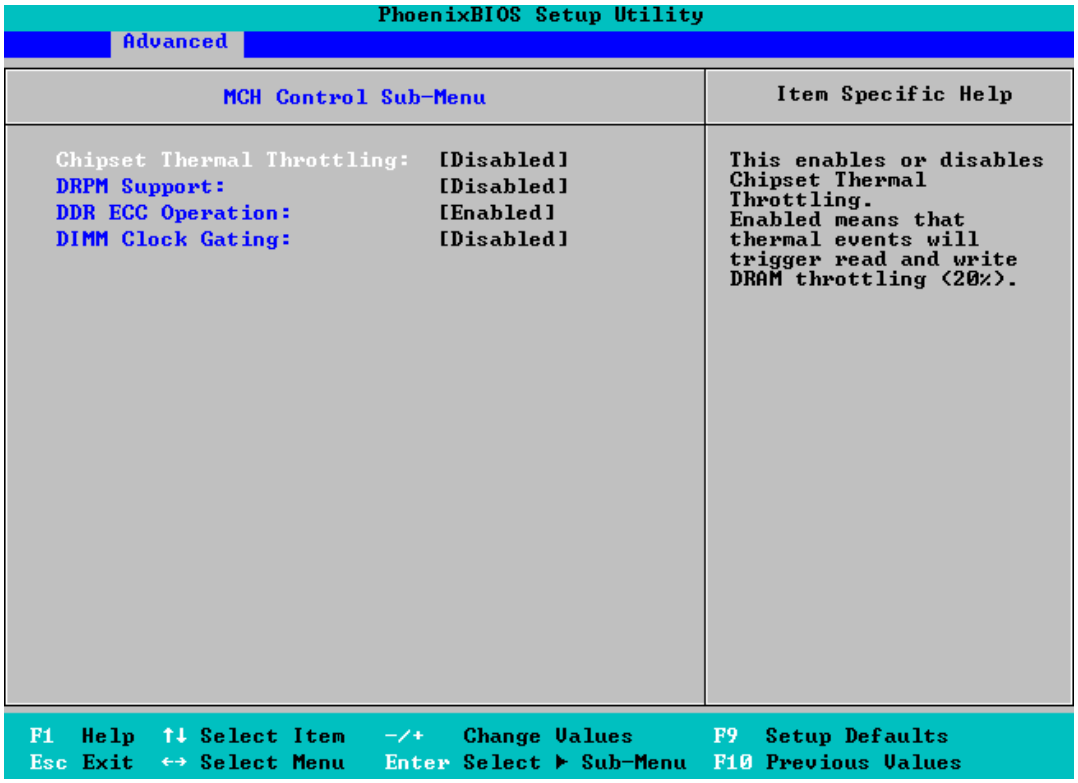
Field	Explanation
Enhanced Intel Speedstep	Choose whether Enhanced Intel Speedstep is to be enabled. This feature is available with Intel Pentium M® processors and is supported by most operating systems.
Boot CPU Performance	Choose the level of CPU performance required on boot. The options available from are explained in the **Item Specific Help** panel on the right-hand side of the screen.

Field	Explanation
Thermal Control Circuit	Used to enable the Thermal Control Circuit (TCC) portion of the Thermal Monitor feature of the CPU. You can choose: • TM1: Thermal Monitor 1. This is the supported mode for Intel Celeron M processors. If the processor reaches its critical temperature (100°C/212°F), TM1 modulates the processor clock, turning it on and off at a 50% duty cycle. This halves the processor speed and cools it (because clock speed and power consumption are proportional). • TM2: Thermal Monitor 2. For Pentium M processors that support Enhanced Intel Speedstep and allow for the processor frequency to be changed from the maximum processor speed down to 600MHz. In this mode the thermal monitor can provide maximum performance under high temperature conditions. • Disabled: Disables the TCC, the processor will shutdown itself down if it's absolute maximum temperature is reached 125°C.

MCH control settings

You can specify settings that affect how the Memory Controller Hub operates.

To specify MCH control settings, highlight **MCH Control Sub-Menu** in the *Advanced* menu and press **Enter**. The following screen is displayed:



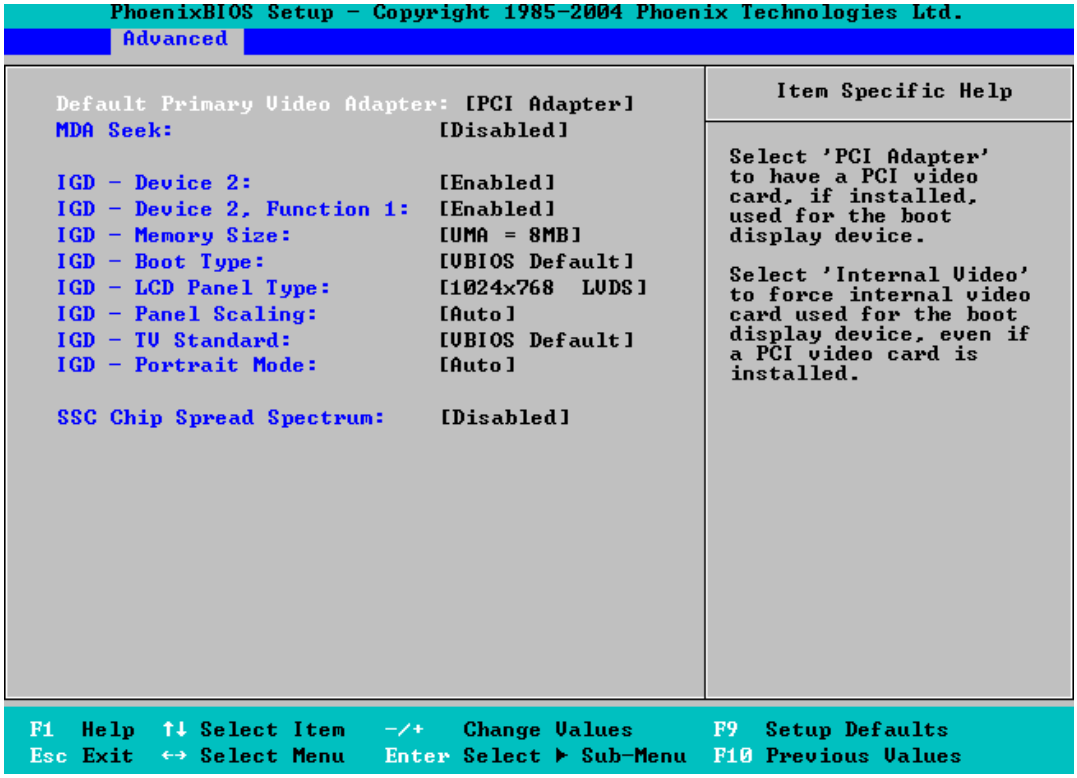
The details you are prompted to specify are explained in the following table:

Field	Explanation
Chipset Thermal Throttling	Choose whether to enable or disable Chipset Thermal Throttling. If you choose **Enabled**, thermal events trigger read and write DRAM throttling.
DRPM Support	Choose whether to enable or disable DRPM (Dynamic Row Power Management) support in the MCH. If you choose **Enabled**, memory clocks are turned off when not in use.
DDR ECC Operation	Choose **Enabled** if you want the system to check SODIMMS support before enabling ECC. This option is not available if ECC is not supported by the DIMMs.
DIMM Clock Gating	Choose **Enabled** if you want to control enabling of the DIMM Clock Gating feature.

Video (Intel IGD) control settings

You can specify settings that determine how the Internal Graphics Device operates.

To specify video (Intel IGD) control settings, highlight **Video (Intel IGD) Control Sub-Menu** in the *Advanced* menu and press **Enter**. The following screen is displayed:



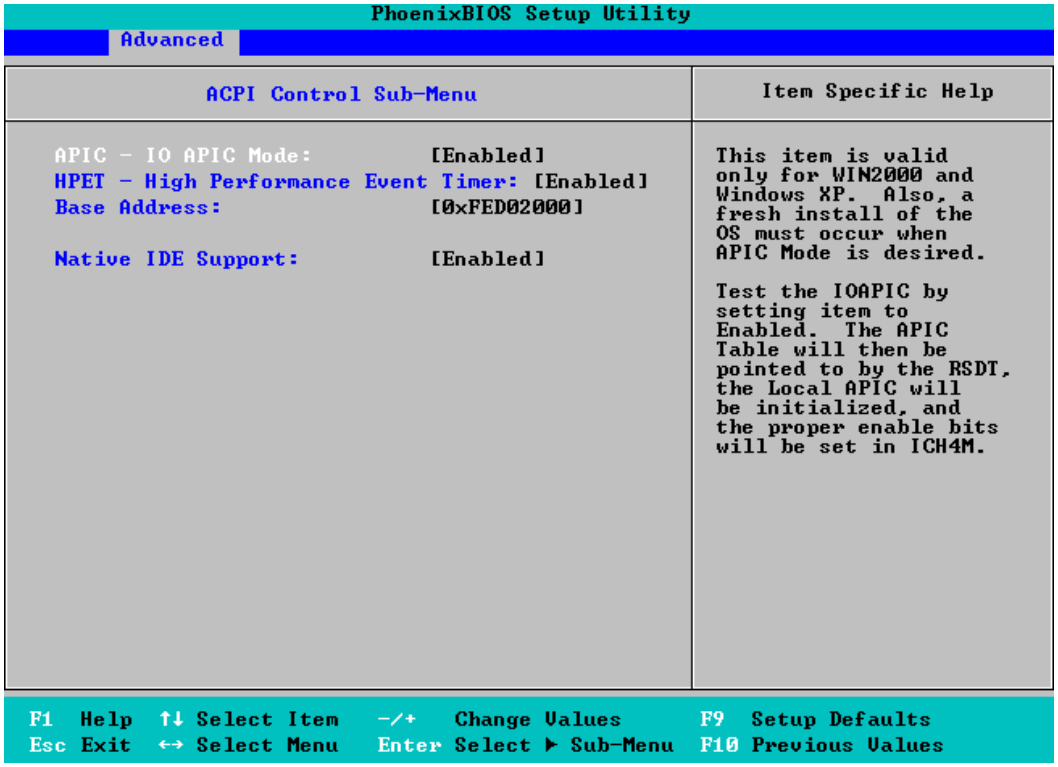
The details you are prompted to specify are explained in the following table:

Field	Explanation
Default Primary Video Adapter	Choose the type of video card to be used for the boot display device. You can choose **PCI Video Adapter** or **Internal Video**. If dual monitor support is required when using a PCI Video Adapter, the Primary Video Adapter should be configured to use the PCI Video Adapter.
MDA Seek	Choose **Enabled** if you want the system to seek an MDA video adapter during boot.
IGD – Device 2	Choose whether to enable or disable the Internal Graphics Device.

Field	Explanation
IGD – Device 2, Function 1	Choose whether to enable or disable IGD - Device 2, Function 1. This is the second graphics controller on the 855GME chipset. This chipset has two graphics controllers integrated within one device, thus enabling two independent displays showing different images. You can turn off the second graphics controller here, for example if you want to support other video cards.
IGD – Memory Size	Choose how much Main Memory the Internal Graphics Device is to use. You can choose **1**, **8**, **16** or **32**MB.
IGD – Boot Type	Choose the video device to be activated during the POST routine. The options you can choose from are listed in the **Item Specific Help** panel.
IGD – LCD Panel Type	Choose the LCD panel to be used by the Internal Graphics Device.
IGD – Panel Scaling	Choose the LCD panel scaling option to be used by the Internal Graphics Device. You can choose: • Auto to use the Intel video BIOS setting. • Force Scaling to scale a lower resolution image so that it fits a higher resolution display. • Off to use the designated resolution. This may result in a border around the image when it is displayed on screen. For these settings to work correctly, the attached display must support EDID (Extended Display Identification Data). This gives the video BIOS an indication of the native resolution of the display.
IGD – TV Standard	Choose the TV signal transmission standard used by the Internal Graphics Device. The options available are listed in the **Item Specific Help** panel on the right-hand side.
IGD - Portrait Mode	Specify whether portrait mode in the Internal Graphics Device is **Enabled** or **Disabled**. Alternatively select **Auto**, in which case the setting is based on setup tables in the BIOS and on the EDID readback from the display.
SSC Chip Spread Spectrum	Choose whether to use the spread spectrum feature of the Spread Spectrum Clock chip, by selecting either **Enabled** or **Disabled**.
SSC value	Choose the % spread to be used.

ACPI control settings

You can control ACPI (Advanced Configuration and Power Interface) settings. To do this, highlight **ACPI Control Sub-Menu** in the *Advanced* menu and press **Enter**. The following screen is displayed:



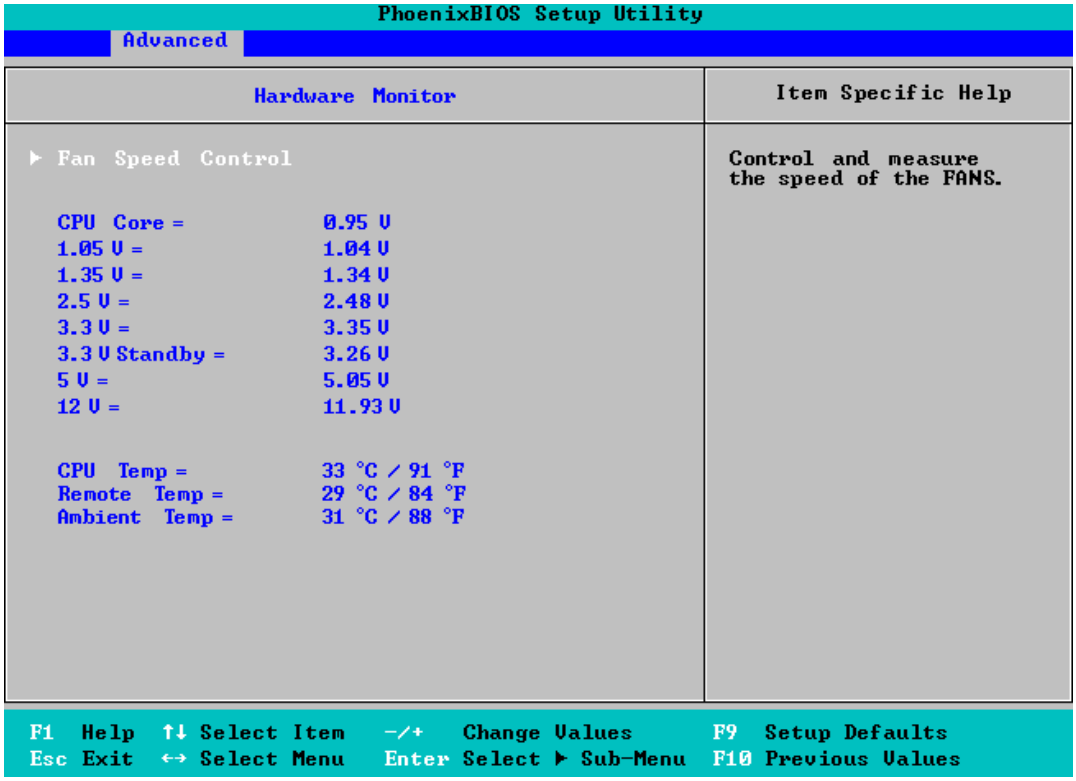
The details you are prompted to specify are explained in the following table:

Field	Explanation
APIC - IO APIC Mode	Choose **Enabled** to set the APIC interrupt mode. See pages 98 and 125 for further information about the APIC Advanced Interrupt Controller.
	This is only valid in Windows XP and Windows 2000. You must re-install the operating system if you want to change to APIC mode.
HPET - High Performance Event Timer	Choose **Enabled** to test the High Performance Event Timer (HPET).
	This is only valid in Windows XP.
Base Address	Specify the base address for the HPET.
Native IDE Support	Select **Enabled** if you want to include Native IDE support for Windows XP. If you do this, the NATA package is created.
	This setting has no effect in Win98, WinME or Win2000.

Monitoring hardware

You can monitor the temperature and voltage of hardware attached to your APOLLO.

To do this, highlight **Hardware Monitor** in the *Advanced* menu and press **Enter**. The following screen is displayed:

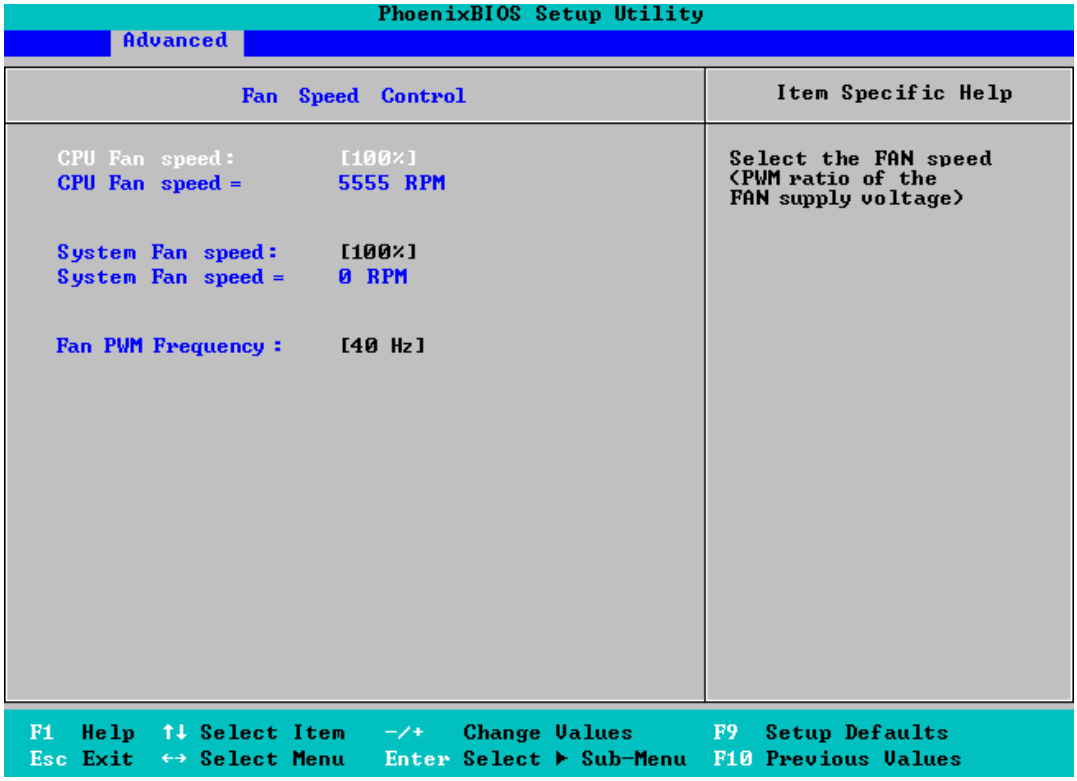


The system voltages and temperatures are shown in real-time. For each voltage required by components, the actual voltage being passed is displayed.

In addition, you can click on **Fan Speed Control** to view and control the system and CPU fan settings. See the following section for more information.

Maintaining system fan settings

When you select *Fan Speed Control* from the *Advanced* menu, the following screen is displayed:

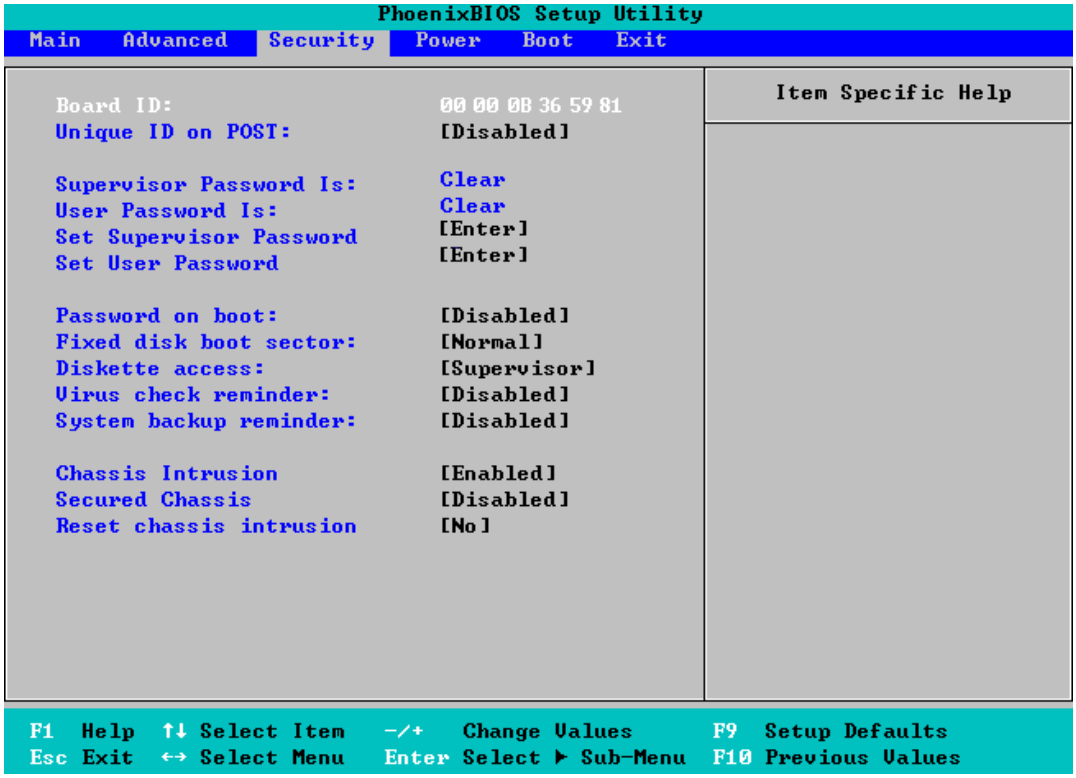


The details you are prompted to specify are explained in the following table:

Field	Explanation
CPU Fan speed	The speed at which the processor fan is currently operating is shown in blue. You can control the speed at which this fan operates. You do this by selecting the proportion of its maximum capacity that the fan is to operate at. (In the example shown, the fan is set to work at 100% of its maximum capacity, i.e. 5555RPM.)
System Fan speed	The speed at which the additional system fan is currently operating is shown in blue (if there is one). You can choose to attach an additional fan if required. This may be, for example, a chassis mounted fan to control airflow within the enclosure. You can control the speed at which this system fan operates. You do this by selecting the proportion of its maximum capacity that the fan is to operate at. (In the example shown, the fan is set to work at 100% of its maximum capacity.)
Fan PWM Frequency	Select the frequency of the Pulse Width Modulation signal for the fan speed control that best suits the fan used. This can be 40Hz or 120Hz.

Security menu

The *Security* menu is used to control access to the system and to set up reminders, for example, to prompt users to backup the system and check for viruses on a regular basis:



The following table explains the security settings you can choose:

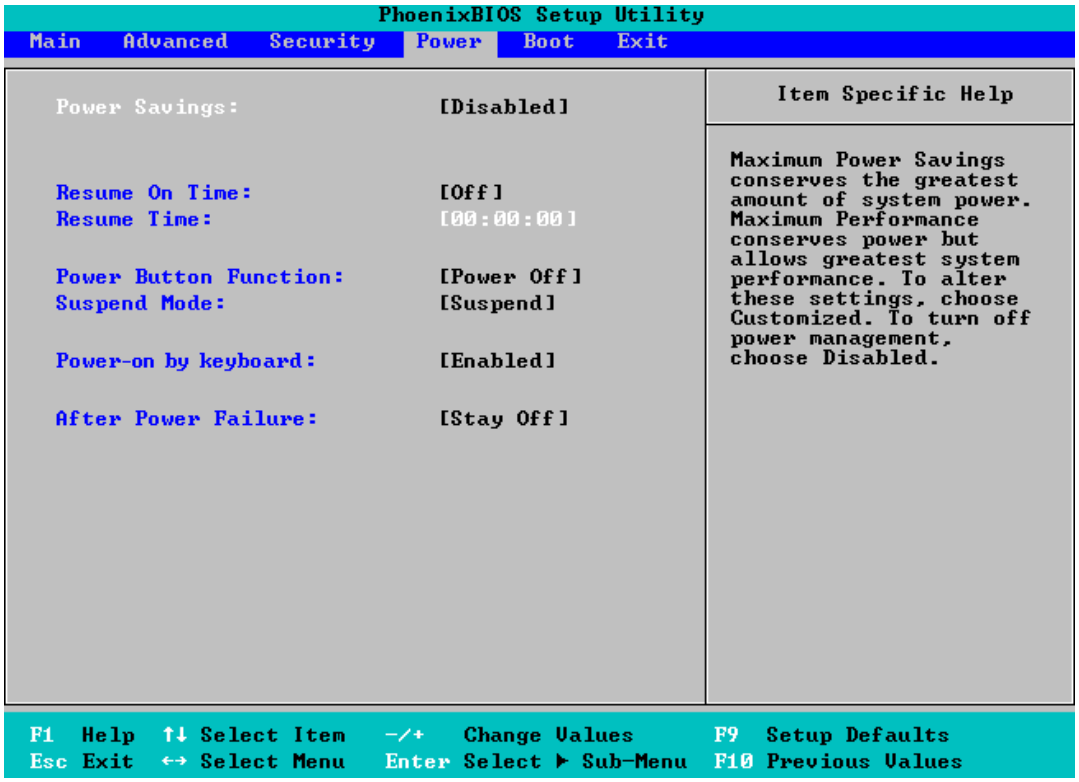
Field	Explanation
Board ID	The 48-bit unique ID, read from the on-board DS2401 device.
Unique ID on POST	Choose **Enabled** if you want this ID to be displayed during POST.
Supervisor Password Is	Indicates whether a supervisor password has been created (**Set**). **Clear** indicates that no supervisor password has been created. You can create or change the supervisor password in the *Set Supervisor Password* field.
User Password Is	Indicates whether a user password has been created (**Set**). **Clear** indicates that no user password has been created. You can create or change the user password in the *Set User Password* field.

Field	Explanation
Set Supervisor Password	Used to specify a password to access system setup. Once you've set a supervisor password, only those who enter this password can view the setup menus in full. To create a supervisor password, press **Enter**. The **Set Supervisor Password** dialog is displayed, ready for you to type the new password. This can be up to eight characters long. To change an existing supervisor password, press **Enter**. The **Set Supervisor Password** dialog is displayed. Type the current password followed by the new password. If you want to remove the supervisor password completely, type the current password and then press **Enter** in both **New Password** fields (i.e. leave them blank). Existing user passwords cannot be changed if the supervisor password has been cleared or has not yet been set.
Set User Password	Used to specify a password that gives restricted access to system setup menus. To create a user password, press **Enter**. The **Set User Password** dialog is displayed, ready for you to type the new password. This can be up to eight characters long. To change an existing user password, press **Enter**. The **Set User Password** dialog is displayed. Type the current password followed by the new password. If you want to remove the user password, type the current password and then press **Enter** in both **New Password** fields (i.e. leave them blank). You cannot create or change the user password if no supervisor password has been set.
Password on boot	Used to force users to enter a password each time the computer is turned on. Choose either **Enabled** or **Disabled**. You must have set up a supervisor password for this to take effect. If you leave this option **Disabled** and have set up a supervisor password, access to system setup when the computer is turned on is provided at the user rather than at the supervisor level.
Fixed disk boot sector	Choose whether to write protect the boot sector on the hard disk for protection against viruses. This means that a password must be entered before a user can format or Fdisk the hard disk. Choose either **Normal** or **Write Protect**.

Field	Explanation
Diskette access	Choose the level of permission required to boot from or access the floppy disk. Select either **User** or **Supervisor**.
Virus check reminder	Choose whether you want to remind users about virus checking. A message is displayed each time the computer is turned on, until the user confirms that they have scanned for viruses. You can choose: • Disabled. • Daily. The message is displayed on the first boot of each day. • Weekly. The message is displayed on the first boot after Sunday. • Monthly. The message is displayed on the first boot of the month.
System backup reminder	Choose whether you want to remind users to back up the system. The same options are available as for *Virus check reminder*, above.
Chassis Intrusion	Choose **Enabled** if you want physical tampering with the computer's chassis to be detected. A warning message is displayed during POST, to let the user know that the system chassis has been opened. This tamper switch is connected to the tamper detect input on connector J14; see page 104 for details.
Secured Chassis	Choose **Enabled** if you want to prevent the system booting fully after tampering has been detected. This ensures the user investigates the intrusion before booting up. In such circumstances, the board will not boot completely until the user enters setup (by pressing **F2** when prompted) and sets *Reset chassis intrusion* to **Yes**. If you've set a supervisor password (as recommended), this must be entered and *Secured Chassis* set to **Disabled** before the system can be booted.
Reset chassis intrusion	Choose **Yes** to reset the *Chassis Intrusion* circuitry the next time you boot up the computer. You may be forced to do this if tampering has been detected, as described for *Secured Chassis*, above.

Power menu

The *Power* menu is used to control power management. For example, you can specify how long the system must be idle before it goes into standby mode to conserve power. Power management reduces the amount of energy used after periods of inactivity:



The following table explains the settings you can choose:

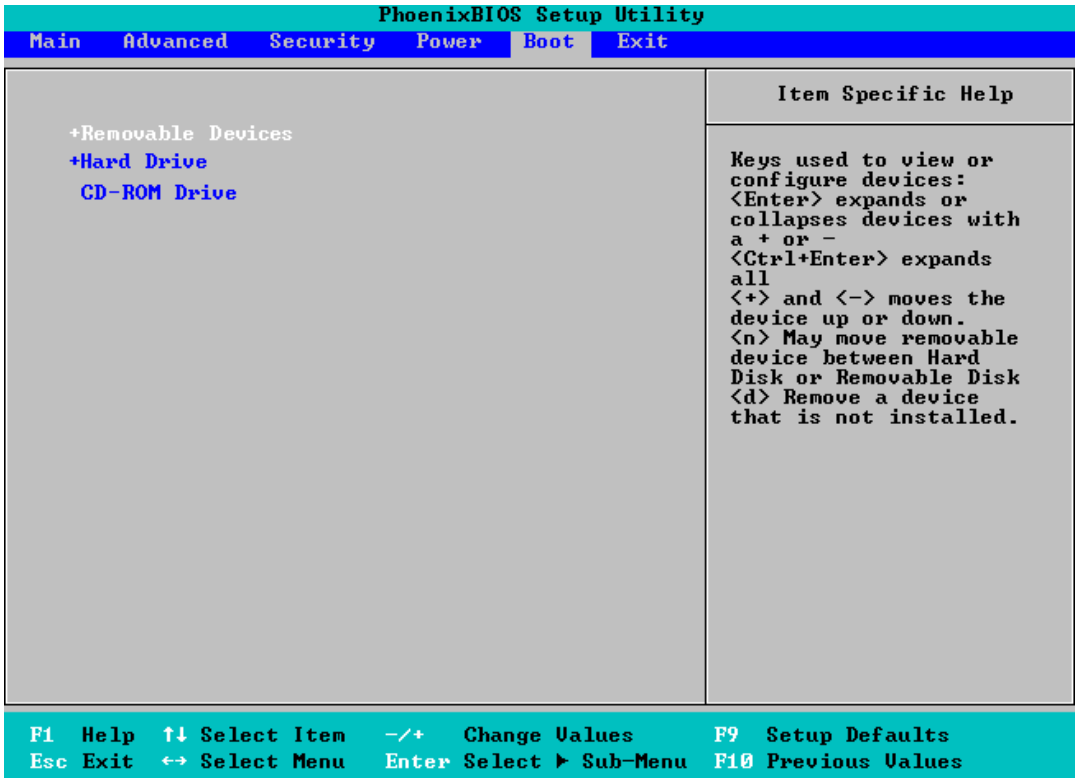
Field	Explanation
Power Savings	Used to specify your power management requirements. The options available are : • Disabled. All power management is disabled. • Customized. You are going to configure your own power management settings (see below). • Maximum Power Savings. Pre-defined timer values are used such that all timers are at low values, i.e. power saving starts after a short period of time. • Maximum Performance. Pre-defined timer values are used such that all timers are at high values, i.e. power saving starts after a longer period of time.
Resume On Time, Resume Time	Specify whether you want the system to wake up at a pre-determined time. If you choose **On**, specify the time the system is to wake up.

Field	Explanation
Power Button Function	Choose the function that the computer's power button is to have, as follows: • Power Off. Pressing the power button toggles the system between power on and power off. • Sleep. Pressing the power button toggles the system between sleep (power saving) mode and wake mode. These power management settings are useful if no APM/ACPI OS is present, for example under DOS. In an ACPI OS (such as Windows XP and some versions of Linux) your selection here has no effect and this behaviour must be configured from the OS itself. For your selection here to have an effect, the *Power Savings* must be set to an option other than **Disabled**.
Suspend Mode	Choose the type of suspend mode. You can choose: • Save To Disk. The system will save its state to disk and power off. • Suspend. The system will save its state but remain in a low power mode.
Power-on by keyboard	Specify whether the power button on the keyboard is to be **Enabled** or **Disabled**.
After Power Failure	Choose what you want to happen if AC power fails. You can choose: • Stay Off to leave the power turned off until the power button is pressed. • Last State to return the system to the power state it was in before the failure. • Power On to restart the computer automatically when power is restored. To allow the APOLLO board to boot automatically when AC power is applied, the **Power On** setting should be selected.

Boot menu

The *Boot* menu is used to specify the order of devices from which the computer attempts to load the operating system when it is switched on.

To specify a device as a boot device, an operating system must be available on the device.



The types of devices in your system are listed. The order in which they are shown is the order in which the computer will attempt to load the operating system. In the example shown, it will start by attempting to load the operating system from the first removable device.

If there are multiple devices of a particular type, '**+**' is shown next to the device type. This indicates that you can expand that device type and view a list of the devices of this type that are available. To do this, use the ↑ and ↓ keys to highlight the device type, and then press **Enter**. You can use the **Enter** key to toggle between showing and hiding the list of devices of this type.

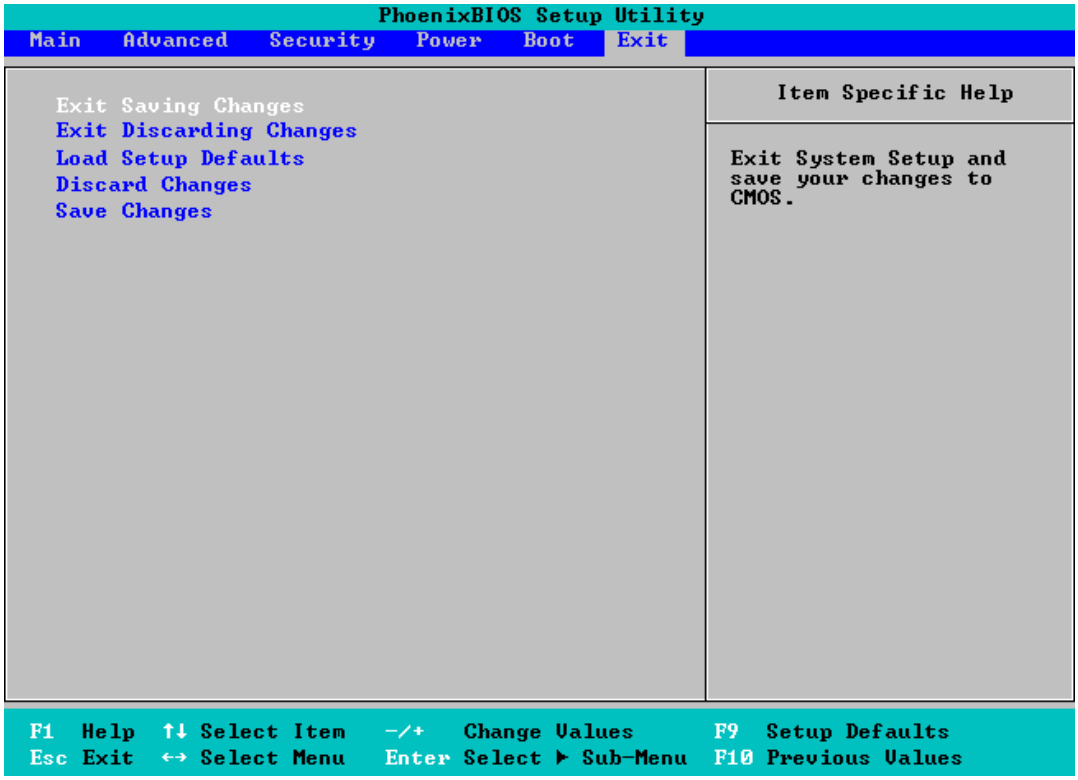
You can change the order of devices from which the computer tries to load the operating system. To move a device in the order, highlight the device and press either **+** (to move it up the order, so the computer tries to load the operating system from it sooner) or **–** (to move it down the order).

The following keys are available while working with the *Boot* menu:

Key	Explanation
Enter	Expands a device type for which there are multiple devices (indicated by '+') to show a list of the devices of this type. Collapses a list of devices of a particular type (indicated by '-').
Ctrl-**Enter**	Expands all device types for which there are multiple devices (indicated by '+'), to show lists of devices of each type.
+ or **-**	Moves a device up or down the list, and thus up or down in the order of devices from which the computer attempts to load the operating system.
n	Changes the device type of a device that acts as both a hard disk drive and a floppy, such as a USB drive. For example, if you select such a device in the **Hard Drive** list and press **n**, it moves to the **Removable Devices** list (and vice versa). This feature only works with devices that support both modes of operation. Typically this support is found with USB/ATAPI adapters, Zip drives and some CompactFlash® microdrives.

Exit menu

The *Exit* menu provides options for saving changes, discarding changes and exiting the PhoenixBIOS setup program:



The following options are available:

Field	Explanation
Exit Saving Changes	Saves any changes you have made, and exits the PhoenixBIOS setup program.
Exit Discarding Changes	Exits the PhoenixBIOS setup program without saving any of the changes made in the current session.
Load Setup Defaults	Reverts to the original factory-assigned BIOS settings. These are the most stable values for the system. Use them if the system is performing erratically due to hardware problems.
Discard Changes	Discards any changes made in the current session. You remain in the PhoenixBIOS setup program.
Save Changes	Saves any changes you have made so far. You remain in the PhoenixBIOS setup program.

Operating system drivers

The APOLLO has been tested with the following operating systems:

- Microsoft Windows XP.
- Microsoft Windows XP Embedded.
- Microsoft Windows 2000.
- Microsoft Windows NT4 Workstation.
- Fedora 8.

Please note:

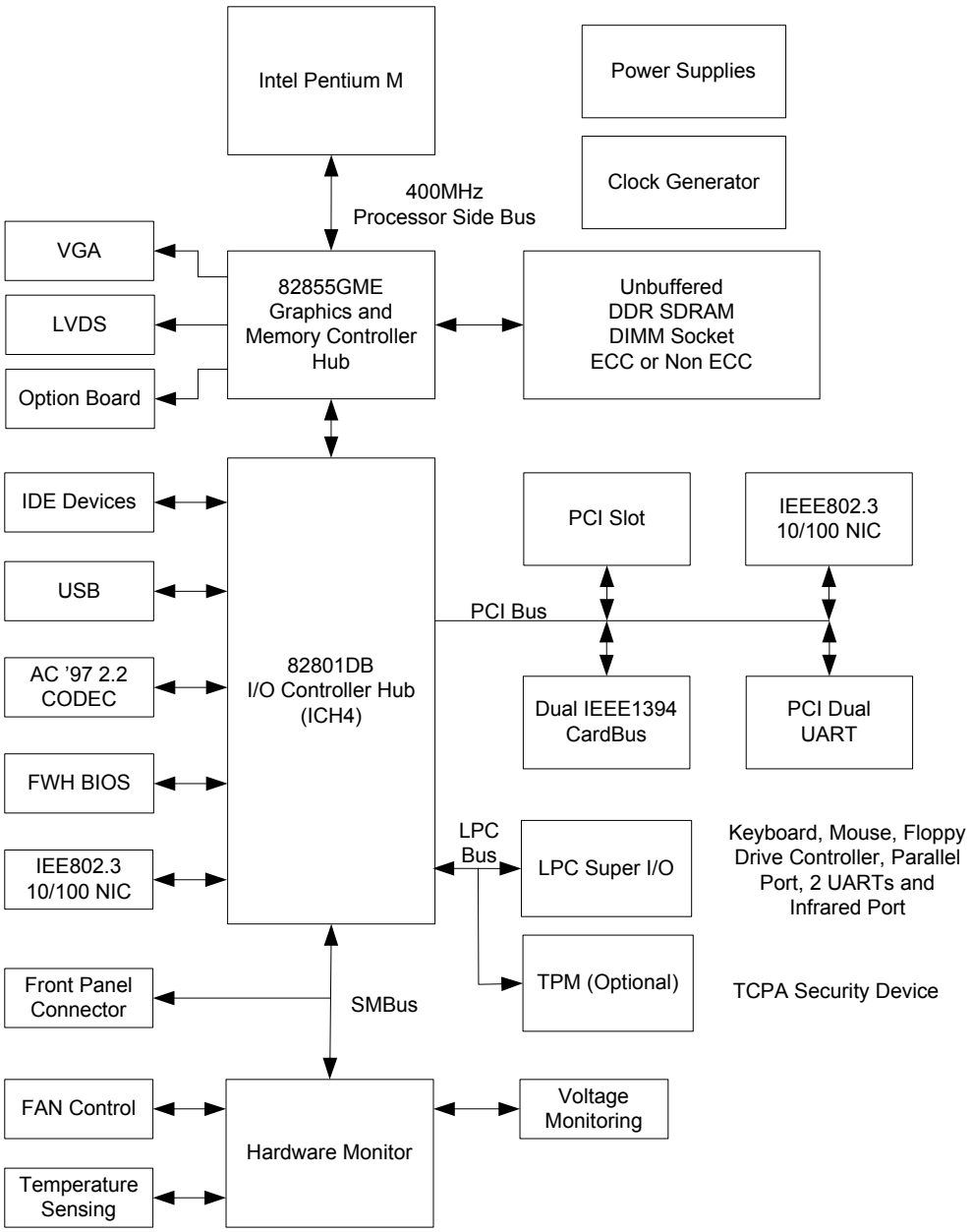
- Eurotech provides a Windows XP Embedded development kit which can be booted from a compact flash card or from a USB flash drive on the APOLLO V2Ix board. Please contact the Eurotech sales team for further information (see Eurotech Group Worldwide Presence, page 144).
- The PCI UART is currently unsupported under Windows NT4.
- Eurotech provide a Linux Fedora 8 development kit that can be booted from a USB flash disk. Contact Eurotech Sales for further details.
- ACPI suspend/resume is not supported under Fedora 8.
- CF boot is currently unsupported under Fedora 8, boot is via a USB device.

Detailed hardware description

This section provides a detailed description of the functions provided by the APOLLO. This information may be required during development, once you have started adding extra peripherals or are starting to use some of the embedded features.

APOLLO block diagram

The diagram below illustrates the functional organization of the APOLLO:



Processor

The standard and Gigabit APOLLO board variants support the Intel Pentium M and Celeron M processors that utilize socketable micro Flip-Chip Pin Grid Array (micro FCPGA) package technology. The Micro-FCPGA package is inserted into a 479-hole, surface-mount, zero insertion force (ZIF) socket, which is referred to as the mPGA479M socket.

The Intel processors currently supported by the Intel Embedded Architecture, and hence with embedded life cycle, are listed in the following table.

Product number	Core speed (GHz)	L2 cache	External bus speed (MHz)	Thermal Design Power (max)	VID	T_j	Device
RH80536GC0332M	1.8	2M	400	21.0W	1.276V	100°C	Pentium® M
RH80535GC0251M	1.6	1M	400	24.5W	1.484V	100°C	Pentium® M
RH80536NC0211M	1.5	1M	400	21.0W	1.260V	100°C	Celeron® M
RH80535NC013512	1.3	512KB	400	24.5W	1.356V	100°C	Celeron® M

µFC-PGA 478-pin Pentium® M and Celeron® M processors supported by the Intel Embedded Architecture

Other Intel Pentium M processors supporting a 400MHz FSB can also be used, although Intel does not guarantee their long-term availability.

The APOLLO does not support the 533MHz front side bus Pentium M/ Celeron M processors, as these have different voltage requirements which are not supported. Using these processors may result in damage to the APOLLO board and/or the processor.

The APOLLO Celeron M 600MHz board variant utilizes a surface mount micro Flip-Chip Ball Grid Array (micro FCBGA) ultra low voltage (ULV) Celeron M processor. This is fitted during manufacture and cannot be upgraded. Details of this processor are as follows:

Product number	Core speed (MHz)	L2 cache	External bus speed (MHz)	Thermal Design Power (max)	VID	T_j	Device
RJ80535VC600512	600	512KB	400	7.0W	1.004V	100°C	Celeron® M

µFC-BGA ULV Celeron® M processors utilized by APOLLO Celeron M 600MHz board variant

Several other micro FCBGA processor options are available and can be fitted based on volume orders. Please contact the Eurotech sales team for further information (see Eurotech Group Worldwide Presence, page 144).

APOLLO chipset

The APOLLO chipset is based on the Intel 82855GME graphics and memory controller hub and 82801DB IO controller hub components. These are a derivative of the Intel Centrino chipset that Intel have provided with additional life cycle support for use in embedded applications.

Graphics and Memory Controller Hub (82855GME)

The 82855GME or Graphics and Memory Controller Hub (GMCH) contains four main components:

- A host interface to the Pentium M/Celeron M processor.
- A system memory interface to DDR SDRAM.
- A hub interface to the IO controller hub (ICH4).
- Integrated Graphics Device.

The GMCH supports a single Pentium M or Celeron M processor with a front side bus (FSB) frequency of 400MHz. See the Processor section on the previous page for details of processor options.

Memory interface

The memory interface on the APOLLO board provides support for one ECC or non-ECC DDR (Double Data Rate) SDRAM 184-pin 2.5V unbuffered dual inline memory module (DIMM). Speeds PC1600 (200MHz), PC2100 (266MHz) and PC2700 (333MHz) are supported. The BIOS automatically reads the parameters of the inserted memory module via its SPD (Serial Presence Device) and configures the memory interface accordingly. No user interaction is required.

The memory controller logic supports aggressive Dynamic Row Power Down features to help reduce power and supports Address and Control line Tri-stating when DDR SDRAM is in an active power down or in self refresh state.

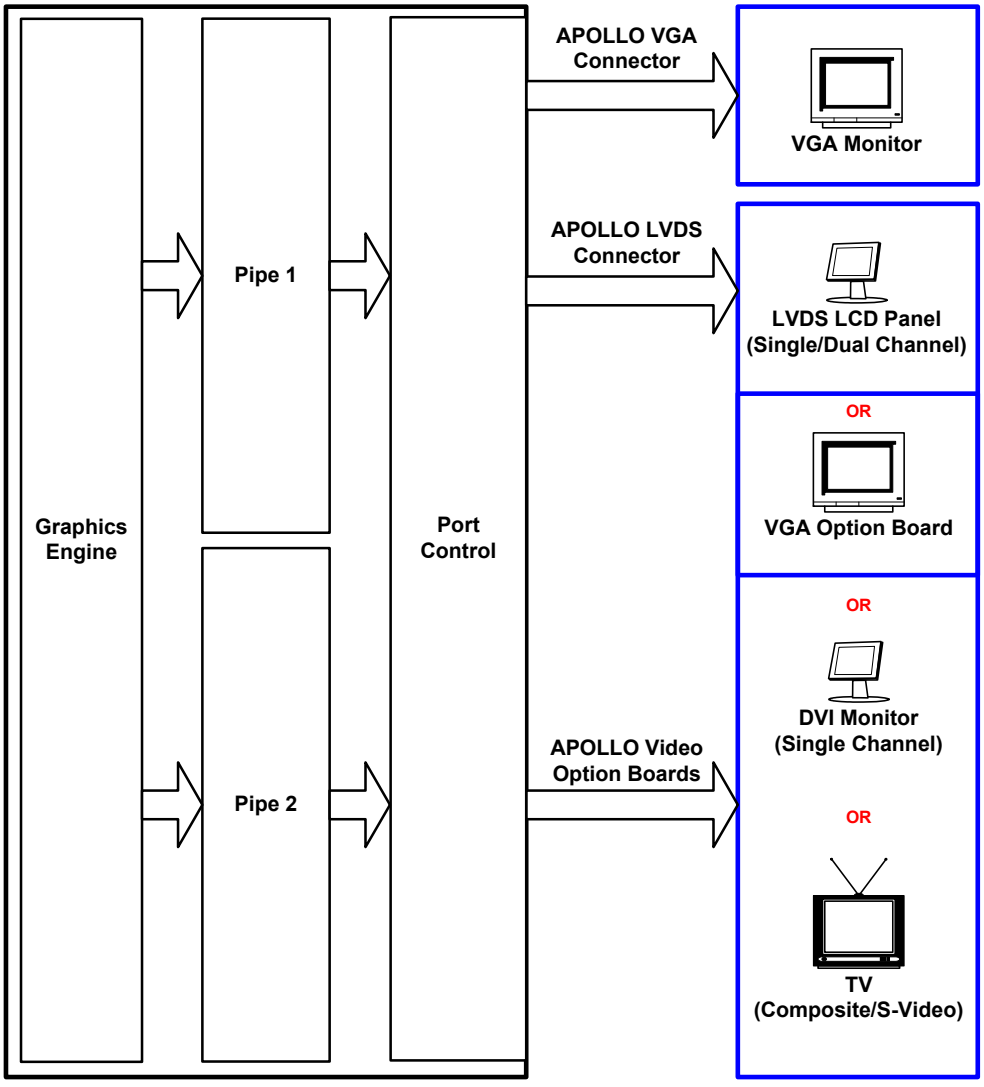
Integrated graphics device

The GMCH contains an integrated Intel Extreme graphics 2 video engine that provides a wide range of display capabilities:

- Integrated graphics accelerator for 3D and 2D graphics.
- Dual independent pipe supporting multiple display modes.
- Dedicated MPEG2 decode engine.
- High bandwidth memory interface.

- Three display output ports. These are:
  - Analogue display interface supporting an analogue CRT. This port uses an integrated 350MHz RAMDAC that can directly drive a standard progressive scan analogue monitor up to a resolution of 2048x1536 pixels at a 75Hz refresh rate.
  - LVDS port. This will directly interface to most LVDS LCD panels and support resolutions up to UXGA (1600x1200).
  - J16 board interface. This provides the capability to interface to a variety of Eurotech display option boards that have a TMDS/DVI, analogue CRT display interface, or a TV display interface via S-Video or composite video outputs.

The three output ports are selectively driven by two independent pipes, allowing for a variety of display options, including dual monitor support with independent video.



Display modes

The three display output ports can be configured in a number of display modes, to allow for independent display timings and extended desktop/multi-monitor operating modes.

The following table shows the display configurations supported by the APOLLO chipset:

Display configuration mode	Description
Single	Normal desktop configuration, single monitor
Twin	Two displays, same content, single resolution
Clone	Two displays, same content, independent timings
Extended	Two displays, different content, independent resolutions

Display interfaces

The APOLLO board supports a range of display interfaces. Details of these are provided below.

Analogue RGB

A standard progressive scan analogue CRT interface is provided from the GMCH. This is interfaced to a high density DB15 VGA connector mounted on the board. A 350MHz RAMDAC provides support for resolutions up to 2048x1536 at 75Hz refresh rate. For connector details, see page 36.

LVDS

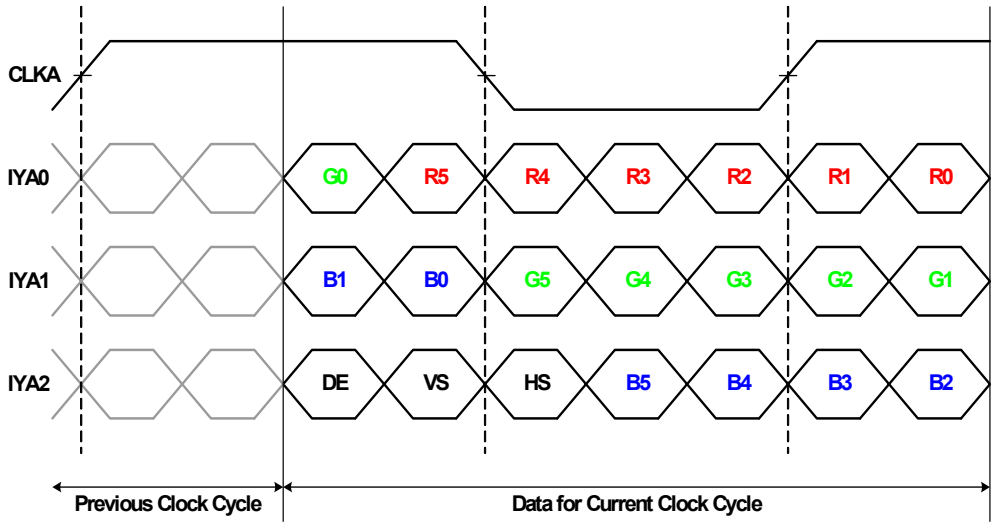
The GMCH has in-built dual channel ANSI/TIA/EIA –644-1995 compliant LVDS drivers. These allow for the direct connection of LVDS LCD panels to the APOLLO board. A high-speed surface mount connector interfaces these signals to an external cable. Spread spectrum clocking is also available to reduce EMI. See Video (Intel IGD) control settings, page 76, for further information. For connector details, see page 44.

The 3.3V power provided on the LVDS connector (J17) is switched through an onboard MOSFET controlled by the video BIOS. This ensures that power is correctly sequenced to the LCD panel. The maximum current that can be supplied by the onboard switch is 1.5A, which is generally sufficient for most LCD displays. In cases where additional current is required, the switched 3.3V power should be used to switch an external power source.

When configuring an LVDS display, the native resolution should be selected in the BIOS to ensure the correct timing set is used for the display. See Video (Intel IGD) control settings, page 76.

Colour mapping

The colour mapping of the APOLLO LVDS LCD interface is compatible with the VESA industry standard colour mapping for LCD displays. The figure below and the table that follows show the configuration for the colour bits in a three channel 6-bit/pixel LVDS bit stream, and the relationship to its clock:



APOLLO LVDS	Common LVDS LCD signal names
IYA0-	RxIN0-, Rin0-, D0-, Link 0-, IN0-
IYA0+	RxIN0+, Rin0+, D0+, Link 0+, IN0+
IYA1-	RxIN1-, Rin1-, D1-, Link 1-, IN1-
IYA1+	RxIN1+, Rin1+, D1+, Link 1+, IN1+
IYA2-	RxIN2-, Rin2-, D2-, Link 2-, IN2-
IYA2+	RxIN2+, Rin2+, D2+, Link 2+, IN2+
ICLKA-	CKIN-, ClkIN-, CK-, Clock-, CLK-
ICLKA+	CKIN+, ClkIN+, CK+, Clock+, CLK+

Dual channel operation

The APOLLO LVDS display interface connector supports dual channel LVDS displays. Commonly these displays have a screen resolution greater than 1024x768. The secondary LVDS display channel on the APOLLO board occupies the remaining connections on the LVDS connector J17.

The secondary channel is designated with a ‘B’. It maps to the LCD display in a similar manner to the primary channel.

LVDS data cable

When interfacing to an LVDS display, the data signals IYA+/-, IYB+/-, ICLKA, ICLKB require a twisted pair cable with a nominal impedance of 100Ω to prevent signal reflections due to impedance discontinuities. For connections over long distances, a ground connection should be used for each LVDS data pair.

LCD backlight connector

A backlight connector (J15) interfaces to and can be configured to control an external CCFL backlight inverter. The header provides +12V, +5V, a backlight enable control line and a software-controllable PWM interface.

The backlight enable signal (Backlight En) pin 5 on connector J15 provides a 3.3V output control signal that is designed to be interfaced to the ON/OFF input common on most backlight inverters. This is an active high signal with a 100K pull down resistor. It is sequenced by the video BIOS to enable the backlight when the display is active.

The backlight control signal (Backlight Control) pin 4 on connector J15 provides a 3.3V PWM output control signal that has been designed to interface to the intensity control input available on most backlight inverters. Buffering may be required for some backlight inverters if the 3.3V PWM signal does not provide the required output range.

The PWM frequency is fixed in the Video BIOS to 200Hz. The duty cycle has been set to predetermined values that can be accessed using the ACPI _BCL control method supported under Windows XP and Linux. When interfaced correctly, this signal allows software control of the backlight intensity.

For connector details, see page 42.

Windows XP/XP Embedded Video Drivers

Two drivers are available for Windows XP and XP Embedded: the Intel Mobile Graphics division Extreme Graphics driver and the Intel Embedded Graphics Driver (IEGD).

Intel Mobile Graphics Division XP Driver – Extreme Graphics

The Intel Extreme Graphics XP driver is a fully featured driver however as it is designed for use primarily with laptop computers some of its features are not fully compatible with Embedded PC design. One aspect of this is if a VGA monitor is not attached when the graphics driver loads then the LVDS display will be selected as the primary display output. This is the expected behaviour for a laptop PC, the LVDS display selection will remain until the VGA display port is selected through the display configuration or using the CTRL-ALT-F1 hotkey combination. These options will only be available if a Windows password login is bypassed. If a login console is to be used the Intel Embedded Graphics Driver is recommended.

Intel Embedded Graphics Driver – IEGD Graphics

The Intel Embedded Graphics Driver (IEGD) driver is a user customisable driver that can be used to support unique display configurations and capabilities not natively supported by the mobile division driver. This allows for features such as forcing the VGA output ON regardless of there being an attached display. IEGD Version 8.0 supports the Intel 855GME chipset used on the APOLLO board. Further information on the IEGD configuration tools are available at www.intel.com/go/iegd.

A preconfigured IEGD VGA output only driver is also available from Eurotech support, please refer to the contact details on page 144.

Video option boards

Two DVO ports capable of driving a variety of DVO devices (e.g. DVI, LVDS and TV out) are provided on a high speed board-to-board connector that allows for interfacing to optional display boards.

Option boards for the connection of DVO devices are available from Eurotech. The option boards connect to the APOLLO using high-speed board-to-board connections. The option boards are available for DVI, TV out and a secondary VGA output. Further details on each of these option boards are provided below. Currently an LVDS option board is not available.

All option boards also break out the APOLLO's additional USB5 and USB6 ports on a standard USB connection as used on the APOLLO board USB connector J18.

Option board 1: DVI

A Silicon Image Sil1162 directly interfaces to the DVO port to provide a single link TMDS output channel that is link DVI 1.0 compliant. This provides support for LCD displays up to 1600x1200. Refer to Appendix E – DVI Video Option Board on page 136 for further details.

Option board 2: TV out

A Focus Enhancements FS453 video encoder converts the DVO port digital display output to a RGB, S-Video or composite TV output signal to provide broadcast-quality video output.

The FS453 takes in high-resolution computer graphics input (VGA through SXGA) and produces SDTV (Standard Definition Television) or HDTV (High Definition Television) analogue output. In SDTV mode it converts, scales, removes flicker, interlaces and encodes the data into NTSC or PAL formats. In HDTV mode, it performs colour space conversions and then inserts the required syncs for output.

Resolutions up to 1024x768 can be encoded for display on a TV. Refer to Appendix F – TV out video option board on page 138 for pinout details.

Option board 3: Secondary VGA CRT

An option board has been developed which allows for a secondary VGA monitor to be interfaced to the APOLLO. The VGA output is derived from the APOLLO LVDS connection. It provides the capability to support the various 'two display' operating modes. When the secondary VGA output is utilized, the LVDS LCD interface cannot be used for interfacing to LVDS LCD panels.

The maximum resolution supported by the VGA CRT board is 1280x1024 at a 60Hz refresh rate. Standard resolutions supported are 800x600, 1024x768 and 1280x1024. Windows XP driver support is provided using the Intel Embedded driver; Linux driver support is limited to Intel support Linux builds. Refer to Appendix G – VGA option board on page 140 for further details.

ICH4 (IO controller hub)

The IO controller hub contains the primary PCI interface, LPC interface, USB 2.0, ATA-100, AC'97, Ethernet controller and other I/O functions. It communicates with the GMCH over an interconnect bus known as the hub interface. The ICH4 supports the following functions:

- ACPI Power Management Logic Support.
- Enhanced DMA controller, Interrupt controller and timer functions.
- Integrated IDE controller supports Ultra ATA100/66/33 and PIO.
- USB host interface with support for six USB ports, one UHCI host controllers and one EHCI high-speed host controller.
- Integrated 10/100 Ethernet controller.
- System Management Bus (SMBus) Specification, version 2.0 with additional support for I2C devices.
- AC '97 codec interface.
- Low Pin Count (LPC) and firmware hub (FWH) interface support.
- Tamper detection input.

Interrupt controller

The ICH4 incorporates the functionality of two 8259-interrupt controllers that provide system interrupts for the ISA compatible interrupts. These interrupts are: system timer, keyboard controller, serial ports, parallel ports, floppy disk, IDE, mouse and DMA channels. In addition, this interrupt controller can support the PCI based interrupts, by mapping the PCI interrupt onto the compatible ISA interrupt line. Each 8259 core supports eight interrupts, numbered 0–7.

The ICH4 also supports the advanced programmable interrupt controller (APIC) that provides for up to 24 interrupts. This interrupt scheme can be enabled in the BIOS ACPI setup screen; see ACPI control settings, page 78, for details. See page 125 for further information about APIC.

The BIOS configures the interrupt routing at boot time. ISA interrupts can be reserved in the BIOS for legacy ISA devices that require this. See PCI/PNP ISA IRQ resource exclusion settings, page 72, for further details.

If you install an operating system using non IO APIC mode of operation, and then subsequently change to APIC mode, the operating system may not boot correctly.

Firmware hub

The firmware hub provides non-volatile storage for the APOLLO PhoenixBIOS and general-purpose inputs that are configured as user jumpers. The firmware hub is accessed via the ICH4 low pin count (LPC) bus.

For additional information about the APOLLO BIOS see PhoenixBIOS features and setup, page 51. For user jumper details see Jumpers and connectors, page 22.

CMOS backup EEPROM

The APOLLO provides an onboard EEPROM that is used to store the CMOS settings. This allows the APOLLO board to be run without a battery and also provides protection from CMOS corruption. If the CMOS values are found to be corrupt then they are automatically restored from the EEPROM at boot time.

As changes to the BIOS settings can result in the APOLLO board not booting correctly, and clearing the CMOS has no effect, an additional jumper is used to restore the BIOS settings from the firmware hub component, bypassing the backup EEPROM. User jumper 1 (USR1 on JP2) is used for this purpose on the APOLLO V1Ix boards and a dedicated EE jumper (EE on JP2) is provided on the APOLLO V2Ix board. Refer to the JP2 jumper settings on page 54 for further details.

To prevent the BIOS settings from being over written, the USR1 jumper should only be used in an application that does not include a reboot cycle.

PCI local bus

The ICH4 provides a 32bit, 33MHz PCI interface for use with onboard PCI devices and PCI expansion cards. The table below shows the devices connected to the bus and their corresponding vendor/device ID's, IRQs and grant/request connections where appropriate.

PCI device	Device	Vendor ID	Device ID	PIRQ	GNT/RQT	See note...
2	82551QM 10/100 Ethernet controller; 82541PI 10/100/1000 Ethernet controller.	8086h 8086h	1229h 1076h	G G	2 2	1
7	Exar XR17D152 Dual PCI UART.	13A8h	0152h	A	N/A	
8	82562ET 10/100 Ethernet controller.	8086h	1039h	E	N/A	
9	PC and Cardbus controller; PCI4510A function 0; IEEE1394 Firewire controller; PCI4510A function 1.	104Ch 104Ch	AC44h 8029h	D C	0 0	2
11	PCI Slot 0 (primary)	N/A	N/A	E, F, G, H	1	3
13	PCI Slot 1 (secondary)	N/A	N/A	F, G, H, E	3	3
15	PCI Slot 2 (tertiary)	N/A	N/A	G, H, E, F	4	3

Notes on table

1 The APOLLO V1Ix board has a Gigabit (82541PI) variant and two 10/100 Ethernet controller (82551QM) variants: standard and 600MHz Celeron M. The APOLLO V2Ix board offers just the 82541PI Gigabit Ethernet controller.

2 The PCI4510A is a dual-function device: two functional devices in one physical package.

3 The APOLLO routes two additional PCI grant/request lines to the single PCI slot to allow for up to three PCI devices to be accessed when using a PCI riser. It is strongly recommended to use a zero delay clock buffer to buffer the 33MHz PCI clock to any additional PCI devices. For connector details see page 40. Routing of the GNT4 signal to the PCI slot 2 is controlled via JP1; see page 25.

PCI Expansion connector

The APOLLO provides a single 33MHz 32bit 5V PCI bus expansion connector. All PCI signals are 5V tolerant. The PCI expansion connector includes PCI auxiliary power for devices requiring power during ACPI standby (S3) and soft off (S5) modes. The PCI PME# power management signal is also provided for device wakeup.

Dual Slot PCI riser

A dual slot 1U height PCI riser card has been designed to interface to the APOLLO board. This is used to provide additional PCI slots to support up to two bus master PCI expansion cards.

Ethernet controllers

The APOLLO provides two Ethernet controllers. The table below summarizes the controller type and supported network speeds based on APOLLO variant used.

APOLLO variant	Primary Ethernet controller	Secondary Ethernet controller
Standard (V1Ix)	10/100 BaseT 82551QM Ethernet Controller	10/100 BaseT ICH4 + 82562ET Ethernet Controller
Gigabit (V1Ix) and V2Ix APOLLO	10/100/1000 BaseT 82541PI Ethernet Controller	

Primary network interface

A primary network interface controller based on the Intel 82551QM 10/100Mb Fast Ethernet PCI Controller is provided. The 82551QM provides efficient scatter-gather bus mastering capabilities enabling the 82551QM to perform high-speed data transfers over the PCI bus. This capability accelerates the processing of high level commands and operations, which lowers CPU utilization. Its architecture enables data to flow efficiently from the bus interface unit to the 3KB Transmit and Receive FIFOs, providing the perfect balance between the wire and system bus. In addition, multiple priority queues are provided to prevent data underruns and overruns. For connector details, see page 35.

Optional Gigabit Ethernet (APOLLO V1Ix)

An Intel 82541PI Gigabit Ethernet controller is provided on the APOLLO Gigabit build variant. This replaces the 82551QM device used on the APOLLO Standard and Celeron M 600MHz variants.

The 82541PI provides performance up to 1000 BaseT, with backwards compatibility with 100BaseTX and 10BaseT Ethernet standards.

APOLLO V2Ix Ethernet

The APOLLO V2Ix boards are fitted with an 82541PI Gigabit Ethernet connection as standard; the 82541PI provides performance up to 1000 BaseT, with backwards compatibility with 100BaseTX and 10BaseT Ethernet standards. The APOLLO V2Ix board has the capability to enable/disable the primary Ethernet port.

Secondary network interface

The IO Controller hub contains an Ethernet controller. An external physical layer component provides the media interface to support 10/100 MB/s Ethernet. The Ethernet controller supports:

- Wake On LAN (WOL).
- Deep power down mode.
- Network boot.

For connector details, see page 35.

The APOLLO V2Ix board has the capability to enable/disable the secondary Ethernet port.

Two LEDs on each RJ-45 port provide information about its operation, as follows:

- The LED on the left (as you look at the connector) tells you about the speed the port is currently operating at.
- The LED on the right (as you look at the connector) tells you whether the connector is currently linked to the network, and indicates when activity takes place via that link, i.e. when data is passing through.

The information provided by each LED is explained in the following table:

Ethernet port	Left LED (speed)	Right LED (link/activity)
10/100	Green: 100Mb/s Off: 10Mb/s	Yellow: Link connected Flashes: Activity is taking place
10/100/1000	Orange: 1000Mb/s Green: 100Mb/s Off: 10Mb/s	Yellow: Link connected Flashes: Activity is taking place

Network boot

The Primary and Secondary Ethernet controllers both provide support for Preboot Execution Environment (PXE) that allows for such features as remote booting and loading of an operating system over a network. This support is provided using the Intel Boot Agent Option ROMs and is configured via the BIOS setup screens – see Boot menu, page 86, for further information.

Ethernet cables

To provide the best immunity to external interference a shielded twisted pair cable is recommended for use with the APOLLO board. For Gigabit Ethernet this should be rated as a CAT5E or higher cable.

IDE interface

The APOLLO provides a single IDE channel capable of Ultra ATA 100 operation. This is listed as the primary IDE interface in the BIOS. The primary IDE interface can support several types of data transfers:

- Programmed I/O (PIO): Processor is in control of the data transfer.
- 8237 style DMA: DMA protocol that resembles the DMA on the ISA bus, although it does not use the 8237 in the ICH4. This protocol off loads the processor from moving data. This allows higher transfer rate of up to 16MB/s.
- Ultra ATA/33: DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 33MB/s.
- Ultra ATA/66: DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 66MB/s.
- Ultra ATA/100: DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 100MB/s.

The primary IDE interface is made available to the user through a 2.54mm (0.1") pitch pin header. For connector details, see page 48.

To improve signal integrity an 80-way IDE cable with 40-way connectors should be used with devices supporting Ultra ATA/66 and above.

USB host controller

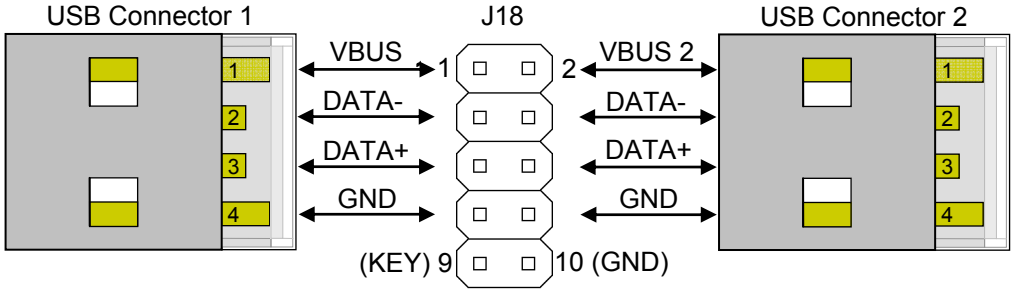
The USB host controller on the ICH4 provides support for six USB 2.0 compliant ports. USB 2.0 allows for a maximum data rate of 480Mbps and is downwardly compatible with the USB 1.1 specification. EHCI (version 2.0) and UHCI (version 1.1) are both supported by the USB ports.

A power switching circuit provides over current feedback to the system and current limiting to 500mA per channel.

There are four signal lines associated with USB channels:

- VBUS
- DATA-
- DATA+
- GND

Their arrangement is summarized in the following illustration:



For connector details, see page 34.

For details about the USB bus, or to determine whether particular peripherals are available, please go to www.usb.org.

A USB power switch provides power to the USB ports during normal operation and also during standby (S3) and soft off (S5).

A USB power control switch is used to control the power and protect against short circuit conditions. This can be enabled/disabled by the processor and the USB function needs to be enabled in the BIOS to ensure that power is supplied to each device. The USB function is controlled using the I/O Device Configuration screen within the setup utility - see page 62 for details.

If the USB voltage is short circuited or more than 500mA is drawn from either supply the switch turns off the power supply and automatically protects the device and board. The VBUS signal is derived from the ATX +5V supply via the APOLLO.

Real Time Clock

The Real Time Clock (RTC) module provides a battery backed-up date and time-keeping device. It has two banks of static RAM with 128 bytes each (although the first bank has 114 bytes for general purpose usage). Three interrupt features are available:

- Time of day alarm with once a second to once a month range.
- Periodic rates of 122µs to 500ms.
- End of update cycle notification.

Seconds, minutes, hours, days, day of week, month and year are counted. Daylight savings compensation is optional. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is functionally compatible with the Motorola MC146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second.

Tamper detection

A tamper detection input is included within the real time clock circuitry on the ICH4 that operates in all power modes. The status of the tamper detection bit is battery backed in static RAM. To use the tamper detection, a normally open switch should be used; a tamper is detected when the switch contacts close.

The *BIOS Security setup* screen (see page 81) provides two options for enabling a case open warning. It also provides a secure chassis mode that requires the supervisor password to be entered and the chassis intrusion detection to be disabled before the board will boot to an operating system. Both options are disabled by default.

Watchdog timer

The APOLLO provides a Maxim MAX6369KA watchdog timer with a pin-selectable timeout of 1ms to 60 seconds. This can be used to generate a complete hardware system reset when an error causes a system lockup. By default, the watchdog timer is disabled and once enabled must be triggered within the timeout period specified. The table below lists the ICH4 GPIO connections relating to the watchdog timer, these ports are configured as outputs by the BIOS during boot and are active during standby (S3). The watchdog output has an open drain connection to the system reset line.

The ICH4 GPIO registers are accessed via an IO location mapped through the ICH4 LPC interface bridge (Bus: 00h, Device: 1Fh, Function: 00h). Please refer to the Intel 82801DB ICH4 datasheet for additional information on the ICH4 GPIO and to the Maxim MAX6369 datasheet for additional information on the watchdog timer settings.

ICH4 GPIO	Default Level	MAX6369KA
GPIO25	High	SET0
GPIO27	High	SET1
GPIO28	Low	SET2
GPIO24	Low	WDI

System control interface

A system control interface connector, J14, is provided to interface to standard input switches and status indicators for:

- *System reset switch.*
  A connection for a momentary on reset switch. This provides standard PC reset functionality.

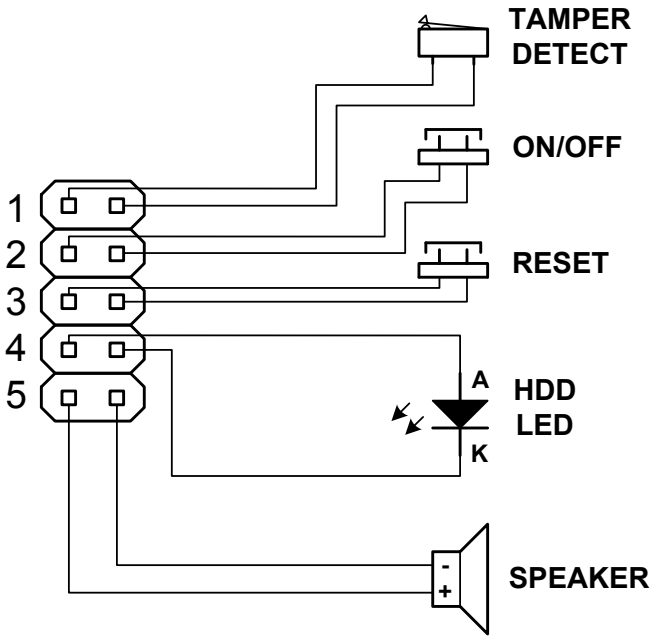
- *Power button (on/off switch).*
  A connection for a momentary on ACPI power button. This provides standard PC on/off functionality. The on/off switch ACPI functionality is configured in the BIOS power management setup screen (see page 84). Holding the on/off switch on for 5 seconds turns the ATX power supply off.

- *Tamper detection.*
  A connection for a normally open switch. The tamper detection circuitry is included in the RTC circuitry (see the previous page for further details). A tamper is detected when the switch contacts close.

- *PC speaker.*
  A connection to a standard 8Ω speaker to support PC speaker functionality. The PC speaker output is also routed to the AC97 Codec and can be mixed with the audio output.

- *HDD activity.*
  A connection for a hard drive activity LED. This LED shows activity on both the IDE based devices and for the CompactFlash® socket.

The connections made to J14 are shown in the following system control interface diagram. For further connector details, see page 41.



AC'97 audio CODEC

The VIA VT1616 AC'97 audio CODEC provides six channel outputs with 18-bit resolution allowing the part to support 5.1 surround sound specifications. For optimum playback performance, the VIA VT1616 has analogue mixer circuitry that integrates stereo enhancement to provide a 3D surround sound effect for stereo media. Further provisions in the hardware allow for down mixing of 6-channel inputs such as DVDs into 4-channel, or even 2-channel outputs.

The codec audio inputs and outputs are interfaced via three 3.5mm audio jacks. They provide Mic In, Line In and Line Out connections under 2.0 mode and Centre, Rear Left, Rear Right, Front Left and Front right audio connections under 5.1 surround sound mode.

Two pins on J14 provide an interface to an on-board speaker for PC BEEP functionality; refer to the system control interface diagram on the previous page for details.

An input for CD-ROM audio and an output for optical SPDIF (Sony/Philips Digital Interface) is also provided.

For connector details, see page 32.

PCI dual UART

An Exar XR17D152 PCI based dual UART is provided on the APOLLO board, this supports COM3 and COM4. COM3 is configured as a standard RS232 port, whilst COM4 is configured as a software selectable RS232, RS485 or RS422 port.

RS232 interfaces

The RS232 signals associated with COM3 and COM4 are routed to a 20-way 2.54mm (0.1") boxed header J22, which has been designed to provide a direct ribbon cable connection to 9-way D-type plugs. For connector details, see page XX. (Reference connector J22)

RS485/422 interfaces

The COM4 serial interface supports RS232, RS422 and RS485 interfaces.

The RS422 interface provides full duplex communication, in point to point or point to multi-point configurations. The signals available are TXA, TXB, RXA, RXB and Ground. The maximum cable length for an RS422 system is 4000ft and support is provided for up to 10 receivers in a system.

RS485 is a half-duplex interface that provides combined TX and RX signals. The maximum cable length for the RS485 interface is the same as for RS422 (4000ft), but RS485 supports up to 32 transmitters and receivers on a single network. Only one transmitter should be switched on at a time to prevent bus contention.

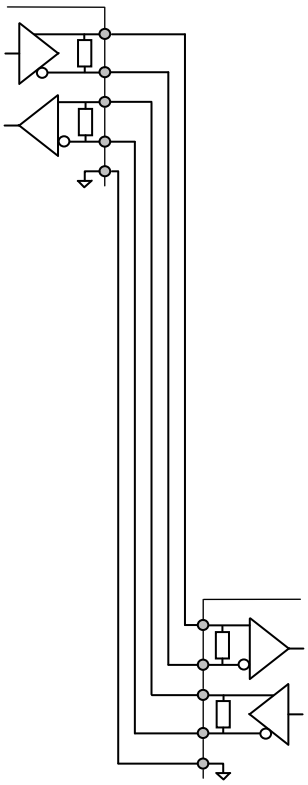
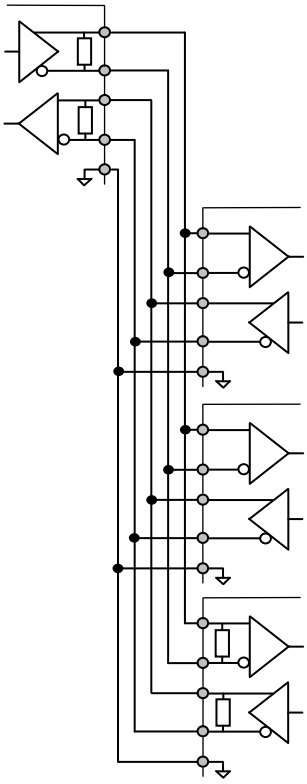
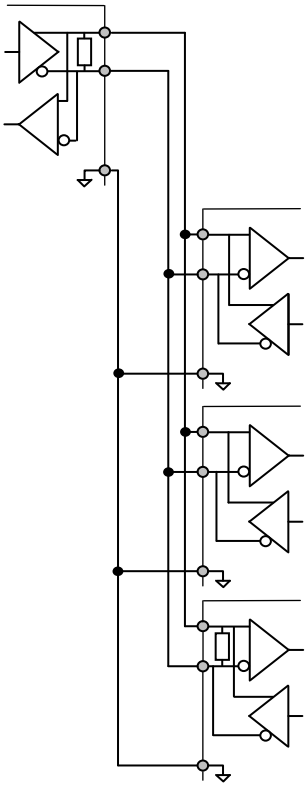
The PCI UART includes circuitry for half duplex flow control also referred to as Auto RTS flow control, eliminating the requirement for software flow control. Auto RTS flow control uses the serial port RTS control signal to enable and disable the RS485/RS422 transmitter. This can be configured in the BIOS (see page 65).

Port	RS232	IrDA	RS422/485	Max Baud Rate
COM3	J22	N/A	N/A	921.6K
COM4	J22	N/A	J25	921.6K

When using connector J25 to interface to RS485 signals only the TXA/TXB signals should be used.

RS485/422 interface configuration

The following table lists the different RS422/RS485 operating modes supported by the APOLLO and the BIOS configurations required to support these operating modes.

RS422 POINT-TO-POINT	RS422 MULTI-DROP	RS485 MULTI-DROP
		
Number of Wires 5 **Transmitters Enabled** always **Receivers Enabled** always **BIOS Mode** RS422 **BIOS Auto Flow Control** Disabled	**Number of Wires** 5 **Transmitters Enabled** active RTS **Receivers Enabled** always **BIOS Mode** RS422 **BIOS Auto Flow Control** Enabled	**Number of Wires** 3 **Transmitters Enabled** active RTS **Receivers Enabled** always **BIOS Mode** RS485 **BIOS Auto Flow Control** Enabled

Termination resistors are often required on the first and last devices of an RS422/RS485 bus. Jumper JP3 is used to enable/disable the RS485/422 termination resistors; see page 28 for details.

Super IO

On the APOLLO V1Ix boards, an SMSC LPC47M292 Super IO controller provides legacy IO support. On the APOLLO V2Ix boards, an SMSC SCH3112 provides the SuperIO support. On both boards the SuperIO resides on the LPC bus and provides:

- Two serial ports.
- Keyboard and mouse PS/2 interface.
- Parallel port.
- Floppy drive.
- IrDA.
- General purpose IO for the front panel connector.

On the APOLLO V1Ix board an additional functional block incorporated into the SuperIO provides an SMBUS based hardware monitor which is used to monitor voltages and temperatures on the board. The APOLLO V2Ix board provides hardware monitor support via an ISA mapped set of indexed registers.

Serial ports

The APOLLO provides four high speed 16C550 compatible UARTs, two via the SuperIO and a further two via a dual PCI based UART. See page 107 for information relating to the PCI UART based serial ports COM3 and COM4.

COM1 and COM2 are interfaced via the SuperIO and can be used as standard RS232 serial interfaces. COM2 is also selectable between RS232 and IrDA operation.

The *Serial Configuration* screen in the BIOS lets you specify the base I/O address and IRQ for COM1 and COM2. See page 64 for details.

The following table shows the hardware configuration for each channel:

Port	RS232 connector	IrDA/ASK-IR connector	RS422/485 connector	Max Baud Rate
COM1	J7B	N/A	N/A	460.8K
COM2	J7C	J26	N/A	460.8K[1]

The maximum baud rate for IrDA is 115.2K and ASK-IR is 57.6K.

COM2 operation

COM2 is selectable between RS232 and two infrared transmission schemes IrDA or Sharp ASK-IR. This is done in the *Serial Configuration* screen in the BIOS (see page 64). When the infrared operating modes are selected, the RS232 transmitter is shutdown. Care should be taken to ensure that the IrDA module is not installed whilst the RS232 transmitter is enabled, as this would cause a conflict between the two devices.

IrDA/ASK-IR

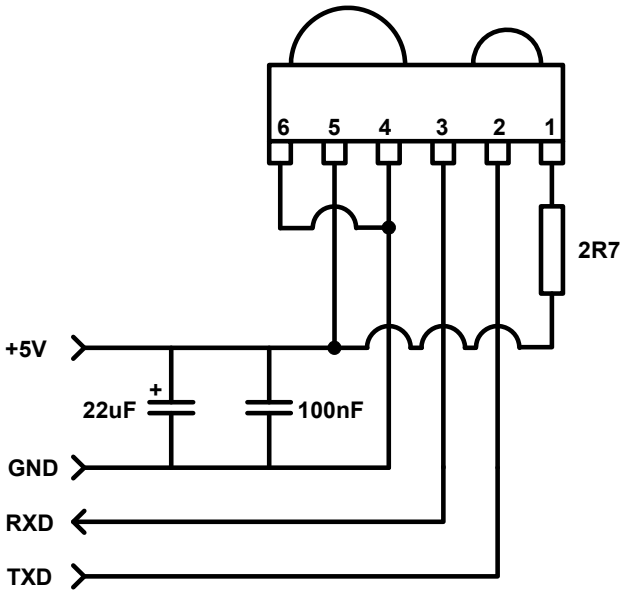
An infrared port is available which supports the following infrared standards:

- Infrared Data Association (IrDA) V1.0 SIR with baud rates to 115.2k/bps.
- SHARP ASK-IR protocol with maximum baud rate up to 57.6k/bps.

For connector details, see page 36.

Enabling the infrared port prevents operation of Serial Port B (COM2). The infrared port should be disconnected before using the COM2 port.

The following diagram shows the connection of the IrDA interface port J26 to a Sharp GP2W0004YP IrDA transceiver module for IrDA 1.0 compliant data transmission.



Parallel port

The APOLLO provides a parallel port that can be used to connect an external printer, tape drive, disk drive, scanner etc., or can provide additional digital I/O capability.

The port is both IBM XT/AT and IEEE1284 compatible. It supports Standard Parallel Port (SPP), Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP) modes and is compliant with the IEEE1284 specification. It also incorporates ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

For connector details, see page 37. Configuration of the parallel port operating mode is performed in the *I/O Device Configuration* menu in the BIOS; see page 62 for details.

Floppy disk controller

The floppy disk controller (FDC) provides the interface between the host processor and the floppy disk drives. It integrates the functions of:

- Formatter/controller.
- Digital data separator.
- Write precompensation.
- Data rate selection logic for an IBM XT/AT compatible FDC.

The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection. The APOLLO allows for an interface to a single slimline floppy drive using a 26-way flat flex cable. For connector details, see page 50.

Hardware monitor

The APOLLO V1Ix board contains an SMBUS hardware monitor (HWM) that provides a combination of voltage and thermal monitoring, a similar HWM is provided on the APOLLO V2Ix board via a set of ISA mapped IO registers.

The table below summarizes the voltages and temperatures

The BIOS provides a *Hardware Monitor screen* (available from the *Advanced* menu in the BIOS – see page 79). This shows system voltages, temperatures and fan speeds in real-time. From this screen the PWM frequency and duty cycle for the CPU and system fans can also be set.

Voltages

System voltage	APOLLO V1Ix	APOLLO V2Ix
CPU Core (0.7V – 1.7V)	✓	✓
+1.05V	✓	✗
+1.35V	✓	✗
+2.5V	✓	✓
+3.3V	✓	✓
+3.3V Standby	✓	✓
+5V	✓	✓
+12V	✓	✓

Temperatures

Component	APOLLO V1Ix	APOLLO V2Ix
CPU	✓	✓
Ambient	✓	✓
SuperIO	✓	✓

Keyboard and mouse controller

The SuperIO contains a universal keyboard controller that is designed for intelligent keyboard management in desktop computer applications. The universal keyboard controller uses an 8042 microcontroller CPU core. Four signal pins are provided which allow for the connection of two external PS/2 devices such as a keyboard and mouse.

The PhoenixBIOS automatically detects the presence of the keyboard and mouse, and provides support for these. For systems requiring it, a BIOS option is available to allow boot without keyboard; see page 58 for details. PS/2 keyboard and mouse connector details are provided on pages 36 and 36.

IEEE1394 ports and CF+ socket

The APOLLO board includes a Texas Instruments PCI5410A, which provides dual IEEE1394a-2000 (Firewire) compliant ports and a single CF+ full IO mode CompactFlash® socket.

CompactFlash® CF+ socket

Function 0 of the PCI4510A device provides a PC Card socket controller, compliant with the latest PC Card standards and compatible with the CompactFlash CF+ host specification. The APOLLO has a single CF+ Type II CompactFlash socket that supports 3.3V and 5V Type I/II CompactFlash cards, providing support for a wide variety of flash, wireless, serial and networking cards. For connector details, see page 46.

When a bootable CompactFlash storage card is installed and the interface is configured to be bootable, the device appears as a bootable device in the BIOS boot menu, allowing the booting of an operating system from CompactFlash memory cards; see page 86 for details. (Booting from CompactFlash network cards is not supported.)

IEE1394 firewire ports

Function 1 of the PCI4510A is an integrated IEEE 1394a-2000 open host controller interface (OHCI) PHY/link-layer controller (LLC). It is capable of transferring data between the 33MHz 32bit PCI bus and the 1394 bus at 100M bits/s, 200M bits/s and 400M bits/s. Two 1394 ports are provided both have separate cable bias (TPBIAS) and both also provide cable power.

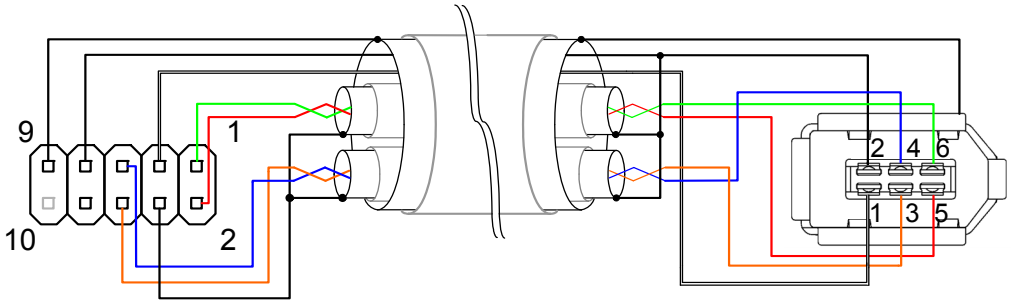
IEEE1394 port 0

Port 0 is configured as a panel mount 6-pin IEEE1394 connector. It provides a fused and diode-protected +12V cable power connection. Cable power is sourced from the 12V rail of the ATX power supply. For connector details, see page 34.

IEEE1394 port 1

Port 1 is configured as a 10-way pin header. It is designed to interface to a cable providing a 6-pin IEEE1394 connector. The pin header connection provides a fused and diode-protected +12V cable power connection. Cable power is sourced from the 12V rail of the ATX power supply.

When connecting to the 10-way pin header, an IEEE1394 compliant cable must be used to ensure signal integrity is maintained.



For connector details, see page 45.

Trusted platform module

On the APOLLO V1Ix board variants, an Atmel AT97SC3201 trusted platform module (TPM) conforming to the Trusted Computing Platform Architecture (TCPA) Rev 1.1 specification is available as a factory build option. Please contact the Eurotech sales team for further information (see page 144) for details.

The APOLLO V2Ix board has an Atmel AT97SC3203 TPM conforming to the TPM 1.2 specification fitted as standard. The BIOS on the APOLLO V2Ix board also performs basic initialization of the TPM so that it can be used at an OS/application level.

Power supply

The APOLLO board is powered by a standard ATX power supply. Connections for the ATX 20-way power connector are shown on page 39. The board incorporates several power supplies to provide the power requirements of the on-board functions and support for ACPI low power sleep states.

As a minimum, the APOLLO requires the ATX power supply, 5V, 5V standby, 3.3V and 12V power rails. The –5V is not used and the –12V is only required if a PCI card used with the APOLLO requires this power rail. The ATX power supply ‘power good’ and ‘power supply ON’ signals should also be connected.

A combination of full power and standby voltages are generated on the board. The required voltage rails are1.05V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V and a variable CPU voltage (IMVP-IV). A combination of linear and switch mode regulators are used to provide these rails.

The BIOS has built-in power management, which can be enabled at the Power menu within the PhoenixBIOS setup program (see page 84). The power management software can control various aspects of the board. You can choose maximum power savings (to conserve system power), maximum performance (which uses more power), or to specify custom settings.

Most small ATX supplies have a minimum load requirement. At times, the APOLLO board does not meet this requirement and an additional load needs to be added to the system for the supply to turn on correctly.

Front panel interface

The APOLLO provides a front panel interface via connector J24. This interface provides the following features:

- LCD character display interface, which can be used as GPIO if the LCD character function is not required.
- Two user configurable LEDs which can be used as GPIO.
- System Management bus (SMBUS) interface.
- One user defined GPIO.

The base address of the front panel interface registers is programmed by the BIOS at bootup. By default, it is at IO location 500h although operating systems are able to modify this base address location. As such, we strongly recommend using the following code fragment to determine the base address:

```
outportb    0x2E, 0x55      ; Enter configuration mode
outportb    0x2E, 0x07      ; Point to the address register
outportb    0x2F, 0x0A      : Look at the runtime register
outportb    0x2E, 0x60      ; Primary base IO address high
inportb     0x2F, ADDRHI
outportb    0x2E, 0x61      ; Primary base IO address low
inportb     0x2F, ADDRLO
outportb    0x2E, 0xAA      ; Exit configuration mode
```

This routine determines the base address by reading the SuperIO configuration registers. These registers are indexed and use an address register at IO location 2Eh and a data register at 2Fh. It returns the high byte of the address in variable ADDRHI and the low bye in ADDRLO.

Eurotech supplied Windows XP and Linux drivers determine the base address using a routine such as this. Please contact Eurotech support for the latest driver.

LCD interface

The APOLLO board provides an LCD interface that can be used to connect to an HD44780 or similar LCD character display. A contrast voltage and diode-protected LED backlight power supply are also provided.

Pin 4 on connector J24 (see page 49) provides the contrast voltage often required by LCD character displays. The contrast voltage is set to 0.5V on the APOLLO board as standard. This can be modified if required to suit the particular LCD character display used.

The GPIO are all configured by the BIOS as open drain outputs. The IO ports are 5V tolerant IO; with 3.3V drive level when in push-pull mode. The signalling voltage levels on the APOLLO V2Ix and V1Ix are different due to the configuration of the SuperIO.

APOLLO V1Ix GPIO: 5V signalling using open drain outputs, 5V tolerant.

APOLLO V2Ix GPIO: 3.3V Signalling using open drain outputs, 5V tolerant.

Registers V1Ix board

Data direction register

IO address	
D0:	Base address + 23h
D1:	Base address + 24h
D2:	Base address + 25h
D3:	Base address + 26h
D4:	Base address + 27h
D5:	Base address + 28h
D6:	Base address + 29h
D7:	Base address + 2Ah
GPIO1:	Base address + 2Ch
GPIO2:	Base address + 2Dh
ENABLE:	Base address + 30h
IOW:	Base address + 31h
RS:	Base address + 33h

Bit	Description
7	Output type select 1 = Open Drain 2 = Push Pull
6:4	Reserved
3:2	00 = GPIO Others = reserved
1	Polarity 1 = Invert 0 = No invert
0	In/out In = 1 Out = 0

LCD data register

IO address
Base address + 4Bh

Bit	Description
7	D7 Data bit
6	D6 Data bit
5	D5 Data bit
4	D4 Data bit
3	D3 Data bit
2	D2 Data bit
1	D1 Data bit
0	D0 Data bit

LCD control bits, GPIO1 and GPIO2 data registers

The LCD control bits correspond with those used on most standard LCD character displays. GPIO1 and GPIO2 are standalone GPIO that are not used by the LCD interface; the data direction register description describes the configuration of the GPIO.

IO address	Bit	Description
Base address + 4Ch	7	Reserved
	6	IOW
	5	ENABLE
	4	Reserved
	3	Reserved
	2	GPIO2
	1	GPIO1
	0	Reserved

IO address	Bit	Description
Base address + 4Dh	7	Reserved
	6	Reserved
	5	Reserved
	4	Reserved
	3	Reserved
	2	Reserved
	1	Reserved
	0	RS

Registers V2Ix board

Data direction register

IO address	
D0:	Base address + 23h
D1:	Base address + 24h
D2:	Base address + 25h
D3:	Base address + 26h
D4:	Base address + 27h
D5:	Base address + 29h
D6:	Base address + 2Ah
D7:	Base address + 2Bh
GPIO1:	Base address + 34h
GPIO2:	Base address + 37h
ENABLE:	Base address + 54h
IOW:	Base address + 55h
RS:	Base address + 56h

Bit	Description
7	Output type select 1 = Open Drain 0 = Push Pull
6:4	Reserved
3:2	00 = GPIO Others = reserved
1	Polarity 1 = Invert 0 = No invert
0	In/out In = 1 Out = 0

GPIO0/GPIO1 are only available as open drain outputs when in output mode.

LCD data register

IO address
Base address + 4Bh

Bit	Description
7	D7 Data bit
6	D6 Data bit
5	D5 Data bit
4	D4 Data bit
3	D3 Data bit
2	D2 Data bit
1	D1 Data bit
0	D0 Data bit

LCD control bits data register

The LCD control bits correspond with those used on most standard LCD character displays and have the following.

RS – Register Select (Command or Data)

IOW – IO Read/Write

ENABLE – Data enable signal

IO address	Bit	Description
Base address + 50h	7	Reserved
	6	Reserved
	5	Reserved
	4	RS
	3	IOW
	2	ENABLE
	1	Reserved
	0	Reserved

GPIO1 and GPIO2 registers

GPIO1 and GPIO2 are standalone GPIO that are not used by the LCD interface; the data direction register description describes the configuration of the GPIO.

IO address	Bit	Description
Base address + 4Dh	7	Reserved
	6	Reserved
	5	Reserved
	4	GPIO2
	3	Reserved
	2	Reserved
	1	GPIO1
	0	Reserved

User LEDs

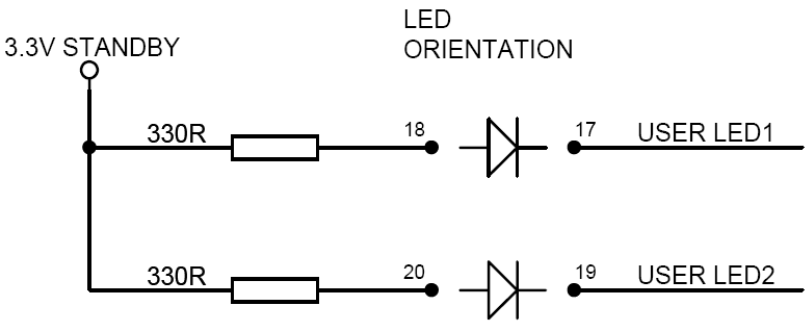
Two connections for LEDs are provided on the front panel interface connector, these can be used as indicators and are accessed through a register in the runtime register block. If enabled these LEDs will remain illuminated whenever standby power is available and are not cleared during a reset event.

The pin connections for the LED allow the user to turn the LEDs on and off and blink independently of each other. Both versions of the APOLLO board utilize the same register address for LED control.

IO address	Bit	Description
LED1: Base address + 5Dh LED2: Base address + 5Eh	7:2	Reserved
	1:0	LED control 00 = Off 01 = Blink, 1Hz rate with 50% duty cycle (0.5 sec on, 0.5 sec off) 10 = Blink, ½ Hz rate with 25% duty cycle (0.5 sec on, 1.5 sec off) 11 = On

The LED connections are designed to power LEDs with a forward voltage drop of 1.5V, most LEDs fall into this category, the exception being blue LEDs which require a higher forward voltage, typically 4V to be illuminated.

The following figure shows the correct connection of a user supplied LED a 330Ω resistor is provided on the APOLLO board so that a direct LED connection can be made.



SMBUS

Connector J24 provides an interface to the system management bus commonly known as the SMBUS. Below is a list of devices that are present on the APOLLO board and their corresponding 7-bit SMBUS address, care should be taken to ensure that any new device added to the bus does not conflict with existing devices as this may cause boot issues.

Boot issues may also occur if the SMBUS clock and data lines are held high or low for an extended period. This is particularly important with devices using external power, as they may not be powered on and configured at the same time the APOLLO accesses the SMBUS.

SMBUS address	SMBUS device
0x2D	SuperIO hardware monitor (APOLLO V1Ix)
0x44	Ethernet 1, default address
0x50	DDR DIMM 0 serial presence device
0x54	CMOS backup EEPROM
0x69	Spread spectrum clock generator IC
0x6A	CK-408 clock generator IC

User jumper

The APOLLO provides two user jumpers for use with program code. These are interfaced to the firmware hub and are IO mapped.

USER jumper	Firmware hub GPI	Alternate function (V1Ix)
1	2	Reload CMOS
2	3	None

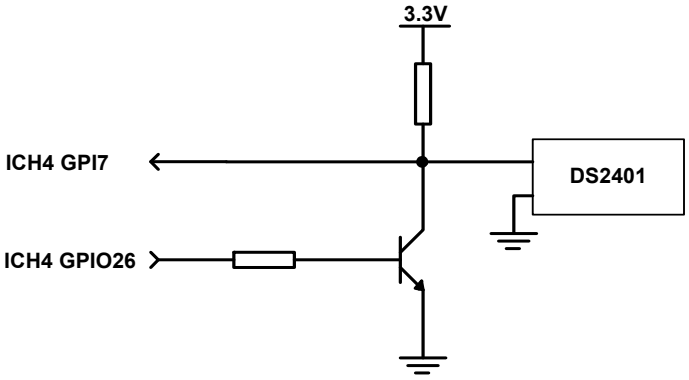
On the APOLLO V1Ix boards, the USER jumper 1 connection has an alternate function to signal to the BIOS to reload the CMOS values from the system BIOS. Care should be taken to ensure that this jumper is not fitted at power on.

On the V2Ix APOLLO boards a dedicated user jumper provides the reload CMOS function.

Unique ID

A Unique ID is provided on the APOLLO using the DS2401 enhanced silicon serial number IC. The DS2401 consists of a factory-lasered 64 bit ROM that includes a unique 48 bit serial number, an 8 bit CRC and an 8 bit family code (01h). The DS2401 has been configured on the APOLLO to interface via two ICH4 GPIO pins:

ICH4 GPIO	Signal name
GPI7	Serial output
GPIO26	Serial input



The Unique ID 48 bit serial number is read by the BIOS and can be displayed during boot. This is provided as an option in the BIOS *Security* menu - see page 81.

System resources

I/O map

IO location	Functional block
0000H – 001FH	DMA controller 1
0020H – 002DH	Programmable Interrupt controller 1
002EH – 002FH	LPC SuperIO index registers
0030H – 003DH	Programmable Interrupt controller 1
0040H – 0043H	System timer 0
0050H – 0053H	System timer
0060H – 0060H	Keyboard controller
0061H – 0067H	Motherboard resources
0070H – 0077H	System CMOS/RTC
0080H – 0091H	DMA controller 1
0092H – 0092H	Port92 reset control register
00A0H – 00B1H	Programmable interrupt controller 2
00B2H – 00B3H	Power management control registers
00B4H – 00BDH	Programmable interrupt controller 2
00C0H – 00DFH	DMA controller 2
00F0H – 00F0H	Coprocessor error register
01F0H – 01F7H	Primary IDE controller
0274H – 0277H	ISAPNP read data port
0279H – 0279H	ISAPNP read data port
02F8H – 02FFH*	COM2 (default)
0378H – 037FH*	LPT1 (default)
03B0H – 03BBH	Graphics controller
03C0H – 03DFH	Graphics controller
03F0H – 03F5H	Floppy disk controller
03F6H – 03F6H	Primary IDE controller
03F7H – 03F7H	Floppy disk controller
03F8H – 03FFH	COM1 (default)
04D0H – 04D1H	Programmable interrupt controller
0500H – 057FH	SuperIO runtime registers
0778H – 077FH	LPT1 (default)
0800H – 080FH	Motherboards resources
0A79H – 0A79H	ISAPNP read data port
0CF8H – 0CFFH	PCI configuration registers
1000H – 107FH	Motherboard resources
1100H – 111FH	Intel SMBUS controller

* The locations marked with an asterisk in the above table are based on the BIOS default setups; the IO location of these devices will change if the default BIOS options are modified.

System memory map

System memory segment	Description
000000H – 09FFFFH	0 – 640KB DOS region
0A0000H – 0BFFFFH	Graphics controller memory region
0C0000H – 0CFFFFH	Video BIOS
0D0000H – 0DAFFFH	Expansion area
0DB000H – 0DBFFFH	PCI 4510A Cardbus controller
0DC000H – 0DFFFFH	Expansion area
0E0000H – 0EFFFFH	Expansion BIOS area
0F0000H – 0FFFFFH	System BIOS area

These locations are based on the BIOS default setups; the memory location of these devices will change if the default BIOS options for the IO ports are modified.

Interrupts

The APOLLO supports two different interrupt modes:

- The standard dual 8259 programmable interrupt controller providing 15 interrupt connections.
- The advanced programmable interrupt controller (APIC) which supports up to 24 interrupt connections.

Most operating systems only provide support for the standard 8259 interrupt controller. However operating systems such as Windows XP® and Windows 2000® support the APIC interrupt mode. The APIC provides a superior interrupt architecture that allows for lower interrupt latency and reduces the number of shared interrupts in a system.

Standard 8259 interrupt connections

The internal connections are routed internally to the 8259 controller. The external interrupts are routed using a serialized interrupt (SERIRQ) mechanism. This is interfaced to the SuperIO for legacy IO, and to the CompactFlash® controller to provide boot support and a TPM when fitted. PCI interrupt mappings are configured by the BIOS during boot.

Master

8259 input	Interrupt source
0	Internal connection to counter 0.
1	Keyboard controller (via SERIRQ).
2	8259 slave connection.
3	IRQ3: configurable. Default connection: Serial port COM2.
4	IRQ4: configurable. Default connection: Serial port COM1.
5	IRQ5: configurable.
6	SERIRQ to floppy disk controller.
7	IRQ7: configurable. Default connection: parallel port LPT1.

Slave

8259 input	Interrupt source
0	Internal connection to real time clock.
1	IRQ9: configurable.
2	IRQ10: configurable.
3	IRQ11: configurable.
4	IRQ12: configurable. Default connection: PS/2 mouse.
5	Internal connection for processor FERR#.
6	IRQ14: Primary IDE.
7	IRQ15: CompactFlash® controller.

Connections for serial, parallel, mouse and CompactFlash are all dependent on BIOS configuration settings.

APIC: Advanced Programmable Interrupt Controller

Use of the APIC interrupt mode is enabled using the field *APIC - IO APIC Mode*, available from the *ACPI Control* sub-menu in the BIOS. See page 78 for further details.

IRQ	Interrupt source
0	Cascade from 8259
1	Keyboard controller
2	8259 counter 0
3	Serial port COM2
4	Serial port COM1
5	SMBus controller
6	Floppy disk controller
7	Configurable
8	High Performance Event Timer/RTC
9	ACPI Subsystem interrupt
10	Configurable
11	Configurable
12	PS/2 compatible mouse
13	Coprocessor error
14	Primary IDE controller
15	Configurable, reserved for the Compact Flash IDE interface when used
16	PCI PIRQ[A]# Connections: VGA controller, PCI UART and USB UHCI controller
17	PCI PIRQ[B]# Connections: AC97 Audio CODEC controller
18	PCI PIRQ[C]# Connections: IEEE1394 Host controller, USB UHCI controller
19	PCI PIRQ[D]# Connections: Cardbus controller, USB UHCI controller
20	PCI PIRQ[E]# Connections: 82562ET Ethernet controller, PCI expansion slot
21	PCI PIRQ[F]# Connections: PCI expansion slot
22	PCI PIRQ[G]# Connections: 82541GI/82551QM Ethernet controller, PCI expansion slot
23	PCI PIRQ[H]# Connections: USB2.0 EHCI Controller, PCI expansion slot

DMA mapping

Mapping	Default use
1	LPT1
2	Floppy Disk Controller
3	Available
4	Cascade from DMA1
5	Available
6	Available
7	Available

Default DMA mappings, changes to the BIOS configuration may modify these mappings.

Appendix A – Specification

CPU

The APOLLO supports:

- Intel Pentium M 478-pin μFCPGA package 90nm and 130nm processors with 400MHz FSB.
- Intel Celeron M 478-pin μFCPGA package 90nm and 130nm processors with 400MHz FSB.
- Intel Ultra Low Voltage Pentium M 479-pin μFCBGA package with 400MHz FSB.

The APOLLO Celeron M 600MHz variant has a non-interchangeable board mounted 600MHz Celeron M processor.

Cache

Pentium M 130nm, 1MB L2 CPU Integrated
Pentium M 90nm, 2MB L2 CPU Integrated
Celeron M 130nm, 512KB L2 CPU Integrated
Celeron M 90nm, 1MB L2 CPU Integrated

Memory

One unbuffered 2.5V DDR SDRAM 184-pin DIMM socket to support 128MB, 256MB, 512MB and 1024MB modules. Supports:

- PC1600 (200MHz) DDR SDRAM.
- PC2100 (266MHz) DDR SDRAM.
- PC2700 (333MHz) DDR SDRAM.

ECC and non-ECC memory is supported by the APOLLO.

Video

Intel Extreme Graphics (chipset integrated).

VGA CRT interface: 2048x1536, 75Hz.

LVDS interface (dual channel): 1600x1200, 60Hz.

An option board interface provides a two channel DVO interface to support:

- Dual channel TMDS (DVI).
- Dual channel LVDS.
- TV out support.

Dual video operation allows for two independent video displays.

Audio

5.1 surround sound AC-97 audio CODEC with variable sampling rate and 3D stereo expansion for simulated surround sound. A header for a speaker is included on the board for PC BEEP functionality.

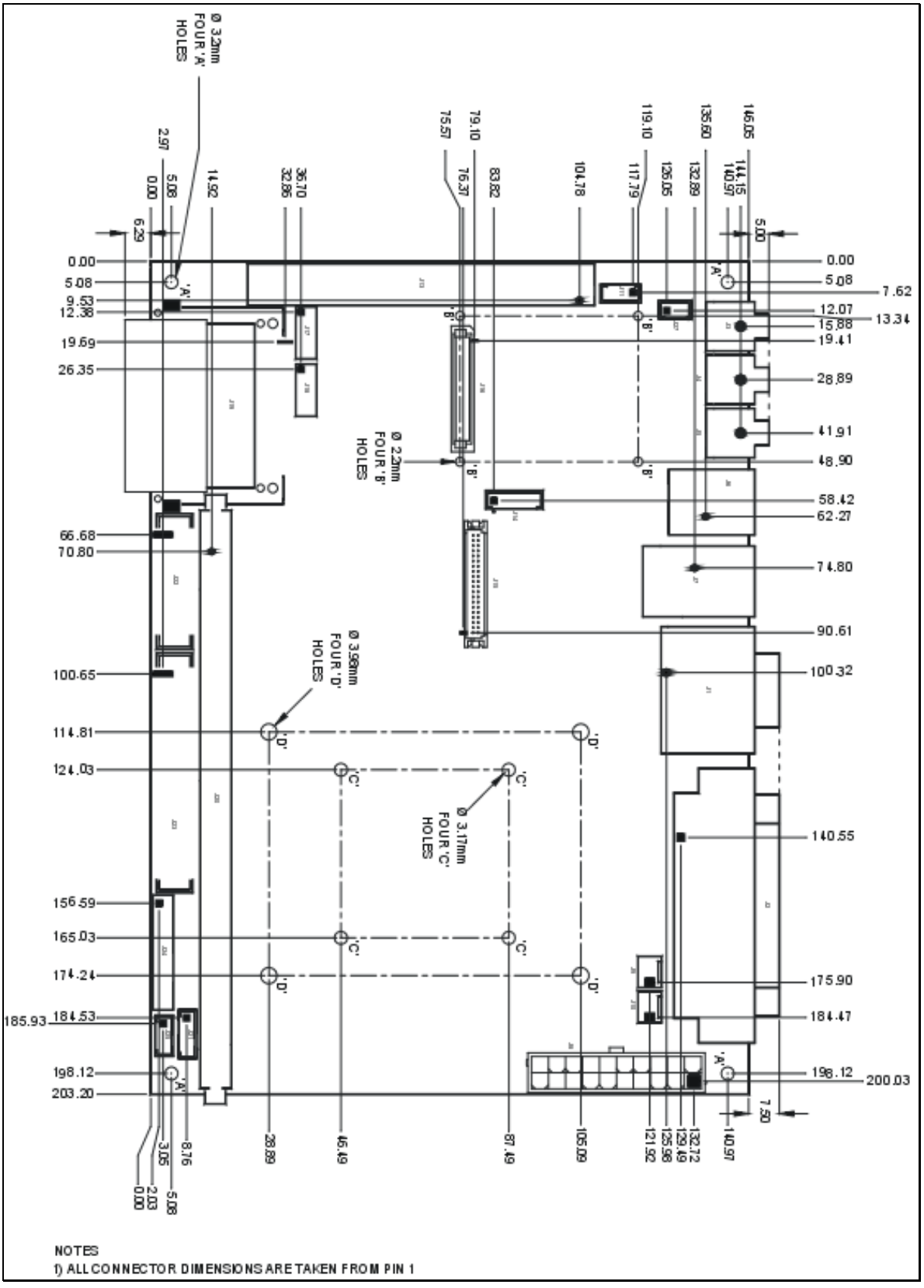
Bus support

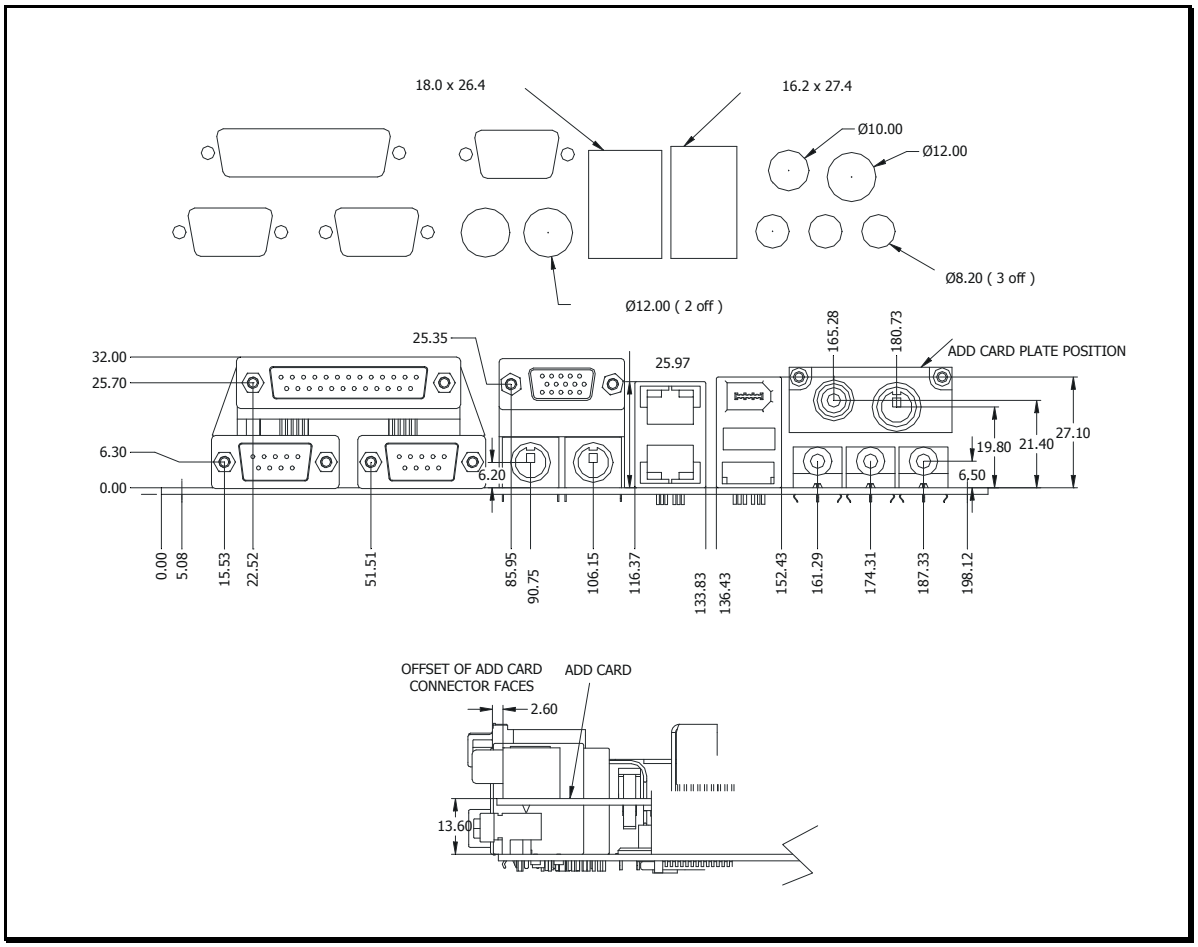
32-bit 33MHz PCI connector rev 2.2 (3 grant/request pairs). Support for 3 PCI cards via a PCI riser card.

IDE drive support	Primary IDE Controller onboard ICH4. Supports Ultra ATA100/66/33, PIO and 8237 style DMA transfers. 40-way 2.54mm IDE connector support provided.
Floppy drive support	100% IBM compatible 2.88MB floppy drive controller with integrated digital separator and dual floppy drive support
I/O ports	One IEEE1284 parallel port (ECP, EPP and SPP modes). One PS/2 mouse port. One PS/2 keyboard port. Four serial ports (3 x RS232, 1 x RS485/RS422/RS232 selectable). One IrDA infrared port (Uses a UART port). One LCD backlight connector. Two user jumpers. One front panel connector providing LCD character display support, 2 x user LEDs, SMBUS interface and 2 x GPIO. One CD ROM audio input connector. One Interface connector to optical S/PDIF transceiver.
Network support	Dual 10/100 Ethernet support. Factory build option of Gigabit Ethernet on primary LAN interface. WOL, WfM, PXE and ASF 1.03 provided on primary LAN interface. All Ethernet controllers interface to board mounted RJ-45's
Real time clock	Motorola MC146818B-compatible real-time clock with 256bytes of battery backed SRAM, integrated in ICH4. A tamper detection circuit is also included in the RTC circuit and it's status held in RTC SRAM memory.
Power consumption	36W at 1.6GHz (full speed). 12.3W at 600MHz (at idle). (Based on a Pentium M 1.6GHz CPU with 512MB PC2700 DDR memory and SpeedStep disabled, i.e. running at fixed frequency.)
CompactFlash®	Single 50 pin CF+ version 2.0 Type I/II socket for full IO mode operation.
IEEE1394a	Two IEEE1394a-2000 Firewire compliant ports 100/200/400 Mbps.
USB	Six USB 2.0 compliant ports capable of high-speed, full-speed and low-speed operation
BIOS	8Mbit Firmware Hub (FWH). CMOS settings battery backed.

Temperature	Fan-less operation (passive cooling): -20°C to +65°C (based on Pentium M CPU running at 600MHz). Operating (active cooling): -20°C to +65°C (based on Pentium M CPU running at 1.6GHz). Storage -40°C (-40°F) to +70°C (158°F).
Humidity	10% to 90% RH (non-condensing).
Real-time clock	Accuracy +/- 1min/month at 25°C (77°F).
Power requirements	ATX Compatible power supply. Typical supply rail requirements with Pentium M 1.6GHz. 12V +/- 5% 2.5A (typical), 3A (max). 5V +/- 5% 1.0A (typical), 1.5A (max). 5V Standby +/- 5% 0.5A (typical), 1A (max). 3.3V +/- 5% 1.0A (typical), 1.5A (max).
Battery	3.0V Lithium 180mAH (CR2032 Coin Cell). Maximum discharge current 6uA.
Dimensions	EBX-compatible format 5.75" x 8.00", 146mm x 203mm
Weight	350 grams (with no heatsink, processor or memory).

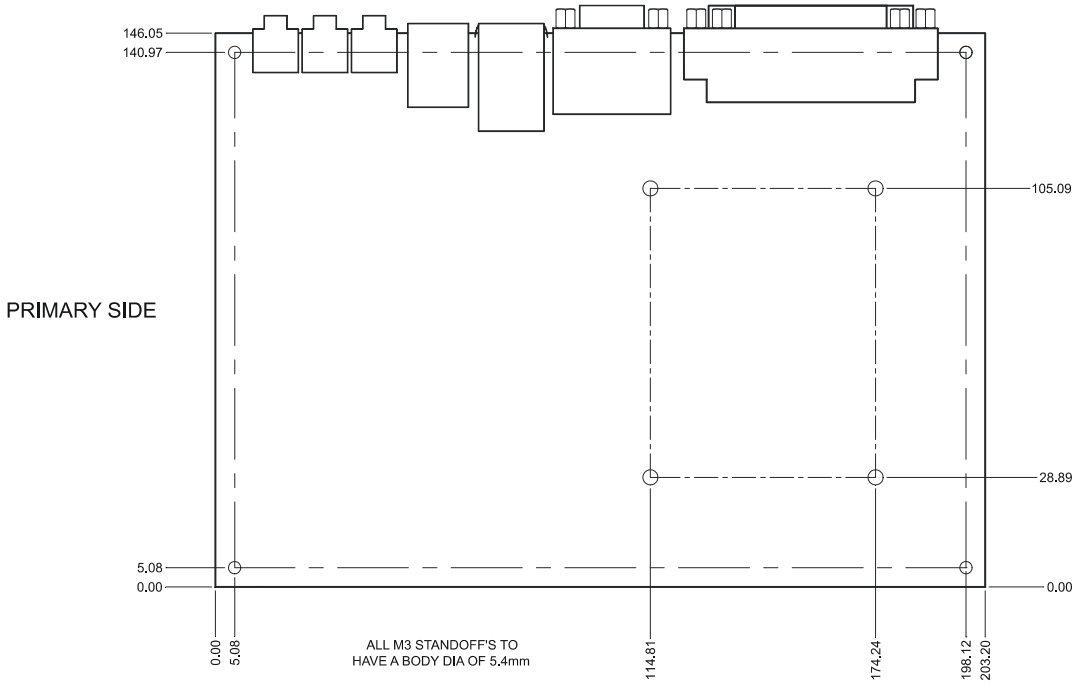
Appendix B – APOLLO mechanical diagram



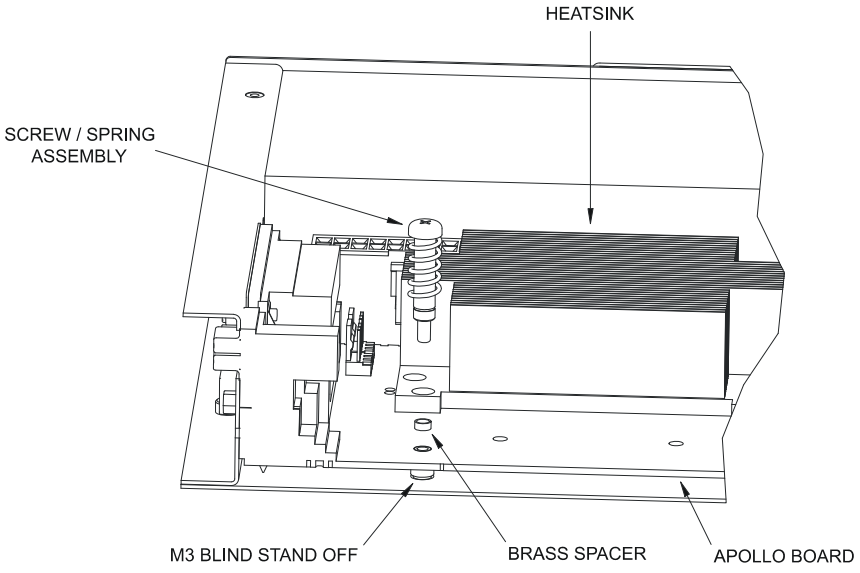

18.0 x 26.4
16.2 x 27.4
Ø10.00
Ø12.00
Ø8.20 (3 off)
Ø12.00 (2 off)
25.35
25.97
165.28
180.73
ADD CARD PLATE POSITION
32.00
25.70
6.30
0.00
6.20
19.80
21.40
27.10
6,50
0.00
5.08
15.53
22.52
51.51
85.95
90.75
106.15
116.37
133.83
136.43
152.43
161.29
174.31
187.33
198.12
OFFSET OF ADD CARD
CONNECTOR FACES
ADD CARD
2.60
13.60

Mounting recommendations

It is strongly recommended that users provide additional support to the APOLLO board using the CPU heatsink mounting holes. This limits flexing of the APOLLO board when DRAM DIMM modules and IDE cables are inserted and removed from the board. All M3 standoffs used in this configuration need to have an outside diameter of at least 5.4mm to prevent the standoff from being drawn into the mounting hole.



If this configuration is used and a large CPU heatsink is used with the APOLLO board then the standard heatsink backing plate is not required and the following configuration should used. The brass spacer has the following dimensions 3.8mm O.D. x 3.0mm.I.D. x 1.7mm long.



Appendix C – TFT display interface cable

The following table shows the connection details for the AU Optronics 15" LCD flat panel display G150XG01 used in the development kits:

APOLLO J17	DF-14H-20P-1.25H	Panel signal name
1	NC	NC
2	NC	NC
3	1	+3.3V
4	2	+3.3V
5	3	Ground
6	4	Ground
7	5	Rin0-
8	8	Rin1-
9	6	Rin0+
10	9	Rin1+
11	7	Ground
12	10	Ground
13	11	Rin2-
14	NC	NC
15	12	Rin2+
16	NC	NC
17	13	Ground
18	NC	NC
19	14	ClkIN-
20	NC	NC
21	15	ClkIN+
22	NC	NC
23	16	Ground
24	19	Ground
25-40	NC	NC

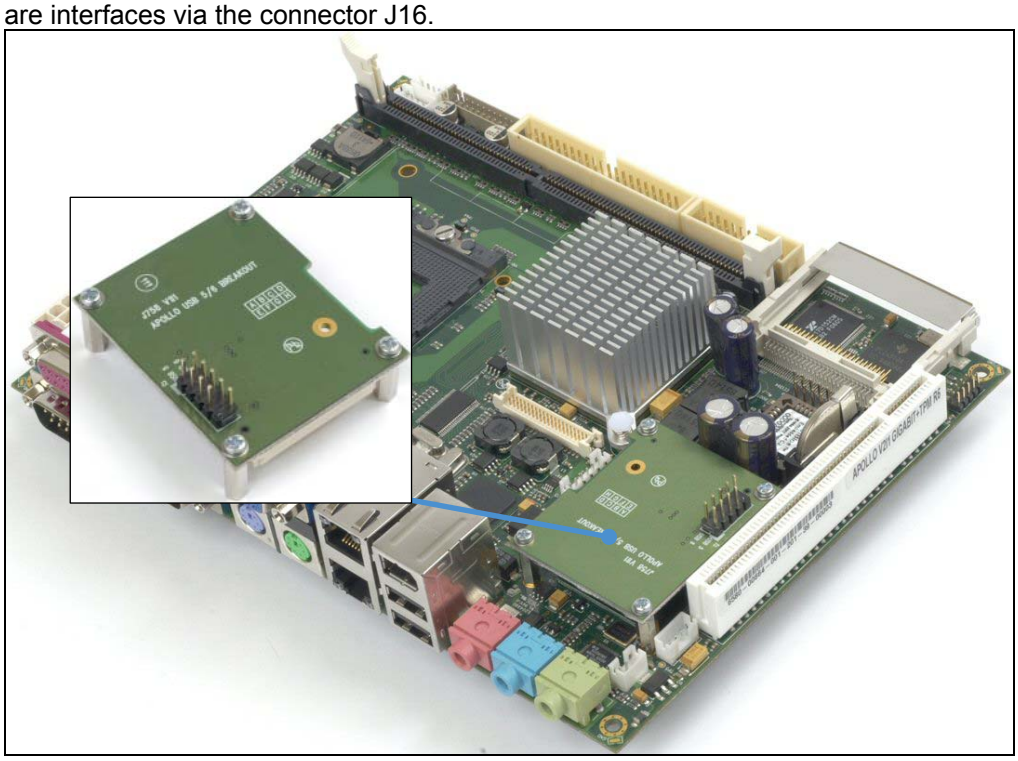
The following table shows the connection details for the TDK CXA-P1612-VJL backlight inverter cable. This configuration allows for PWM based brightness control from the APOLLO board. See J15 – Backlight connector, page 42, and LCD backlight connector, page 96, for further details.

APOLLO J15	51021-0500 housing
1	1
2	2
3	NC
4	3
5	5
6	NC

Pin 4 of the 5 way housing is not used and should be removed.

Appendix D – APOLLO USB 5/6 breakout

A board has been designed to provide a breakout option for the USB 5 and 6 ports which are interfaces via the connector J16.



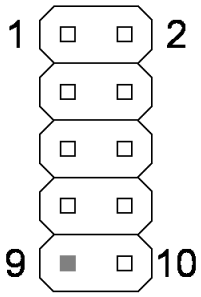
J2 – USB ports 5 and 6

10-way, 2.54mm (0.1") x 2.54mm (0.1") dual row header.

Mating connector: Harwin M20-1070500

Mating connector crimps: Harwin M20-1180022

Pin	Signal name	Pin	Signal name
1	VBUS (port 5)	2	VBUS (port 6)
3	D- (port 5)	4	D- (port 6)
5	D+ (port 5)	6	D+ (port 6)
7	Ground	8	Ground
9	Key (no pin)	10	Ground



For error free data transmission, cable certified for USB 2.0 operation should be used.

Appendix E – DVI video option board

The DVI video option board provides the ability to connect single channel DVI 1.0 compliant display devices to the APOLLO board. This can be used in conjunction with the LVDS or VGA display interfaces to provide dual display capabilities. The following connections refer to pinouts on the DVI board. The option board also provides the same USB functionality as the USB 5/6 breakout and is mounted in the same location.

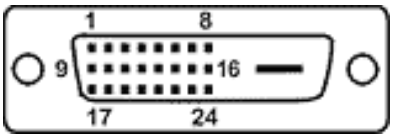
BIOS setup

To enable the operation of the DVI video option board the BIOS setup option *IGD – Boot Type* in the Advanced → Video (Intel IGD) Control Sub-Menu should be set to the External Flat Panel (EFP) option.

J2 – DVI connector

DVI-D (Digital Visual Interface – Digital only)

Pin	Signal name	Pin	Signal name
1	TMDS D2–	13	No connect
2	TMDS D2+	14	+5V Power
3	TMDS D2 shield	15	Ground
4	No connect	16	Hot plug detect
5	No connect	17	TMDS D0–
6	DDC clock	18	TMDS D0+
7	DDC data	19	TMDS D0 shield
8	No connect	20	No connect
9	TMDS D1–	21	No connect
10	TMDS D1+	22	TMDS clock shield
11	TMDS D1 shield	23	TMDS clock+
12	No connect	24	TMDS clock–



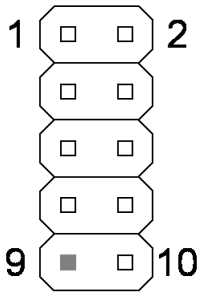
J3 – USB ports 5 and 6

10-way, 2.54mm (0.1") x 2.54mm (0.1") dual row header.

Mating connector: Harwin M20-1070500

Mating connector crimps: Harwin M20-1180022

Pin	Signal name	Pin	Signal name
1	VBUS (port 5)	2	VBUS (port 6)
3	D- (port 5)	4	D- (port 6)
5	D+ (port 5)	6	D+ (port 6)
7	Ground	8	Ground
9	Key (no pin)	10	Ground

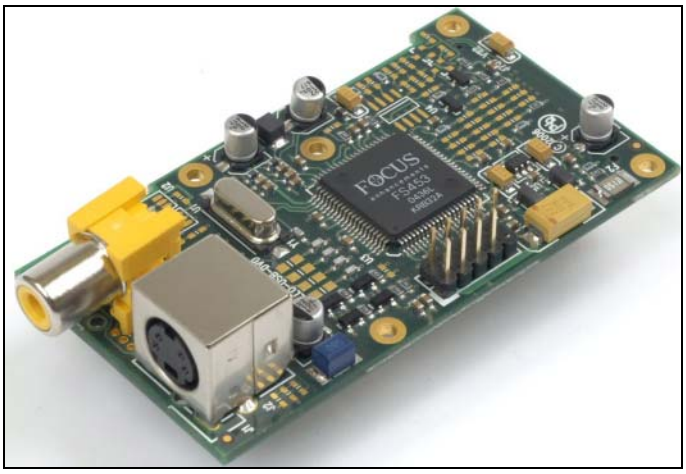


For error free data transmission, cable certified for USB 2.0 operation should be used.

Appendix F – TV out video option board

The TV out video option board provides the ability to encode the DVO output for S-Video and composite video outputs in a wide variety of broadcast quality NTSC and PAL video output modes. Configuration of the video output mode is made using graphics options from within the operating system graphics configuration, Windows XP, XP Embedded and some Linux OS are supported.

The option board also provides the same USB functionality as the USB 5/6 breakout and is mounted in the same location. The following connections refer to pinouts on the TV Out board.



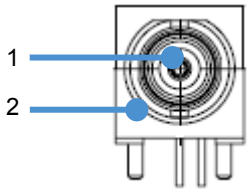
BIOS Setup

To enable the operation of the TV Out Video Option board the BIOS setup option *IGD – Boot Type* in the Advanced → Video (Intel IGD) Control Sub-Menu should be set to the TV option.

J3 – Composite TV OUT

Connector: Kycon KLPX-0848A-2-Y

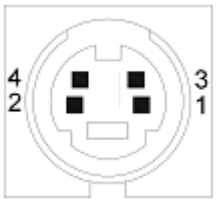
Pin	Signal name
1	CVBS
2	VGND



J2 – S-Video

Connector: 4-pin Mini-DIN, Kycon KMDGX-4S-BS

Pin	Signal name
1	Ground (Y)
2	Ground (C)
3	Y - Intensity (Luminance)
4	C – Colour (Chrominance)



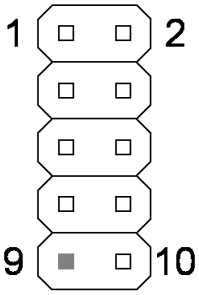
J4 – USB ports 5 and 6

10-way, 2.54mm (0.1") x 2.54mm (0.1") dual row header.

Mating connector: Harwin M20-1070500

Mating connector crimps: Harwin M20-1180022

Pin	Signal name	Pin	Signal name
1	VBUS (port 5)	2	VBUS (port 6)
3	D- (port 5)	4	D- (port 6)
5	D+ (port 5)	6	D+ (port 6)
7	Ground	8	Ground
9	Key (no pin)	10	Ground



For error free data transmission, cable certified for USB 2.0 operation should be used.

Appendix G – VGA option board

The APOLLO VGA option board provides a secondary VGA output that can be used independently or in conjunction with the primary on board VGA output. The option board uses the APOLLO LVDS data and converts this to a standard VGA monitor output. The display resolutions supported are 800x600, 1024x768 and 1280x1024 at a 60Hz refresh rate. A cable is supplied with the board to connect between the APOLLO LVDS connector J17 and the option boards LVDS input connector J2. The option board also provides the same USB functionality as the USB 5/6 breakout and is mounted in the same location. The following connections refer to pinouts on the VGA option board.

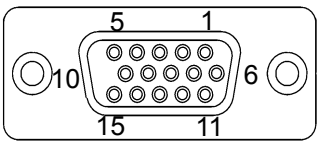
BIOS Setup

To enable the operation of the VGA option board the BIOS setup option *IGD – Boot Type* in the Advanced → Video (Intel IGD) Control Sub-Menu should be set to the CRT+LCD option.

J1 – VGA CRT connector

DB15 female

Pin	Signal name	Pin	Signal name
1	Red	2	Green
3	Blue	4	No connect
5	#Ground	6	AGround
7	AGround	8	AGround
9	+5V (fused)	10	#Ground
11	No connect	12	DDC_SDA
13	HSYNC	14	VSYNC
15	DDC_SCL		



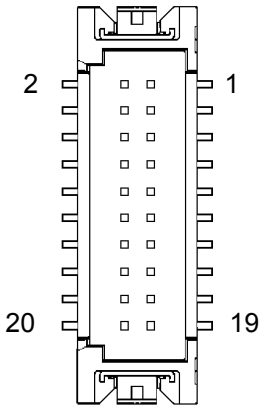
J2 – LVDS input interface (single channel)

20-way 2mm Hirose DF13-20DP-1.25V.

Mating connector: Hirose DF13-20DS-1.25C

Crimps: Hirose: DF13-2630SCFA

Pin	Signal name	Pin	Signal name
1	+3.3V	2	+3.3V
3	GND	4	GND
5	LVDS_D0-	6	LVDS_D0+
7	GND	8	LVDS_D1-
9	LVDS_D1+	10	GND
11	LVDS_D2-	12	LVDS_D2+
13	GND	14	LVDS_CLK-
15	LVDS_CLK+	16	GND
17	DDC_CLK	18	DDC_DATA
19	GND	20	GND



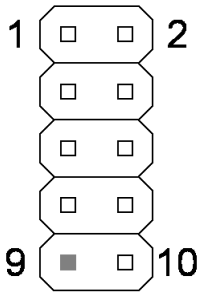
J4 – USB ports 5 and 6

10-way, 2.54mm (0.1") x 2.54mm (0.1") dual row header.

Mating connector: Harwin M20-1070500

Mating connector crimps: Harwin M20-1180022

Pin	Signal name	Pin	Signal name
1	VBUS (port 5)	2	VBUS (port 6)
3	D- (port 5)	4	D- (port 6)
5	D+ (port 5)	6	D+ (port 6)
7	Ground	8	Ground
9	Key (no pin)	10	Ground



For error free data transmission, cable certified for USB 2.0 operation should be used.

Appendix H – Reference information

Product information

Product notices, updated drivers, support material:
www.eurotech.com

PCI special interest group

PCI Bus specification and list of manufacturers:
www.pcisig.org

USB information

Universal Serial Bus (USB) specification and product information:
www.usb.org

Intel

Information about Pentium M and Celeron M processors:
developer.intel.com

CompactFlash®

Information about CompactFlash:
www.compactflash.org

PCI SIG

Information about PCI development:
www.pcisig.com

Digital Display Working Group

Information about developing a digital connectivity specification for high-performance PCs and digital displays:
www.ddwg.com

IEEE Specifications

Information about wired and wireless communication:
www.ieee.org

Trusted Computing Group

Information about TCG open specifications:
www.trustedcomputinggroup.org

Trusted Computing Platform Alliance

Information about Trusted Platform:
www.trustedcomputing.org

Appendix I – RoHS-6 Compliance - Materials Declaration Form

EUROTECH

Confirmation of Environmental Compatibility for Supplied Products

Substance	Maximum concentration
Lead	0.1% by weight in homogeneous materials
Mercury	0.1% by weight in homogeneous materials
Hexavalent chromium	0.1% by weight in homogeneous materials
Polybrominated biphenyls (PBBs)	0.1% by weight in homogeneous materials
Polybrominated diphenyl ethers (PBDEs)	0.1% by weight in homogeneous materials
Cadmium	0.01% by weight in homogeneous materials

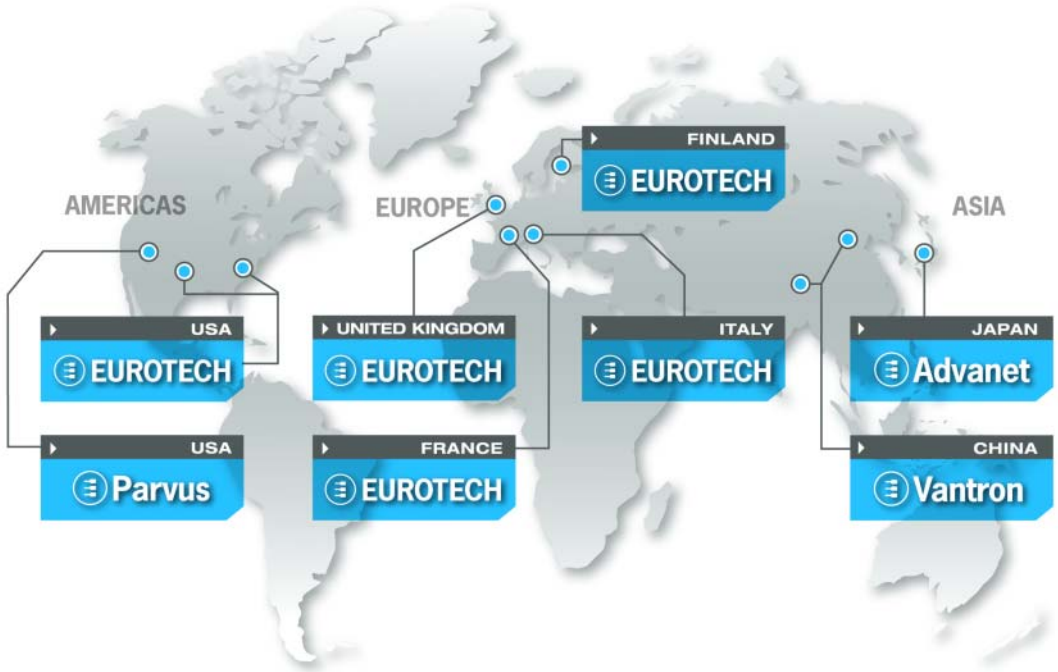
The products covered by this certificate include:

Product name	Eurotech part number
APOLLO-GIGABIT-R6	6580-00664-001-201

Eurotech has based its material content knowledge on a combination of information provided by third parties and auditing our suppliers and sub-contractor's operational activities and arrangements. This information is archived within the associated Technical Construction File. Eurotech has taken reasonable steps to provide representative and accurate information, though may not have conducted destructive testing or chemical analysis on incoming components and materials.

Additionally, packaging used by Eurotech for its products complies with the EU Directive 2004/12/EC in that the total concentration of the heavy metals cadmium, hexavalent chromium, lead and mercury do not exceed 100 ppm.

Eurotech Group Worldwide Presence



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