

# PEGASUS

SINGLE BOARD COMPUTER

Issue D - August 2009 - ETH\_PEGASUS\_USM

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## REVISION HISTORY

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## CONTENTS

|  |    |
|--|----|
| Product handling and environmental compliance .....  | 5  |
| Introduction .....   | 6  |
| Features .....   | 7  |
| About this manual .....  | 8  |
| Conventions .....  | 8  |
| Getting started with the PEGASUS .....   | 9  |
| Setup diagram .....  | 9  |
| Connecting a host PC to the PEGASUS console (COM1) .....                                   | 10 |
| Using a VGA card .....   | 11 |
| Connecting a hard disk drive .....   | 11 |
| Connecting a CD-ROM (IDE type) .....   | 11 |
| Using the PC/104 expansion bus .....   | 11 |
| Using the Ethernet interface .....   | 11 |
| Detailed hardware description .....  | 12 |
| Processor .....  | 12 |
| Memory .....   | 12 |
| Memory map .....   | 14 |
| I/O map .....  | 14 |
| Interrupts .....   | 15 |
| DMA controller .....   | 16 |
| IDE interface .....  | 17 |
| Real time clock .....  | 17 |
| Keyboard/mouse controller .....  | 17 |
| Ethernet controller .....  | 18 |
| User link .....  | 18 |
| PC/104 interface .....   | 18 |
| Serial ports .....   | 19 |
| Power supply .....   | 21 |
| RESET switch .....   | 21 |
| Watchdog timer .....   | 22 |
| SSI (Synchronous Serial Interface) .....   | 22 |
| Links .....  | 23 |
| LK1 - Clear CMOS / battery disable .....   | 24 |
| LK2 - Reset (A8-B8) .....  | 24 |
| LK3 - User link 1 (A7-B7) .....  | 24 |
| LK4 - User link 2 (A6-B6) .....  | 24 |
| LK5 (A5-B5), LK6 (A4-B4), LK7 (A1/2-A2/3), LK8 (B1/2-B2/3) - RS422/485 configuration ..... | 25 |
| Connectors .....   | 26 |
| PL1 - LPT parallel port .....  | 27 |
| PL2 - PS/2 keyboard/mouse .....  | 27 |
| PL3 - 4 x COMS ports .....   | 28 |
| PL5 - SSI .....  | 28 |
| PL6 - IDE HDD connector .....  | 29 |
| PL8 and PL9 - PC/104 interface .....   | 29 |
| PL10 - Ethernet RJ45 .....   | 31 |
| PL11 - Power .....   | 31 |
| PL12 - Ethernet status LEDs .....  | 31 |

|   |    |
|---|----|
| General Software's BIOS set-up .....        | 32 |
| Basic CMOS Configuration screen .....       | 33 |
| Custom Configuration screen .....           | 38 |
| Shadow Configuration Setup screen .....     | 42 |
| Other setup options .....                   | 42 |
| Software support .....                      | 43 |
| Datalight ROM-DOS 6.22 .....                | 43 |
| Datalight FlashFX Flash filing system ..... | 43 |
| FUPDATE utility .....                       | 44 |
| Boot disk .....                             | 44 |
| Example code .....                          | 44 |
| Hardware support information .....          | 45 |
| Appendix A – Specification .....            | 46 |
| Appendix B – Reference information .....    | 47 |
| Appendix C – Troubleshooting .....          | 48 |
| Appendix D – Mechanical drawing .....       | 49 |
| Eurotech Group Worldwide Presence .....     | 51 |

# Product handling and environmental compliance

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## Anti-static handling

This board contains CMOS devices that could be damaged in the event of static electricity being discharged through them. At all times, please observe anti-static precautions when handling the board. This includes storing the board in appropriate anti-static packaging and wearing a wrist strap when handling the board.

## Battery

The board contains a Lithium non-rechargeable battery. Do not short-circuit the battery or place on a metal surface where the battery terminals could be shorted. During shipment the battery is isolated from the board's circuitry and should be connected before using the board.

When disposing of the board or battery, take appropriate care. Do not incinerate, crush or otherwise damage the battery.

## Packaging

Please ensure that should a board need to be returned to Eurotech it is adequately packed, preferably in the original packing material.

## Electromagnetic compatibility (EMC)

The PEGASUS is classified as a component with regard to the European Community EMC regulations and it is the user's responsibility to ensure that systems using the board comply with the appropriate EMC standards.

The PEGASUS ICE Enclosure meets the following standards:

- EN 50081-1 Generic emissions from residential commercial and light industrial environments.
- EN 50082-2 Generic Immunity from industrial environments.
- EN 55024 Class A immunity.
- EN 61000-4-3 Electromagnetic field immunity.
- EN 61000-4-2 Electrostatic discharge immunity.
- EN 61000-4-4 Fast Transients immunity.

## Introduction

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This manual describes the operation and use of Eurotech's PEGASUS Single Board Computer. It has been designed as both a reference and a user manual and includes information on using all aspects of the board.

This board should have been supplied as part of a PEGASUS Development Kit and you should have already read the Quickstart manual.

The PEGASUS is a PC/104 sized, PC/AT compatible processor board that has been designed to be embedded into OEM equipment. It contains all the standard features found in a PC/AT system with some embedded additions.

The board can be purchased in the following standard variants:

- PEGASUS-133-M32-F16: 133MHz CPU, 32MB DRAM, 16MB Flash.
- PEGASUS-133-M16-F8: 133MHz CPU, 16MB DRAM, 8MB Flash.

Please contact Eurotech sales for pricing and availability (see page [51](#)).

## Features

The features included in the PEGASUS are described below.

### CPU

- AMD Elan SC520 133MHz processor (Am5x86 CPU).

### Cache

- 16kB unified cache.

### BIOS

- General Software's Embedded BIOS 4.3 in Flash EPROM.
- Onboard reprogramming.

### System memory

- Up to 64MB SDRAM.

### Silicon disk

- Up to 16MB Intel Strata Flash.
- Datalight FlashFX Flash filling system.

### RAM disk

- 128kB SRAM disk, battery backed (not fitted as standard).

### Integrated I/O

- SMSC FDC37B727 with built-in real time clock and keyboard controller.

### IDE interface

- Supports up to two IDE devices.

### Parallel port

- High speed parallel port, SPP/EPP/ECP modes.
- BIOS configurable.

### Serial ports

- Four 16C550 compatible high speed UARTs:
  - 2 x RS232.
  - 1 x RS422/485.
  - 1 x TTL interface.

### Network support

- National MacPhyter DP83815 10/100-BaseT PCI Ethernet controller.
- 32-bit PCI bus, revision 2.2 compliant.

### Miscellaneous

- 2 x user links.
- SSI (Synchronous Serial Interface).
- Watchdog.

## About this manual




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This manual describes the operation and use of the PEGASUS Single Board Computer. It is designed to be a reference and user manual and includes information about all aspects of the board.

## Conventions

### Symbols

The following symbols are used in this guide:

| Symbol   | Explanation   |
|--|---|
|   | Note - information that requires your attention.  |
|   | Tip - a handy hint that may provide a useful alternative or save time.                            |
|  | Caution – proceeding with a course of action may damage your equipment or result in loss of data. |

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## Getting started with the PEGASUS

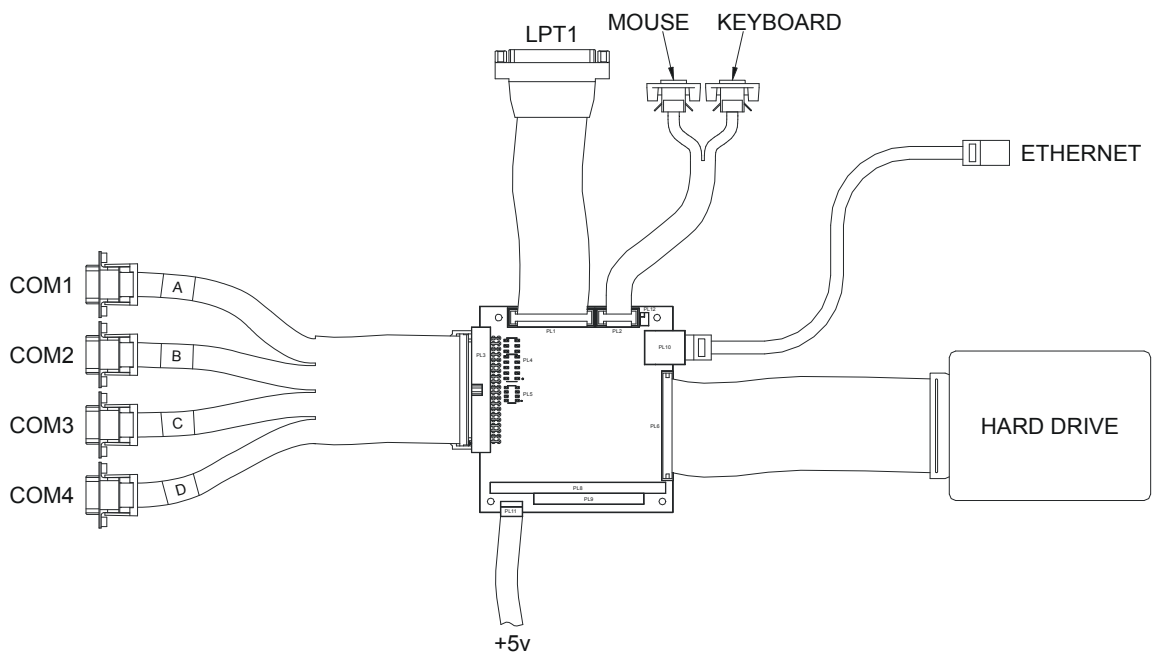
The Development Kit contains a Quickstart manual that has been designed to enable you to set up and start using the board as soon as possible. You should read this manual and follow the steps explaining how to set up the board. Once you have a working PEGASUS system you can start adding other peripherals to begin development.

In this section we guide you through setting up and using some of the features of the PEGASUS. If you would like more detailed information about any aspect of the board refer to the section [Detailed hardware description](#), beginning on page [12](#).

The PEGASUS uses a General Software BIOS (Basic Input-Output System) to provide support for the board. The BIOS has a built-in set-up program for users to modify the basic system configuration. You can invoke the set-up program during the power on sequence by pressing any key when prompted during boot-up. The set-up parameters are stored in the CMOS RAM and, if the battery backup supply is connected, are retained when the power is switched off. See the section [Links](#), page [23](#), for more details.

The BIOS defaults have been selected to enable the board to operate with a minimum of devices connected. If CMOS settings are lost the board will correctly power up and boot from the on-board Flash disk, without any other peripherals connected.

### Setup diagram



## Connecting a host PC to the PEGASUS console (COM1)

As the PEGASUS does not have any video functionality on-board, by default the console is directed to COM1. To view the console you need a null modem cable (see below for details) and a computer with a suitable terminal emulator (for example Windows and HyperTerminal), follow these steps:

- 1 Connect one end of the null modem cable to COM1 on the PEGASUS and the other to your computer.
- 2 Set the terminal emulator as follows:
  - Baud rate: 115200
  - Data bits: 8
  - Parity: None
  - Stop bits: 1
  - Flow control: None
- 3 Plug the power supply into the PEGASUS. You should now see the following in your terminal emulator window:

```

General Software 80486 Embedded BIOS (tm) Version 4.3
00000640K Low Memory Passed
00031744K Ext Memory Passed
Press ^C for Setup

Bus  Dev  Func  Vendid  DevID  Class          Irq
00   00   00    1022   3000   Host Bridge
00   11   00    100B   0020   Ethernet        9

For more information: (800) 850-5755, sales@gensw.com, www.gensw.com.

(C) 2000 General Software, Inc.
80486-4.3-6E65-4A0E
    
```

The null modem cable pin out is shown below:

| 9 way D-type (female) |   | 9 way D-type (female) |
|-----------------------|---|-----------------------|
| 2                     | → | 3                     |
| 3                     | → | 2                     |
| 5                     | → | 5                     |

## Using a VGA card

The alternative to using the serial console functionality of the PEGASUS is to use a PC/104 video card. Although the PEGASUS was not designed for display-orientated systems, the BIOS will automatically detect the presence of a VGA adapter and direct the console through it. When the BIOS is in this mode, it also configures the PS/2 keyboard/mouse interface (PL2).

## Connecting a hard disk drive

The PEGASUS can support up to two IDE hard disk drives. Both drives should be connected to PL6 via a 44-way cable. The primary drive should be set-up as a 'MASTER' and the secondary drive as a 'SLAVE'. The BIOS automatically detects the hard disk drive during the POST (Power-on Self-Test) processes and configures the hardware correctly. The BIOS attempts to load an operating system from the primary disk drive. If the operating system is DOS this drive becomes DRIVE C: when the operating system has loaded. If the on-board Flash memory is fitted and has been formatted as a silicon disk drive, this is allocated as the last drive in the system.

## Connecting a CD-ROM (IDE type)

If you require a CD-ROM drive in the system, you can connect it in place of the secondary drive detailed above. Configure the CD-ROM as a 'SLAVE' device. Drivers are required to support the drive under DOS.

## Using the PC/104 expansion bus

PC/104 modules can be used with the PEGASUS to add extra functionality to the system. The PC/104 interface supports 8/16-bit ISA bus style interfaces.

Eurotech has a wide range of PC/104 modules that are compatible with the PEGASUS. These include modules for digital I/O, analogue I/O, motion control, CAN bus, serial interfaces, and so on. Please contact Eurotech sales (see page 51) if a particular interface you require does not seem to be available, as these modules are continually being developed. Other manufacturers' boards can also be used with this interface if they conform to the PC/104 specification.

In order to use a PC/104 board with the PEGASUS, plug the board into PL8 for 8-bit cards and either PL8 or PL9 for 16-bit cards. Before powering up the system ensure that you have checked that the link settings on the card for I/O address, IRQ, and DMA settings do not conflict with any devices on the PEGASUS.



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A PC/104 card that requires +5V is automatically supplied via the PC/104 header. If you require +12V, this is only available if the +12V pins on the 'POWER' connector PL11 are connected to a supply. If you require -5V or -12V, these will need to be supplied directly to the PC/104 board.

---

## Using the Ethernet interface

The National Semiconductor DP83815 Ethernet controller is used on the PEGASUS. Drivers for various operating systems are supplied on the support CD-ROM, and the appropriate driver must be loaded before the Ethernet interface can be used.

Connection is made via the 8 way RJ45 connector PL10. A second connector PL10 provides outputs that can be used to drive LEDs for TX / RX and LINK status.

## Detailed hardware description

---

This section provides a detailed description of the functions provided by the PEGASUS. This information is useful during development, when adding extra peripherals or starting to use some of the embedded features of the board.

### Processor

The AMD Elan SC520 processor is an Am5x86 class processor with an integrated floating point unit (FPU), compliant with ANSI/IEEE 754 standard. Integrated in the device are a PCI host bridge, SDRAM controller, and enhanced PC/AT-compatible peripherals. The device has been designed to provide a low power, low cost, fully integrated PC/AT compatible architecture. The SC520 is a 32-bit x86 compatible device and has 16K of unified cache integrated into the processor. A 133MHz part is used on the PEGASUS. The processor has a dual supply rail and is powered from +3.3V and 2.5V. These voltages are generated on the PEGASUS from the main +5V supply input.

### Memory

The following sections describe the SDRAM, BIOS EPROM, Flash memory / silicon disk, and battery backed SRAM.

#### SDRAM

There are two variants of the board. One is fitted with 16MB of SDRAM, the other 32MB of SDRAM. These are surface mount devices soldered to the board and cannot be upgraded. The BIOS automatically detects the amount of memory fitted to the board. The board can be fitted with 64MB – contact Eurotech for further information (see page [51](#)).

#### BIOS EPROM

A 256kB Flash EPROM device is used to store the BIOS code. This device can be reprogrammed in situ using the UPDATE utility supplied on the support CD-ROM (see the section [Software support](#), page [43](#), for details). The system BIOS is copied into shadow RAM between 0E0000H and 0FFFFFFH.

The Flash device is a +5V only device and there are no link settings required to enable programming.

## Flash memory / silicon disk

The PEGASUS board supports up to 16MB Flash memory, which is configured as a wear levelling read/write silicon disk drive. The Datalight FlashFX Flash filing system is automatically loaded to enable the Flash drive to be accessed. The Flash drive uses a 16kB memory window at 0D0000-0D3FFF to access the device, and one 16bit I/O address (@ 200h) location is used to select the appropriate Flash area.

The table below shows the 200H 16-bit I/O write:

| Bit no. | Page address register |
|---------|-----------------------|
| 0       | Address bit 14        |
| 1       | Address bit 15        |
| 2       | Address bit 16        |
| 3       | Address bit 17        |
| 4       | Address bit 18        |
| 5       | Address bit 19        |
| 6       | Address bit 20        |
| 7       | Address bit 21        |
| 8       | Address bit 22        |
| 9       | Address bit 23        |
| 10      | Address bit 24        |
| 11      | Not used              |
| 12      | Not used              |
| 13      | Not used              |
| 14      | Not used              |
| 15      | Not used              |

## Battery backed SRAM (not fitted as standard)

The PEGASUS board can be fitted with a 128kB SRAM device on-board, which can be used as a high-speed drive. The SRAM is backed up by the on-board battery, and uses a 16kB memory window at 0D4000-0D7FFF, the same 16-bit page register as used by the Flash, to select the appropriate area.

## Memory map

The following table shows the memory map for the PEGASUS:

| Address            | Block Size | Description                           |
|--------------------|------------|---------------------------------------|
| 100000h –          | 63MB       | (Up to) 63MB SDRAM                    |
| 0E0000h – 0FFFFFFh | 128K       | PC BIOS                               |
| 0DF000h – 0DFFFFh  | 4K         | Elan SC520 configuration registers    |
| 0D8000h – 0DEFFFh  | 28K        | Free                                  |
| 0D4000h – 0D7FFFh  | 16K        | SRAM window (to 128K SRAM), if fitted |
| 0D0000h – 0D3FFFh  | 16K        | Flash window                          |
| 0C0000h – 0CFFFFh  | 64K        | Free                                  |
| 0B0000h – 0BFFFFh  | 64K        | Free                                  |
| 0A0000h – 0AFFFFh  | 64K        | Free                                  |
| 000000h – 009FFFh  | 640K       | System DRAM                           |

## I/O map

The PC/AT I/O address map is limited to 1K addresses. This is because only the lower ten address lines were originally used to decode I/O devices. The remaining lines were treated as undefined. Therefore the usable address range is 0-3FFH. Above this range, devices are mirrored throughout the entire 64K I/O address range of the processor.

The table on the following page shows the I/O address mapping for the PEGASUS. If expansion boards are added via the PC/104 interface you should ensure that they are configured to be at a free address location. Otherwise they will not function correctly and may even cause the PEGASUS board to stop operating.

| Device               | I/O location (Hex) |
|----------------------|--------------------|
| COM1                 | 3F8-3FF            |
| Reserved I/O space   | 3F0-3F7            |
| COM3                 | 3E8-3EF            |
| Reserved I/O space   | 3E2-3E7            |
| PC card              | 3B0-3E1            |
| Reserved I/O space   | 380-3AF            |
| Parallel port        | 378-37F            |
| PC card              | 300-377            |
| COM2                 | 2F8-2FF            |
| Available for PC/104 | 2F0-2F7            |
| COM4                 | 2E8-2EF            |

*continued...*

| Device                                 | I/O location (Hex) |
|--|--------------------|
| PC card                                | 202-2E7            |
| Flash page                             | 200-201            |
| Available for PC/104                   | 1F8-1FF            |
| IDE controller                         | 1F0-1F7            |
| Alternate CPU reset control            | 0EF                |
| Alternate A20 gate control             | 0EE                |
| Master DMA (DMA0)                      | 0C0-0DF            |
| Interrupt controller 2                 | 0A0-0A1            |
| System control port A                  | 092                |
| General registers / DMA page registers | 080-08F            |
| Real time clock                        | 070-071            |
| Keyboard/mouse                         | 060-064            |
| Programmable interval timer (PIT)      | 040-043            |
| Master interrupt controller            | 020-021            |
| Slave DMA (DMA1)                       | 000-00F            |

## Interrupts

The following table shows the PEGASUS interrupts:

| Internal SC520 IRQ | Function | Source          |            |
|--------------------|----------|-----------------|------------|
| Master<br>ICU      | IRQ0     | Timer Tick      | Elan SC520 |
|                    | IRQ1     | Keyboard        | Super I/O  |
|                    | IRQ2     | Slave ICU       | Elan SC520 |
|                    | IRQ3     | COM2            | Elan SC520 |
|                    | IRQ4     | COM1            | Elan SC520 |
|                    | IRQ5     | Reserved        | -          |
|                    | IRQ6     | Free            | PC/104     |
|                    | IRQ7     | Parallel port   | Super I/O  |
| Slave<br>ICU       | IRQ8     | Real time clock | Elan SC520 |
|                    | IRQ9     | Ethernet        | DP83815    |
|                    | IRQ10    | COM4            | Super I/O  |
|                    | IRQ11    | COM3            | Super I/O  |
|                    | IRQ12    | PS/2 mouse      | Super I/O  |
|                    | IRQ13    | Co-processor    | Elan SC520 |
|                    | IRQ14    | IDE drive       | -          |
|                    | IRQ15    | Free            | PC/104     |

These IRQs are only available to devices external to the Elan SC520 if they are configured to use one of the external programmable interrupt pins of the Elan SC520. Each of these pins is programmable to correspond to one of the Elan SC520 internal interrupts (IRQ1, IRQ3-IRQ15). For further information please refer to the AMD Elan SC520 Microcontroller User Manual. The Elan SC520 internal interrupts are configured to correspond to the interrupts available in the PC/AT system.

The external interrupt pins of the Elan SC520 are connected to the PC/104 interface and the SMSC FDC37C932 Super IO controller. The table below shows the connections and default programming for the interrupts:

| Elan SC520 external interrupt pin | Elan SC520 internal interrupt | PC/104 interface | SuperIO interrupt pin | Usage                  |
|-----------------------------------|-------------------------------|------------------|-----------------------|------------------------|
| PIRQ0                             | IRQ11                         | IRQ11            | IRQ11                 | COM3                   |
| PIRQ1                             | IRQ1                          | -                | IRQ1                  | Keyboard               |
| PIRQ2                             | IRQ12                         | IRQ12            | IRQ12                 | Mouse*                 |
| PIRQ3                             | IRQ3                          | IRQ3             | IRQ3                  | COM2*                  |
| PIRQ4                             | IRQ10                         | IRQ4             | IRQ4                  | COM4*                  |
| PIRQ5                             | -                             | -                | -                     | Reserved               |
| PIRQ6                             | IRQ6                          | IRQ6             | IRQ6                  | PC104                  |
| PIRQ7                             | IRQ7                          | IRQ7             | IRQ7                  | PC104 / printer (LPT)* |
| PIRQ8                             | IRQ15                         | IRQ15            | -                     | PC104                  |
| PIRQ9                             | IRQ9                          | IRQ9             | -                     | Reserved               |
| PIRQ10                            | IRQ14                         | -                | IRQ10                 | IDE*                   |

## DMA controller

There are two 8237A compatible DMA controllers internal to the Elan SC520. These controllers are cascaded in a standard PC/AT style and provide seven user DMA channels. There are four 8-bit channels and three 16-bit channels.

Any two of the seven channels can be mapped to the two external DMA request/acknowledge lines provided by the Elan SC520. The table below shows the default assignment for the DMA channels on the PEGASUS:

| DMA | Usage                    | External channel |
|-----|--------------------------|------------------|
| 0   | Unassigned               | PRDQ0 / PDACK0#  |
| 1   | Unassigned               | PRDQ1 / PDACK1#  |
| 2   | Unassigned               | PRDQ2 / PDACK2#  |
| 3   | Parallel port (ECP mode) | PRDQ3 / PDACK3#  |
| 4   | Unassigned               |                  |
| 5   | Unassigned               |                  |
| 6   | Unassigned               |                  |

The four external DMA channels of the Elan SC520 are connected to DMA channels 0 to 3. Channel 3 may only be used if the parallel port is disabled.

\* These IRQs can be enabled for PC104, by disabling options in the BIOS. Refer to the section [Custom Configuration screen](#), page 38.



## IDE interface

The PEGASUS has a single Integrated Drive Electronics (IDE) controller that supports up to two hard disk drives. The disk drives are connected via a 1:1 44-way ribbon cable or 40 -> 44 way ribbon cable using PL6 (see page [29](#) for pin assignment details). One drive must be configured as a 'MASTER' and the other drive as a 'SLAVE'. An IDE compatible CD-ROM drive can also be used and should be configured as the 'SLAVE' device.

If a hard disk drive is attached to this interface the default configuration causes the drive to be used as the standard boot device and the Flash disk (if present) to become the next available drive.

## Real time clock

The PEGASUS uses the real time clock internal to the Elan SC520. It is fully compatible with the MC146818A standard clock device used in PC/AT systems. The date and time functions are stored in the real time clock when the main power is removed if the battery backup supply is enabled (see the section [LK1 - Clear CMOS / battery disable](#), page [24](#), for more information). The real time clock is decoded in I/O address space at 70-71H. The real time clock registers are accessed via an indexed addressing mechanism. I/O location 70h is used to select the appropriate register and location 71H is used to access the data. See the Elan SC520 Microcontroller Register Set Reference Manual for further details.

The real time clock and CMOS settings are maintained by the battery backup circuit when the main power input is disconnected. A lithium cell provides the battery backup supply and has a capacity of 170 mAH. This battery provides sufficient support for at least 3 years continuous backup. The battery is disabled during shipment to prolong its useful life. If the board is going to be placed out of service for long periods of time then the battery should again be disabled. If the main supply is present on the board the battery is automatically disconnected from the real time clock circuitry.

The accuracy of the real time clock is based on the operation of the 32.768kHz watch crystal. This provides an accuracy of +/- 1 minute per month if the board is in an ambient environment of +25°C. If the board is operated outside this temperature the accuracy may be degraded.

## Keyboard/mouse controller

The SMSC FDC37B727 SuperIO controller provides support for a standard PC/AT keyboard and mouse. Both interfaces are present on PL2, see page [27](#) for pin assignment details. The keyboard controller is decoded at I/O address location 60-64H and uses IRQ1 for keyboard and IRQ12 for mouse support. Power for the keyboard and mouse is sourced from the +5V supply.



These interfaces are only initialised by the BIOS when there is a VGA board present. The IRQs are disabled when the interfaces are not in use.

---

## Ethernet controller

A National Semiconductor DP83815 Ethernet controller provides a 10/100-BASET interface. This is a 32-bit PCI device that is configured by the BIOS during power ON. The device provides compliance with IEEE802.3u 100BASE-T specification and IEEE 802.3x Full Duplex Flow Control. A 93C46 EEPROM is used to store configuration data and ID information.

An 8-way RJ45 connector PL10 is used to provide signals (see page [31](#), for pin assignment details).

A second connector PL12 (see page [31](#), for pin assignment details) also provides users with status signals that are designed to drive LEDs. The status lines provide 10M, 100M, and LINK status.

The support CD-ROM contains drivers for most operating systems and network software. These are stored in the ETHERNET directory.

## User link

LK3 and LK4 of the PEGASUS are user links. The status of this user link can be read via superIO I/O mapped registers. If the link is made then the bit will be read as logic '0' (see page [24](#) for further details). This link does not have any defined function on the board and therefore can be used to select options in the application program. Refer to the section [Software support](#), page [43](#), for details of example code.

## PC/104 interface

The PC/104 interface supports 8/16-bit ISA style PC/104 signals. Add-on boards can be used to enhance the functionality of the main board. A large number of companies have adopted the PC/104 standard and boards are available which support a wide range of interfaces. This bus can be used to add digital I/O, analogue I/O, serial ports, video capture devices, PC CARD interfaces, motion control devices, etc.

Any board plugged into this interface will be accessed as if it were part of the main board. Therefore it may conflict with I/O and memory devices on-board, if it has not been correctly configured. Before using an expansion board you should check that it can be configured to work alongside the peripherals already incorporated on-board.

The PC/104 bus signals are fully compatible with the ISA bus electrical timing definitions. Some IRQ and DMA signal lines may be associated with on-board devices and are therefore not free to be used by add-on boards.

## Serial ports

There are four high-speed 16550 serial UARTs on the PEGASUS: two RS282, one TTL, and one RS422/485.

The Elan SC520 device supports COM1 (RS232) and COM2 (RS232). The SuperIO FDC37B727 device supports COM3 (TTL) and COM4 (RS422/485).

The table below shows the configuration for each channel:

| Port               | I/O address | Elan SC520 internal IRQ |
|--------------------|-------------|-------------------------|
| COM1 (RS232)       | 3F8-3FFH    | IRQ4                    |
| COM2 (RS232)       | 2F8-2FFH    | IRQ3                    |
| COM3 (TTL)         | 3E8-3EFH    | IRQ11                   |
| COM4 (RS422 / 485) | 2E8-2EFH    | IRQ10                   |

### RS232 interfaces

Both RS232 channels are fully software compatible with the 16550 and can be used as standard RS232 serial interfaces.

### TTL interface

The TTL interface is an unbuffered serial port, offering full hardware handshaking. The UART is fully 16550 compatible.

### RS422/485 interfaces

The COM4 serial interface can be used to support RS422 or RS485 interfaces. The default link configuration has been selected to enable COM4 as RS422.

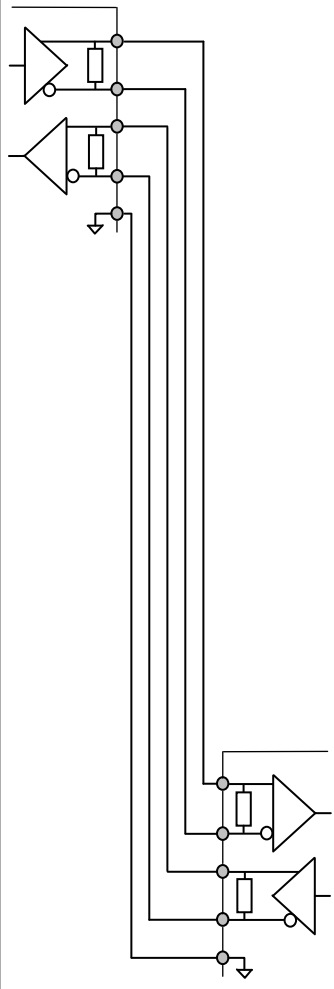
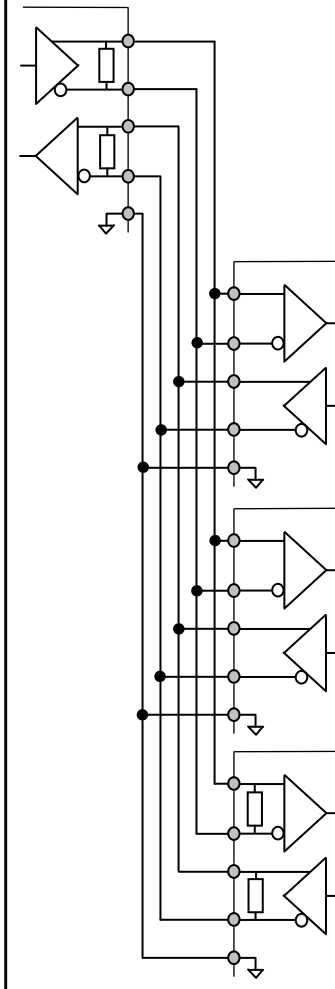
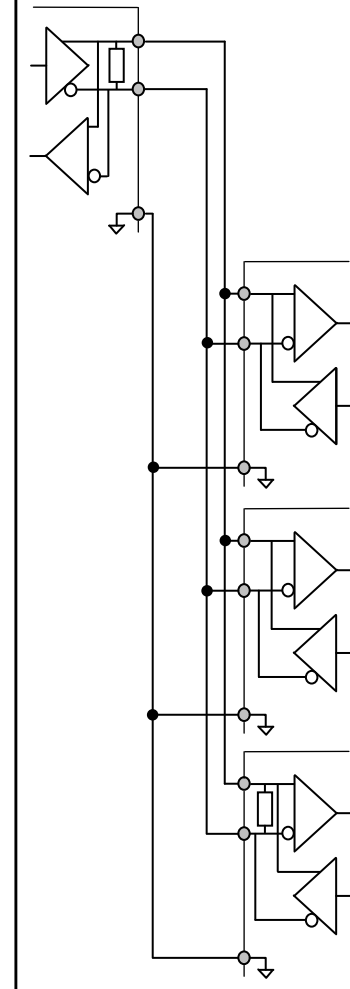
#### RS422

The RS422 interface provides full duplex communication. The signals available are TX+, TX-, RX+, RX-, and Ground. The maximum cable length for an RS422 system is 1200m (4000ft) and it supports 1 driver and up to 10 receivers. To enable RS422 operation, links LK7 and LK8 should be in position B and the RTS line of COM3 should be at logic '0'. Links LK5 and LK6 should be made (to connect the 120Ω line termination resistors) if the board is at either end of the network.

RS485

RS485 is a half-duplex interface that provides combined TX and RX signals. PL3 pin 5 provides TX+/RX+ and pin 6 provides TX-/RX-. A ground connection (Pin 10) is also required for this interface. The maximum cable length for RS485 is the same as RS422 (4000ft), but RS485 supports up to 32 transmitters and receivers on a single network. Only one transmitter should be switched on at a time.

The PEGASUS uses the RTS signal to control transmission. When this signal is at logic '1', the driver is switched off and data can be received from other devices. When the RTS line is at logic '0', the driver is on. Any data that is transmitted from the PEGASUS is automatically echoed back to the receiver. This enables the serial communications software to detect that all data has been sent and disable the driver when required. Links LK7 and LK8 should be in position A to enable the RS485 interface. Links LK5 and LK6 should be made (to connect the 120Ω line termination resistors) if the PEGASUS is at either end of the network. The differences between each of the configurations are illustrated below:

| RS422 POINT-TO-POINT   |        | RS422 MULTI-DROP  |            | RS485 MULTI-DROP   |            |
|--|--------|---|------------|--|------------|
|  |        |  |            |  |            |
| Number of Wires  | 5      | Number of Wires   | 5          | Number of Wires  | 3          |
| Transmitters Enabled   | always | Transmitters Enabled  | active RTS | Transmitters Enabled   | active RTS |
| Receivers Enabled  | always | Receivers Enabled   | always     | Receivers Enabled  | always     |
| Duplex Mode  | full   | Duplex Mode   | full       | Duplex Mode  | half       |
| LK7  | B      | LK7   | B          | LK7  | A          |
| LK8  | B      | LK8   | B          | LK8  | A          |

## Parallel port

The parallel port is fully IEEE1284 compatible and provides Standard Parallel Port (SPP), Enhanced Parallel Port (EPP), and Extended Capabilities (ECP) support. The parallel port is decoded at I/O address location 378-37FH (LTP1) and uses IRQ7.



The default BIOS set-up does not initialise IRQ7 for use by the parallel port. If the parallel port is to be used with interrupts, change the BIOS default settings. See the BIOS set-up section of this manual for more details.

The parallel port has built in protection circuitry to protect against powered devices being connected when the main supply is removed and damaging the device. Each data and control signal is designed to sink 24mA maximum, and source 12mA maximum.

The parallel port connector PL1 is a 26-way 0.1" boxed header. The pin assignment of this connector has been designed to provide 1:1 connection to an IDC 25-way D-Type socket (see [27](#) for pin assignment details). This socket is compatible with a standard PC parallel port connector.

The parallel port can be used to connect an external printer, tape drive, disk drive, scanner, etc.

## Power supply

The PEGASUS is designed to operate from a single +5V +/- 5% (4.75V to +5.25V) supply.

The 5V is monitored automatically onboard and if this supply falls below 4.63V the board is placed in RESET. When the power supply rises above this threshold voltage the board starts to operate again. This power supply monitor ensures that the board does not hang if the supply voltage fails at any point.

An external battery connection +VBAT is also provided. An external battery can be fitted to provide the battery backup for the BIOS CMOS settings, the real time clock and the SRAM disk drive. The external battery will supply power to the battery backup circuit when there is no +5V supply to the board AND the internal battery is disconnected or the internal battery has a lower voltage than the external battery. The battery needs to have a voltage of no less than 2.8V and no more than 3.3V.

## RESET switch

A momentary switch may be connected on LK2. If the switch is pressed the board is reset and the BIOS starts executing from the top of memory. This may be useful during development to restart the board if the software crashes.

## Watchdog timer

The PEGASUS contains a watchdog timer, which can be used to protect against application software conditions that may cause the PEGASUS to 'hang'. The watchdog timer, once started, will trigger a CPU reset if it is not re-triggered within a set timeout period. The timeout period can be set to a value between 492µs and 32.31s. For information on programming the watchdog timer please see the supplied example code on the Development Kit CD-ROM.

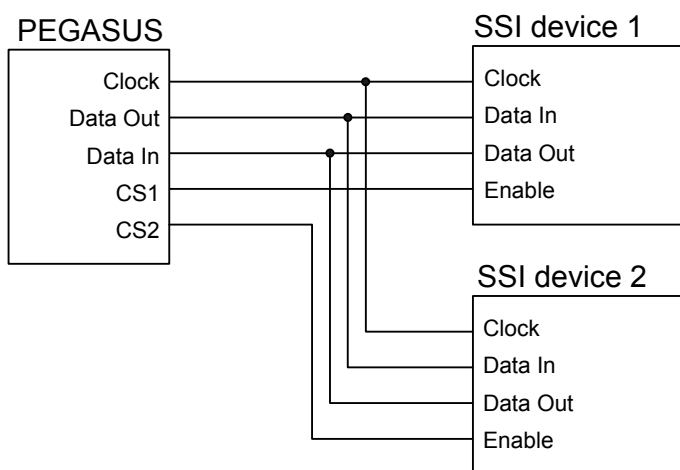
## SSI (Synchronous Serial Interface)

The PEGASUS includes a synchronous serial interface (SSI). It can easily communicate with slave interfaces that are compatible with Motorola's Serial Peripheral Interface (SPI), Motorola's Serial Communication Port (SCP), National Semiconductor Corporation's Microwire, and other industry standards.

Five SSI signals are supplied:

- 1 Clock.
- 2 Data in.
- 3 Data out.
- 4 CS1.
- 5 CS2.

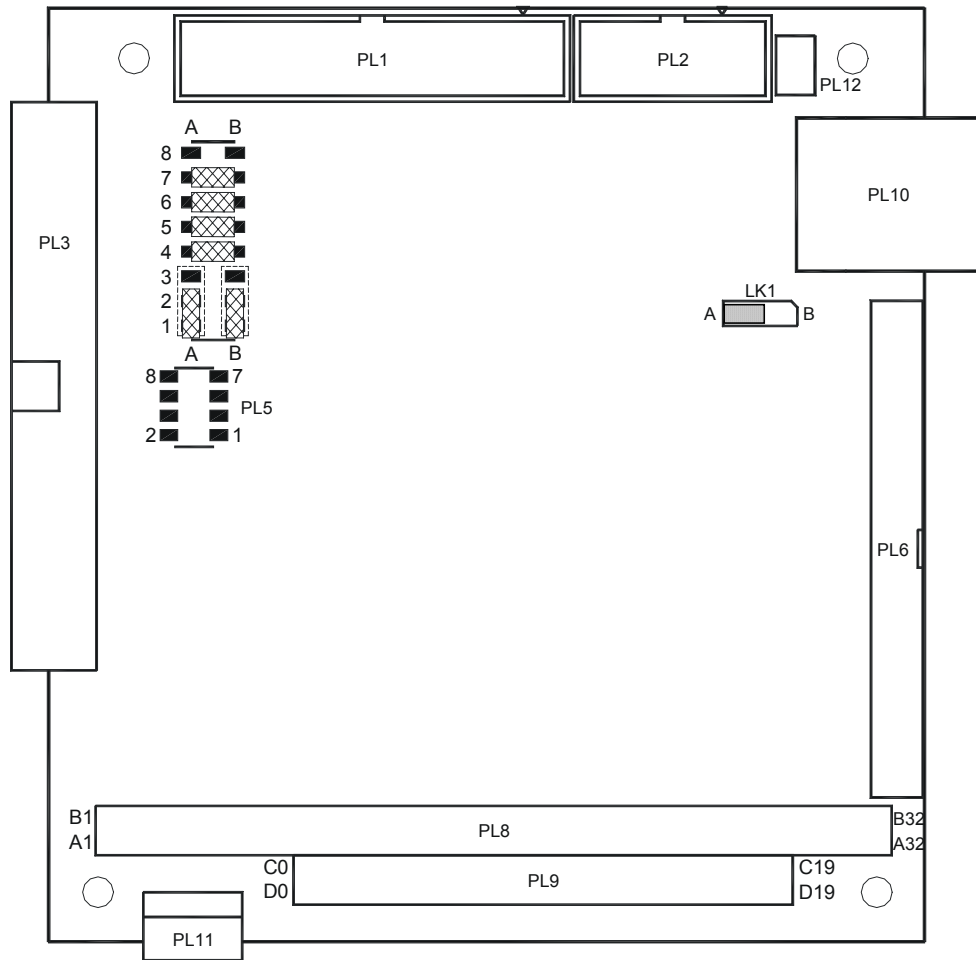
### Wiring example



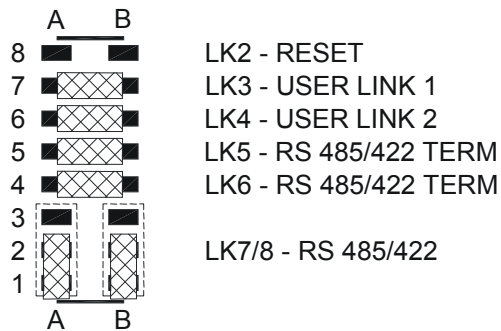
Example software for the SSI port is supplied on the Development Kit support CD, which demonstrates how to communicate with a Dallas Semiconductor DS1306 device.

# Links

There are eight user-selectable links on the PEGASUS. The following diagram shows the links in their default locations:



Below is a diagram showing the configuration of the links:



The following pages provide further information for each link. In each diagram the '+' sign indicates the default position for the link.

## LK1 - Clear CMOS / battery disable

A battery link is fitted that is used to prevent drain on the battery during shipment. This link can also be used to clear the contents of the CMOS RAM.

| LK1 | Description                                |
|-----|--|
| A+  | Battery backup disabled (CMOS RAM cleared) |
| B   | Battery backup enabled                     |

## LK2 - Reset (A8-B8)

If desired, you may connect a momentary switch to LK2. When the button is pressed it puts the board into a full hardware reset; when the link is open circuit, the board starts executing from the top of memory. This is useful during development to restart the board after a software crash.

## LK3 - User link 1 (A7-B7)

LK3 is a user configuration link. It has no reserved function on the PEGASUS, but can be used by an application program to signify a configuration setting. The position of this link can be read via GP66 on the SuperIO.

| LK3  | Description       |
|------|-------------------|
| Fit+ | GP66 is 'Logic 0' |
| Omit | GP66 is 'Logic 1' |

## LK4 - User link 2 (A6-B6)

LK4 link is a user configuration link. It has no reserved function on the PEGASUS, but can be used by an application program to signify a configuration setting. The position of this link can be read via the GP52 on the SuperIO.

| LK4  | Description       |
|------|-------------------|
| Fit+ | GP52 is 'Logic 0' |
| Omit | GP52 is 'Logic 1' |



## LK5 (A5-B5), LK6 (A4-B4), LK7 (A1/2-A2/3), LK8 (B1/2-B2/3) - RS422/485 configuration

These links are used to configure the RS422/485 serial interface. They can be used to select either RS485 (half-duplex) or RS422 (full-duplex) connection and RS422/485 line termination. See the section [RS422/485 interfaces](#), page 19 for more details.

| LK5  | Description  |
|------|--|
| Fit+ | RS422 TX line termination resistor (120Ω) connected    |
| Omit | RS422 TX line termination resistor (120Ω) disconnected |

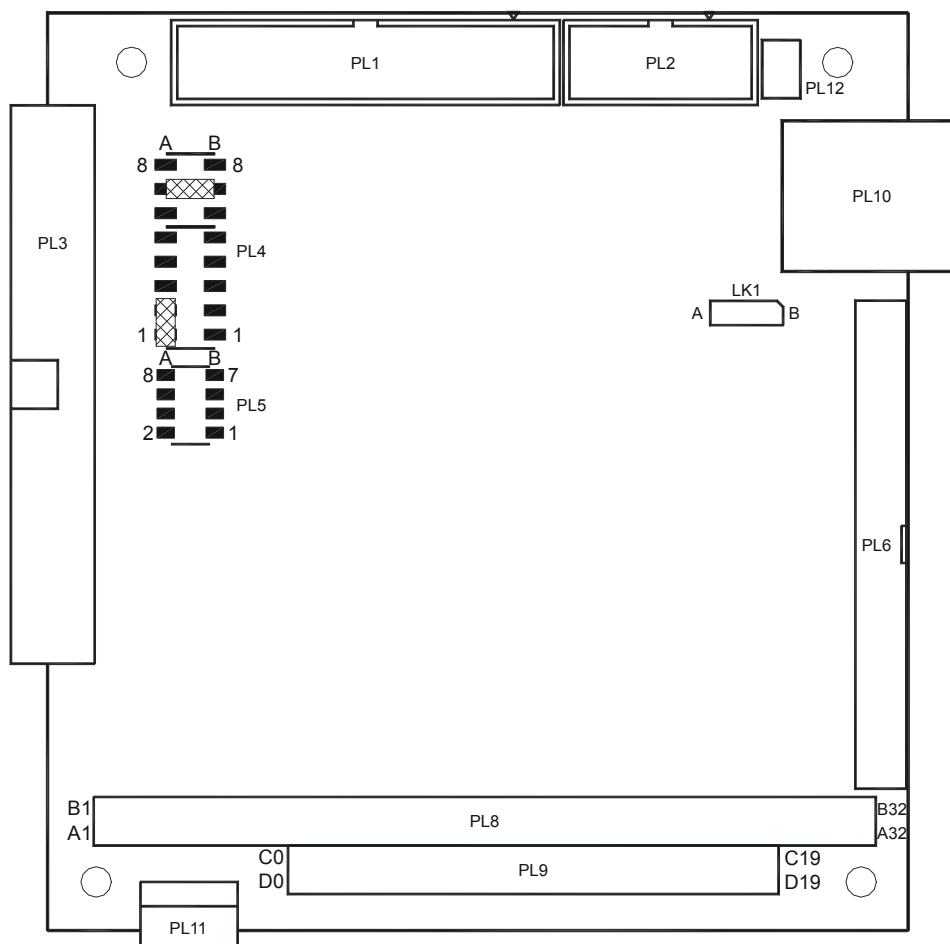
| LK6  | Description  |
|------|--|
| Fit+ | RS485 (RS422 RX line) termination resistor (120Ω) connected    |
| Omit | RS485 (RS422 RX line) termination resistor (120Ω) disconnected |

| LK7 and LK8 | Description                                 |
|-------------|---|
| A+          | RS485 half-duplex connection (A2-A3. B2-B3) |
| B           | RS422 full-duplex connection (A1-A2. B1-B2) |



Both LK7 and LK8 must be set to the same position, i.e. both set to 'A' or both set to 'B'.

# Connectors

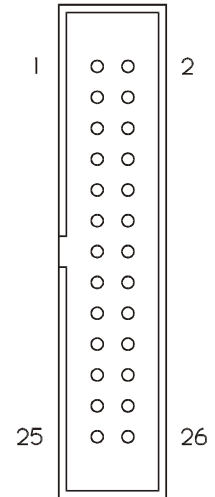


| Connector | Description             | See ...                 |
|-----------|-------------------------|-------------------------|
| PL1       | Parallel port interface | Page <a href="#">27</a> |
| PL2       | PS/2 keyboard/mouse     | Page <a href="#">27</a> |
| PL3       | 4 x serial ports        | Page <a href="#">28</a> |
| PL4       | Link header             | Page <a href="#">28</a> |
| PL5       | SSI interface           | Page <a href="#">28</a> |
| PL6       | IDE interface           | Page <a href="#">29</a> |
| PL7       | Factory use only        | -                       |
| PL8       | 8-bit PC/104 expansion  | Page <a href="#">29</a> |
| PL9       | 16-bit PC/104 expansion | Page <a href="#">29</a> |
| PL10      | Ethernet                | Page <a href="#">31</a> |
| PL11      | Power header            | Page <a href="#">31</a> |
| PL12      | Ethernet status header  | Page <a href="#">31</a> |

## PL1 - LPT parallel port

Connector: 26-way 0.1" IDC header.

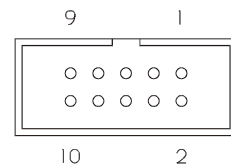
| Pin | Signal name      | Pin | Signal name |
|-----|------------------|-----|-------------|
| 1   | /STROBE          | 2   | /AUTO       |
| 3   | D0               | 4   | /ERROR      |
| 5   | D1               | 6   | /INIT       |
| 7   | D2               | 8   | /SELECT     |
| 9   | D3               | 10  | Ground      |
| 11  | D4               | 12  | Ground      |
| 13  | D5               | 14  | Ground      |
| 15  | D6               | 16  | Ground      |
| 17  | D7               | 18  | Ground      |
| 19  | /ACK             | 20  | Ground      |
| 21  | BUSY             | 22  | Ground      |
| 23  | PAPER END        | 24  | Ground      |
| 25  | Printer selected | 26  | No connect  |



## PL2 - PS/2 keyboard/mouse

Connector: 10-way 0.1" IDC header.

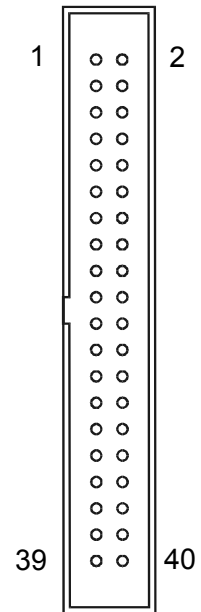
| Pin | Signal name    | Pin | Signal name   |
|-----|----------------|-----|---------------|
| 1   | +5V            | 2   | Keyboard data |
| 3   | Keyboard clock | 4   | GND           |
| 5   | +5V            | 6   | +5V           |
| 7   | Mouse data     | 8   | Mouse clock   |
| 9   | Ground         | 10  | Ground        |



### PL3 - 4 x COMS ports

Connector: 40-way 0.1" IDC header.

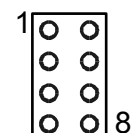
| Pin | Signal name | Pin | Signal name |
|-----|-------------|-----|-------------|
| 1   | N/C         | 2   | N/C         |
| 3   | N/C         | 4   | N/C         |
| 5   | RX/TX+      | 6   | RX/TX-      |
| 7   | RX+         | 8   | RX-         |
| 9   | N/C         | 10  | GND         |
| 11  | DSR3        | 12  | GND         |
| 13  | RX3         | 14  | TX3         |
| 15  | DTR3        | 16  | DCD3        |
| 17  | RTS3        | 18  | CTS3        |
| 19  | RI3         | 20  | N/C         |
| 21  | DCD2        | 22  | DSR2        |
| 23  | RX2         | 24  | RTS2        |
| 25  | TX2         | 26  | CTS2        |
| 27  | DTR2        | 28  | RI2         |
| 29  | GND         | 30  | N/C         |
| 31  | DCD1        | 32  | DSR1        |
| 33  | RX1         | 34  | RTS1        |
| 35  | TX1         | 36  | CTS1        |
| 37  | DTR1        | 38  | RI1         |
| 39  | GND         | 40  | N/C         |



### PL5 - SSI

Connector: 8-way 2mm header.

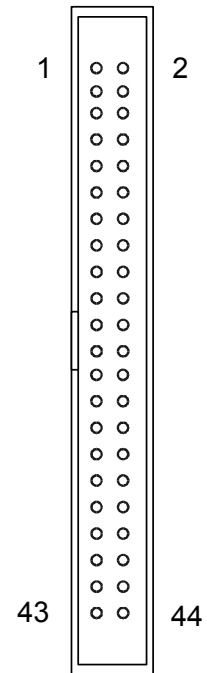
| Pin | Signal name | Pin | Signal name |
|-----|-------------|-----|-------------|
| 1   | +5V         | 2   | Ground      |
| 3   | +5V         | 4   | Data in     |
| 5   | Data out    | 6   | Clock       |
| 7   | CS1         | 8   | CS2         |



## PL6 - IDE HDD connector

Connector: 44-way 2mm IDC header.

| Pin | Signal name | Pin | Signal name |
|-----|-------------|-----|-------------|
| 1   | /RESET      | 2   | Ground      |
| 3   | D7          | 4   | D8          |
| 5   | D6          | 6   | D9          |
| 7   | D5          | 8   | D10         |
| 9   | D4          | 10  | D11         |
| 11  | D3          | 12  | D12         |
| 13  | D2          | 14  | D13         |
| 15  | D1          | 16  | D14         |
| 17  | D0          | 18  | D15         |
| 19  | Ground      | 20  | No connect  |
| 21  | DREQ        | 22  | Ground      |
| 23  | /IOW        | 24  | Ground      |
| 25  | /IOR        | 26  | Ground      |
| 27  | /IOCHRDY    | 28  | Ground      |
| 29  | DACK        | 30  | Ground      |
| 31  | INTR        | 32  | /IOCS16     |
| 33  | A1          | 34  | No connect  |
| 35  | A0          | 36  | A2          |
| 37  | /CS0        | 38  | /CS1        |
| 39  | LED         | 40  | Ground      |
| 41  | VCC         | 42  | VCC         |
| 43  | GND         | 44  | GND         |



## PL8 and PL9 - PC/104 interface

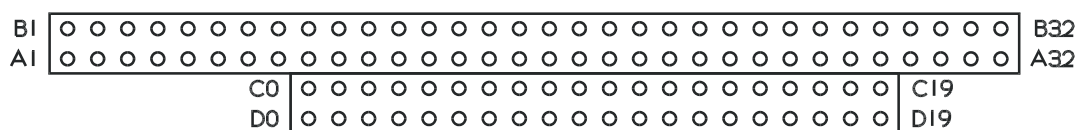
Both 8-bit and 16-bit modules can be fitted to the PEGASUS. The board complies with the PC/104 specification with the exception that the /MASTER and REFRESH signal lines are not implemented on the 40-way connector. The PEGASUS is therefore the only master allowed in the system.

Take care when installing modules, especially 16-bit types. Ensure that all the pins are correctly aligned with the sockets on the PEGASUS before pushing home. Secure the module with the fixing kit provided.

Connector (Row A and B): 64 way 0.1" Non-stackthrough PC/104 compatible connector.

Connector (Row C and D): 40 way 0.1" Non-stackthrough PC/104 compatible connector.

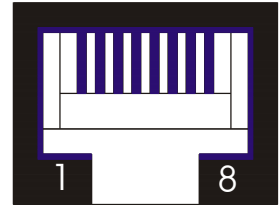
| Pin | Row A   | Row B    | Row C  | Row D    |
|-----|---------|----------|--------|----------|
| 0   | -       | -        | Ground | Ground   |
| 1   | /IOCHCK | Ground   | /SBHE  | /MEMCS16 |
| 2   | D7      | RSTDRV   | LA23   | /IOCS16  |
| 3   | D6      | +5V      | LA22   | IRQ10    |
| 4   | D5      | IRQ9     | LA21   | IRQ11    |
| 5   | D4      | -5V      | LA20   | IRQ12    |
| 6   | D3      | DRQ2     | LA19   | IRQ15    |
| 7   | D2      | -12V     | LA18   | IRQ14    |
| 8   | D1      | /ENDXFR  | LA17   | /DACK0   |
| 9   | D0      | +12V     | /MEMR  | DRQ0     |
| 10  | IOCHRDY | KEY      | /MEMW  | /DACK5   |
| 11  | AEN     | /SMEMW   | D8     | DRQ5     |
| 12  | A19     | /SMEMR   | D9     | /DACK6   |
| 13  | A18     | /IOW     | D10    | DRQ6     |
| 14  | A17     | /IOR     | D11    | /DACK7   |
| 15  | A16     | /DACK3   | D12    | DRQ7     |
| 16  | A15     | DRQ3     | D13    | +5V      |
| 17  | A14     | DACK1    | D14    | MASTER   |
| 18  | A13     | DRQ1     | D15    | Ground   |
| 19  | A12     | /REFRESH | KEY    | Ground   |
| 20  | A11     | SYSCLK   | -      | -        |
| 21  | A10     | IRQ7     | -      | -        |
| 22  | A9      | IRQ6     | -      | -        |
| 23  | A8      | IRQ5     | -      | -        |
| 24  | A7      | IRQ4     | -      | -        |
| 25  | A6      | IRQ3     | -      | -        |
| 26  | A5      | /DACK2   | -      | -        |
| 27  | A4      | TC       | -      | -        |
| 28  | A3      | BALE     | -      | -        |
| 29  | A2      | +5V      | -      | -        |
| 30  | A1      | OSC      | -      | -        |
| 31  | A0      | Ground   | -      | -        |
| 32  | Ground  | Ground   | -      | -        |



### PL10 - Ethernet RJ45

Connector: 8-way RJ45.

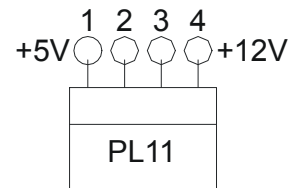
| Pin | Signal name |
|-----|-------------|
| 1   | TX+         |
| 2   | TX-         |
| 3   | RX+         |
| 4   | No connect  |
| 5   | No connect  |
| 6   | RX-         |
| 7   | No connect  |
| 8   | No connect  |



### PL11 - Power

Connector: 4-way Molex.

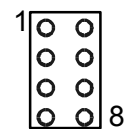
| Pin | Signal name |
|-----|-------------|
| 1   | +5V         |
| 2   | GND         |
| 3   | VBAT        |
| 4   | +12V        |



### PL12 - Ethernet status LEDs

Connector: 6-way 2mm pin header.

| Pin | Signal name | Pin | Signal name |
|-----|-------------|-----|-------------|
| 1   | RX/TX       | 2   | GND         |
| 3   | 10-BaseT    | 4   | GND         |
| 5   | 100-BaseT   | 6   | GND         |



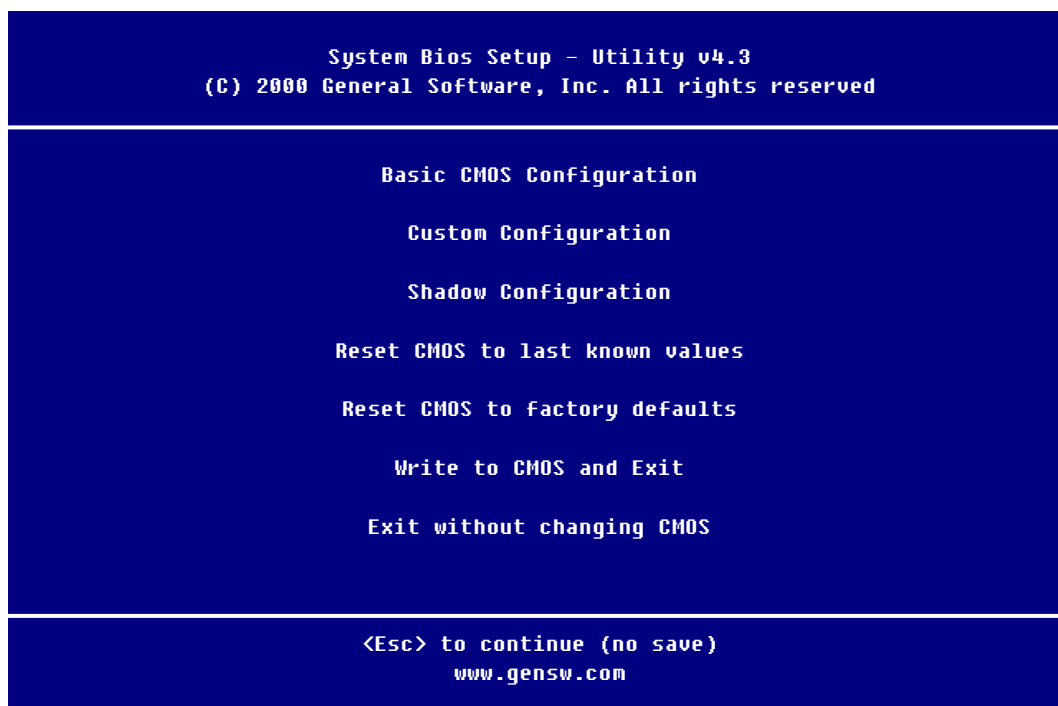
## General Software’s BIOS set-up

The BIOS setup screen is loaded during the POST (Power On Self Test) memory count up display. If the console is the PC keyboard and video monitor, then press the **Del** key during the POST. If the console is a serial link, then press **^C**.

The following table shows the control keys available in serial and VGA console modes:

| Key (serial console mode) | Key (VGA console mode) | Action                                     |
|---------------------------|------------------------|--|
| <b>^E</b>                 | <b>Up arrow</b>        | Up   |
| <b>^X</b>                 | <b>Down arrow</b>      | Down                                       |
| <b>N/A</b>                | <b>Left arrow</b>      | Left                                       |
| <b>N/A</b>                | <b>Right arrow</b>     | Right                                      |
| <b>Tab</b>                | <b>Tab</b>             | Next cell                                  |
| <b>+ / -</b>              | <b>+ / -</b>           | Change selection                           |
| <b>Esc</b>                | <b>Esc</b>             | Go to previous menu (or exit without save) |

The *BIOS Setup* main menu looks like this:



The following sections explain each of these options.



## Basic CMOS Configuration screen

The *Basic CMOS Configuration* screen looks like this:

| System Bios Setup - Basic CMOS Configuration<br>(C) 2000 General Software, Inc. All rights reserved   |   |   |
|---|---|---|
| <b>DRIVE ASSIGNMENT ORDER:</b><br>Drive A: (None)<br>Drive B: (None)<br>Drive C: (None)<br>Drive D: (None)<br>Drive E: (None)<br>Drive F: (None)<br>Drive G: (None)<br>Drive H: (None)<br>Drive I: (None)<br>Drive J: (None)<br>Drive K: (None) | Date:>Jan 01, 1980<br>Time: 00 : 23 : 45<br>NumLock: Disabled<br><br><b>BOOT ORDER:</b><br>Boot 1st: Drive C:<br>Boot 2nd: (None)<br>Boot 3rd: (None)<br>Boot 4th: (None)<br>Boot 5th: (None)<br>Boot 6th: (None) | Typematic Delay : 250 ms<br>Typematic Rate : 30 cps<br>Seek at Boot : None<br>Show "Hit Del" : Enabled<br>Config Box : Enabled<br>Parity Checking : (Unused)<br>Memory Test Tick : (Unused)<br>Test Above 1 MB : Enabled<br>Debug Breakpoints: Disabled<br>Splash Screen : (Unused) |
| Boot Method: Boot Sector<br><b>FLOPPY DRIVE TYPES:</b><br>Floppy 0: Not installed<br>Floppy 1: Not installed  | <b>IDE DRIVE GEOMETRY:</b> Sect Hds Cyls<br>Ide 0: 3 = AUTOCONFIG, LBA<br>Ide 1: Not installed<br>Ide 2: Not installed<br>Ide 3: Not installed  | <b>Memory</b><br>Base:<br>640KB<br>Ext:<br>31MB   |

There are three variables on this screen that you need to set to configure a drive:

- *DRIVE ASSIGNMENT ORDER.*
- *BOOT ORDER.*
- *IDE DRIVE GEOMETRY (drive type).*

These are described in the following sections.

### Configuring drive assignments

There is an extra field at the boot of the *Drive Assignment Order* column: *Boot Method*. For normal use of booting an OS from the boot sector of the selected drive select *Boot Sector*. If *Windows CE* is selected the BIOS will attempt to load and execute a Windows CE Kernel file (NK.BIN), from the root directory of a selected drive.

### Determining boot order

Use the *Boot Order* column to determine the order in which the PEGASUS attempts to boot from a drive. Set this to your required boot order. If a valid boot record is not found on the first drive, the BIOS attempts to boot from the next drive.

## Configuring IDE drive types

If an IDE device is assigned a drive letter in the *Drive Assignment Order* column, then the IDE drives must be configured in the *IDE Drive Geometry* column as follows:

- IDE 0: IDE Primary Master Device (on-board IDE).
- IDE 1: IDE Primary Slave Device (on-board IDE).
- IDE 2: IDE Secondary Master Device (not used).
- IDE 3: IDE Secondary Slave Device (not used).

To use the primary IDE drive on the PEGASUS, follow these steps:

- 1 Configure IDE 0 in the *IDE Drive Geometry* column.
- 2 Map IDE 0 to drive C: in the *Drive Assignment Order* column.
- 3 Set the required boot order in the *Boot Order* column.

The IDE devices can be configured in one of five different modes:

- *None*.
- *User*. Lets you manually select the number of cylinders, heads, and sectors associated with the IDE device.
- *Physical*. The BIOS auto-detects the drive geometry at POST. No translation is performed, so the size of the drive is limited to a maximum of 512MB.
- *LBA*. The BIOS auto-detects the drive geometry at POST, translating the geometry using the standard LBA convention. This supports drives up to 16GB.
- *CHS*. The BIOS auto-detects the drive geometry at POST, translating the geometry using the Phoenix CHS convention. This supports drives up to 16GB.

## Booting a CD-ROM

To boot a CD-ROM, follow these steps:

- 1 Depending on the configuration, set the drive assignment A: to *CD FL/Pri Master* or *CD FL/Pri Slave*.
- 2 Set the first boot order to *Drive A:*.
- 3 Make sure *Not installed* is selected in the *IDE Drive Geometry* column for the CD-ROM device.

An example of the screen with these settings selected is shown below:

| System Bios Setup – Basic CMOS Configuration<br>(C) 2000 General Software, Inc. All rights reserved   |  |   |  |
|---|--|---|--|
| DRIVE ASSIGNMENT ORDER:<br>Drive A: CD FL/Pri Slave<br>Drive B: (None)<br>Drive C: (None)<br>Drive D: (None)<br>Drive E: (None)<br>Drive F: (None)<br>Drive G: (None)<br>Drive H: (None)<br>Drive I: (None)<br>Drive J: (None)<br>Drive K: (None) | Date:>Jan 01, 1980<br>Time: 00 : 23 : 45<br>NumLock: Disabled<br><br>BOOT ORDER:<br>Boot 1st: Drive A:<br>Boot 2nd: (None)<br>Boot 3rd: (None)<br>Boot 4th: (None)<br>Boot 5th: (None)<br>Boot 6th: (None) | Typematic Delay : 250 ms<br>Typematic Rate : 30 cps<br>Seek at Boot : None<br>Show "Hit Del" : Enabled<br>Config Box : Enabled<br>Parity Checking : (Unused)<br>Memory Test Tick : (Unused)<br>Test Above 1 MB : Enabled<br>Debug Breakpoints: Disabled<br>Splash Screen : (Unused) |  |
| Boot Method: Boot Sector<br>FLOPPY DRIVE TYPES:<br>Floppy 0: Not installed<br>Floppy 1: Not installed   | IDE DRIVE GEOMETRY: Sect Hds Cyls<br>Base:<br>Ide 0: Not installed<br>Ide 1: Not installed<br>Ide 2: Not installed<br>Ide 3: Not installed   | Memory<br>640KB<br>Ext:<br>31MB   |  |

The following sections explain each of the relevant fields in the column on the right hand side of the screen.



The fields *Parity Checking*, *Memory Test Tick*, *Debug Breakpoints*, and *Splash Screen* are not used.

## Typematic Delay

The *Typematic Delay* field defines the time between the first and second character being displayed when holding down a key. The options available are summarised in the following table:

| Option          | Explanation  |
|-----------------|--|
| <i>Disabled</i> | Disables the typematic delay.                                  |
| <i>250ms</i>    | Sets the typematic delay to 250 milliseconds (default option). |
| <i>500ms</i>    | Sets the typematic delay to 500 milliseconds.                  |
| <i>750ms</i>    | Sets the typematic delay to 750 milliseconds.                  |
| <i>1000ms</i>   | Sets the typematic delay to 1000 milliseconds.                 |

## Typematic Rate

The *Typematic Rate* field determines the number of characters per second displayed when holding down a key. The options available are summarised in the following table:

| Option        | Explanation   |
|---------------|---|
| <i>6 cps</i>  | Sets the typematic rate to 6 characters per second.                   |
| <i>8 cps</i>  | Sets the typematic rate to 8 characters per second.                   |
| <i>10 cps</i> | Sets the typematic rate to 10 characters per second.                  |
| <i>15 cps</i> | Sets the typematic rate to 15 characters per second.                  |
| <i>20 cps</i> | Sets the typematic rate to 20 characters per second.                  |
| <i>24 cps</i> | Sets the typematic rate to 24 characters per second.                  |
| <i>30 cps</i> | Sets the typematic rate to 30 characters per second (default option). |

## Seek at Boot

During POST the BIOS can access an IDE device. This can be used to force a hard drive or CD-ROM to 'spin up'. In the *Seek at Boot* field, select *IDE* if you are having difficulty booting from a hard drive or CD-ROM. The options available are summarised in the following table:

| Option          | Explanation                          |
|-----------------|--------------------------------------|
| <i>Disabled</i> | Disable the seek (default option).   |
| <i>IDE</i>      | Seek the primary IDE device at boot. |
| <i>Floppy</i>   | Not used.                            |

## Show "Hit Del"

The *Show "Hit Del"* field enables or disables the prompt *Hit Del for setup* to enter the setup screen during boot up. You can disable this prompt to speed up the boot process. The options available are summarised in the following table:

| Option          | Explanation                          |
|-----------------|--------------------------------------|
| <i>Disabled</i> | Disable the message.                 |
| <i>Enabled</i>  | Enable the message (default option). |

## Config Box

The *Config Box* field allows you to disable the configuration screen that is displayed at the end of POST. The options available are summarised in the following table:

| Option          | Explanation                                       |
|-----------------|---|
| <i>Disabled</i> | Disable the configuration screen.                 |
| <i>Enabled</i>  | Enable the configuration screen (default option). |

## Test Above 1MB

The *Test Above 1MB* field is used to enable or disable the memory test above 1MB. You can speed up the boot process by disabling this test. The options available are summarised in the following table:

| Option          | Explanation  |
|-----------------|--|
| <i>Enabled</i>  | The BIOS tests all on-board memory (default option). |
| <i>Disabled</i> | The BIOS only tests the first 1MB of memory.         |

## Custom Configuration screen

The *Custom Configuration* screen looks like this:

```

System BIOS Setup - Custom Configuration
(C) 2000 General Software, Inc. All rights reserved

UART1 (COM1)      :>3F8h          UART2 (COM2)      : 2F8h
UART3 (COM3)      : 3E8h          UART4 (COM4)      : 2E8h
COM1 IRQ          : IRQ 4         COM2 IRQ          : IRQ 3
COM3 IRQ          : IRQ 10        COM4 IRQ          : IRQ 11
CPU speed         : 133 MHz       LPT1 IRQ         : Disabled
FlashFx          : Enabled        Serial Console port : COM1
Serial Console Baud : 115200      Dark Boot Mode   : Disabled
Hard Disk        : Enabled        PS/2 Mouse      : Enabled

^E/^X/<Tab> to select or +/- to modify
<Esc> to return to main menu

```

The following sections explain each of the fields on this screen.

### UART1 (COM1)

The *UART1 (COM1)* field enables or disables the COM1 port. The options available are summarised in the following table:

| Option          | Explanation   |
|-----------------|---|
| <i>3F8h</i>     | Sets COM1 to be at base address 3F8h (default option).            |
| <i>Disabled</i> | Disables COM1, so the address 3F8h is no longer decoded to UART1. |

### UART2 (COM2)

The *UART2 (COM2)* field enables or disables the COM2 port. The options available are summarised in the following table:

| Option          | Explanation   |
|-----------------|---|
| <i>2F8h</i>     | Sets COM1 to be at base address 2F8h (default option).            |
| <i>Disabled</i> | Disables COM2, so the address 2F8h is no longer decoded to UART2. |

### UART3 (COM3)

The *UART3 (COM3)* field enables or disables the COM3 port. The options available are summarised in the following table:

| Option          | Explanation   |
|-----------------|---|
| <i>3E8h</i>     | Sets COM1 to be at base address 3E8h (default option).            |
| <i>Disabled</i> | Disables COM3, so the address 3E8h is no longer decoded to UART3. |

### UART4 (COM4)

The *UART4 (COM4)* field enables or disables the COM4 port. The options available are summarised in the following table:

| Option          | Explanation   |
|-----------------|---|
| <i>2E8h</i>     | Sets COM1 to be at base address 2E8h (default option).            |
| <i>Disabled</i> | Disables COM4, so the address 2E8h is no longer decoded to UART4. |

### COM1 IRQ

The *COM1 IRQ* field sets the COM1 IRQ. The options available are summarised in the following table:

| Option          | Explanation                          |
|-----------------|--------------------------------------|
| <i>IRQ4</i>     | Sets COM1 IRQ to 4 (default option). |
| <i>Disabled</i> | Disables COM1 IRQ.                   |

### COM2 IRQ

The *COM2 IRQ* field sets the COM2 IRQ. The options available are summarised in the following table:

| Option          | Explanation                          |
|-----------------|--------------------------------------|
| <i>IRQ3</i>     | Sets COM2 IRQ to 3 (default option). |
| <i>Disabled</i> | Disables COM2 IRQ.                   |

### COM3 IRQ

The *COM3 IRQ* field sets the COM3 IRQ. The options available are summarised in the following table:

| Option          | Explanation                           |
|-----------------|---------------------------------------|
| <i>IRQ10</i>    | Sets COM3 IRQ to 10 (default option). |
| <i>Disabled</i> | Disables COM3 IRQ.                    |

## COM4 IRQ

The *COM4 IRQ* field sets the COM4 IRQ. The options available are summarised in the following table:

| Option          | Explanation                           |
|-----------------|---------------------------------------|
| <i>IRQ4</i>     | Sets COM4 IRQ to 11 (default option). |
| <i>Disabled</i> | Disables COM4 IRQ.                    |

## CPU speed

The SC520 processor can run at two different speeds: 133MHz and 100MHz. You can use the *CPU speed* field to change the speed in order to save power, and to enable you to run the processor at higher temperatures. The options available are summarised in the following table:

| Option        | Explanation                                   |
|---------------|---|
| <i>133MHz</i> | Run the processor at 133MHz (default option). |
| <i>100MHz</i> | Run the processor at 100MHz.                  |

## LPT1 IRQ

The *LPT1 IRQ* field sets the LPT1 IRQ. The options available are summarised in the following table:

| Option          | Explanation                         |
|-----------------|-------------------------------------|
| <i>IRQ7</i>     | Sets LPT1 IRQ to 7.                 |
| <i>Disabled</i> | Disables LPT1 IRQ (default option). |

## FlashFX

The *FLASHFX* field enables or disables the Flash filing system. The options available are summarised in the following table:

| Option          | Explanation   |
|-----------------|---|
| <i>Enabled</i>  | The board is able to boot to the on-board Flash (default option). |
| <i>Disabled</i> | The board is not able to boot the Flash.                          |

## Serial Console port

The *Serial Console port* field sets the current serial console port. The options available are summarised in the following table:

| Option      | Explanation   |
|-------------|---|
| <i>COM1</i> | Sets the current console port to COM1 (default option). |
| <i>COM2</i> | Sets the current console port to COM2.                  |
| <i>COM3</i> | Sets the current console port to COM3.                  |
| <i>COM4</i> | Sets the current console port to COM4.                  |



## Serial Console Baud

The *Serial Console Baud* field sets the baud rate for the current serial console port. The options available are summarised in the following table:

| Option | Explanation  |
|--------|--|
| 9600   | Sets the current console baud rate to 9600.                    |
| 19200  | Sets the current console baud rate to 19200.                   |
| 38400  | Sets the current console baud rate to 38400.                   |
| 115200 | Sets the current console baud rate to 115200 (default option). |

## Dark Boot Mode

Enabling *Dark Boot Mode* disables all console activity to the serial console. You can turn the console on again by issuing a software interrupt, as follows:

INT15

Called with:

AH - Alh

BX specifies the console device, 0 indicates a VGA console (VGA and keyboard), and nonzero values indicate the COM port number (starting with 1 for COM1).

Returns:

CY - Clear if successful.

AH - Status error code.

00h - No error.

86h - Not supported by BIOS configuration.

For example code, please refer to the software section on the supplied Development Kit CD.

## Hard Disk

The *Hard Disk* field enables or disables the IDE interface. When disabled, IRQ14 is available on the PC104 interface. The options available are summarised in the following table:

| Option          | Explanation                             |
|-----------------|---|
| <i>Enabled</i>  | IDE interface enabled (default option). |
| <i>Disabled</i> | IDE interface disabled.                 |

## PS/2 Mouse

The *PS/2 Mouse* field enables or disables the PS/2 mouse interface. When disabled IRQ12 is available on the PC104 interface. The options available are summarised in the following table:

| Option          | Explanation                                    |
|-----------------|--|
| <i>Enabled</i>  | PS/2 mouse interface enabled (default option). |
| <i>Disabled</i> | PS/2 mouse interface disabled.                 |

## Shadow Configuration Setup screen

Use the system *Shadow Configuration Setup* screen to enable and disable the shadowing of areas of ISA ROM regions. Normally shadowing should be enabled at E000-F000 to maximise system ROM BIOS performance, and any other region that a ROM BIOS extension may be executed from.

## Other setup options

The following options are also available:

| Option                                 | Explanation  |
|--|--|
| <i>Reset CMOS to last known values</i> | Causes the setup program to restore the CMOS values it had prior to any edits performed in the current session.                        |
| <i>Reset CMOS to factory defaults</i>  | Causes the setup program to restore the CMOS values to the hard coded factory settings. This is the same as removing the battery link. |
| <i>Write CMOS and Exit</i>             | Causes the setup program to save the current edits to the CMOS and reboots the board, causing the new values to load.                  |
| <i>Exit without changing CMOS</i>      | Causes the setup program to exit, without saving any changes made during the current session.  |

## Software support

---

The Development Kit contains a support CD-ROM that contains reference material and software utilities to support the PEGASUS. The following sections describe the software support and provide guidelines for using the drivers supplied on the CD.

### Datalight ROM-DOS 6.22

If your PEGASUS board is fitted with Flash memory it is supplied with a license for Datalight's ROM-DOS 6.22 operating system. This operating system is pre-installed on the Flash drive.

ROM-DOS is a Microsoft MS-DOS compatible operating system, which has been specifically designed for embedded systems. The system and command files are physically much smaller, but still provide full compatibility to allow standard DOS applications to run without modification. ROM-DOS supports all the standard utility files like SYS, PRINT, MODE, FDISK, FORMAT, etc. These files are supplied on the support CD-ROM and can be used as required.

A full user manual for ROM-DOS is supplied on the CD, which provides detailed information on the operating system and supported interrupts and features.

### Datalight FlashFX Flash filing system

The Flash memory incorporated onto the PEGASUS is configured as a silicon read/write disk drive. This disk is supported using Datalight's FlashFX software. This software is designed to allow the disk to be accessed using standard DOS routines. The FlashFX software is installed during the POST process as a BIOS extension. This enables the Flash disk to be used as a boot disk and is the default boot device if a hard disk drive is not present in the system. When shipped, the Flash memory is formatted and configured as a ROM-DOS system disk.

The FlashFX software has been designed to incorporate wear levelling algorithms. The wear levelling ensures that the Flash memory is used evenly and that no one sector is continually being written to. This maximises the write performance of the Flash device.

The support CD contains utilities that can be used to ensure that the Flash disk is configured correctly (see the README file in the FlashFX section of the support CD-ROM). If the Flash disk becomes corrupted for any reason you can use these utilities to reformat the Flash. The CD can be used as a 'boot disk', providing an automatic mechanism for reformatting the Flash memory and copying the ROM-DOS operating system.

## FUPDATE utility

The FUPDATE utility is used to update the BIOS used on the board. This may be required if you experience any incompatibilities with the BIOS and a later version is available. Please contact Eurotech if you require support that is not in the standard BIOS. The FUPDATE utility can be invoked from the DOS command line and should be supplied with the BIOS image file name required, i.e. FUPDATE BIOS.BIN. The program will automatically load the file and prompt you to confirm that you want to reprogram the BIOS ROM. Once the device has been reprogrammed you should reboot the system.

The FUPDATE utility can be found in the “\BIOS” directory on the ROMDOS Development Kit CD-ROM.



Make sure **no** memory managers or TSR are running, as this would cause the update to fail. Also during this process it is important that you do not switch off the board as this may corrupt the BIOS ROM, which would stop the board from operating.

---

## Boot disk

The development CD-ROM is also a boot disk. A menu is provided once the board has started to boot to allow you to perform some pre-defined operations. These include reformatting the Flash disk, copying the system files to the Flash disk, and re-installing the Development Kit Flash image. Once the appropriate selection has been made the software performs the operation automatically.

## Example code

The development CD-ROM contains example code for various PEGASUS board functions:

- SSI.
- Watchdog.
- User links.

You can find these in the “\EXAMPLE” directory on the CD-ROM.

## Hardware support information

---

As the PEGASUS is a compatible PC/AT processor board, any standard PC reference guide will provide information on hardware aspects of the board. The following material has been included on the support CD-ROM as it relates to specific features of the board, which may not be available from other sources. The following information is stored in the REFERENCE directory:

- AMD SC520 data sheet.
- National Semiconductors DP83815 Ethernet Controller data sheet.
- SMSC 37B727 SuperIO Controller data sheet.
- Intel Strata Flash data sheet.
- PC/104 specification.

Please refer to the documentation on the CD-ROM for the latest information.

If you are trying to locate information on a specific function that is not included above, refer to [Appendix B – Reference information](#), page 47, for links to some relevant internet sites.

## Appendix A – Specification

---

|                                 |   |
|---------------------------------|---|
| <b>Temperature</b>              | Operating -20°C to 70°C.<br>Storage -20°C to +85°C.                           |
| <b>Humidity</b>                 | 10% to 90% RH (non-condensing).   |
| <b>Real time clock accuracy</b> | +/- 1min/month.   |
| <b>Software</b>                 | Datalight ROM-DOS operating system.<br>Datalight FlashFX Flash filing system. |
| <b>Power requirements</b>       | +5V +/- 5% 800mA (typical), 1.0A (max).                                       |
| <b>Battery</b>                  | 3.0V lithium 180mAH (CR2032 coin cell).<br>Maximum discharge current 2uA.     |
| <b>Dimensions</b>               | PC/104 compatible format.<br>90.8mm x 90.4mm (3.575" x 3.550").               |
| <b>Weight</b>                   | 96 grams.   |
| <b>MTBF</b>                     | 150,000 hours, based on MIL-HDBK-217F using generic failure rates.            |

## Appendix B – Reference information

---

### *Product information*

Product notices, updated drivers, support material, 24hr-online ordering:

[www.eurotech.com](http://www.eurotech.com)

### *PC/104 Consortium*

PC/104 and PC/104-Plus specifications, vendor information, and available add-on products:

[www.pc104.org](http://www.pc104.org)

### *PCI Special Interest Group*

PCI Bus specification and list of manufacturers:

[www.pcisig.org](http://www.pcisig.org)

### *AMD*

AMD Élan™ SC520 processor documentation:

[www.amd.com](http://www.amd.com)

### *SMSC*

SMSC Super I/O documentation:

[www.smisc.com](http://www.smisc.com)

### *Datalight Inc.*

ROM-DOS and FlashFX information:

[www.datalight.com](http://www.datalight.com)

### *General Software*

BIOS documentation and support material:

[www.gensw.com](http://www.gensw.com)

## Appendix C – Troubleshooting

---

The PEGASUS board is delivered 'ready to run' and automatically starts running and loading an operating system when power is applied, either from the on-board Flash memory or mechanical disk drive. Once the board is running, you can refer to the information in this manual for connection details and guidelines to attach peripherals, and for general help when using the board.

If you are experiencing problems with a particular feature of the board, please refer to the relevant documentation to ensure that the board is configured correctly. If you are still unable to resolve the problem then contact Eurotech's technical support team who are able to offer advice and investigate the problem (see page [51](#)).

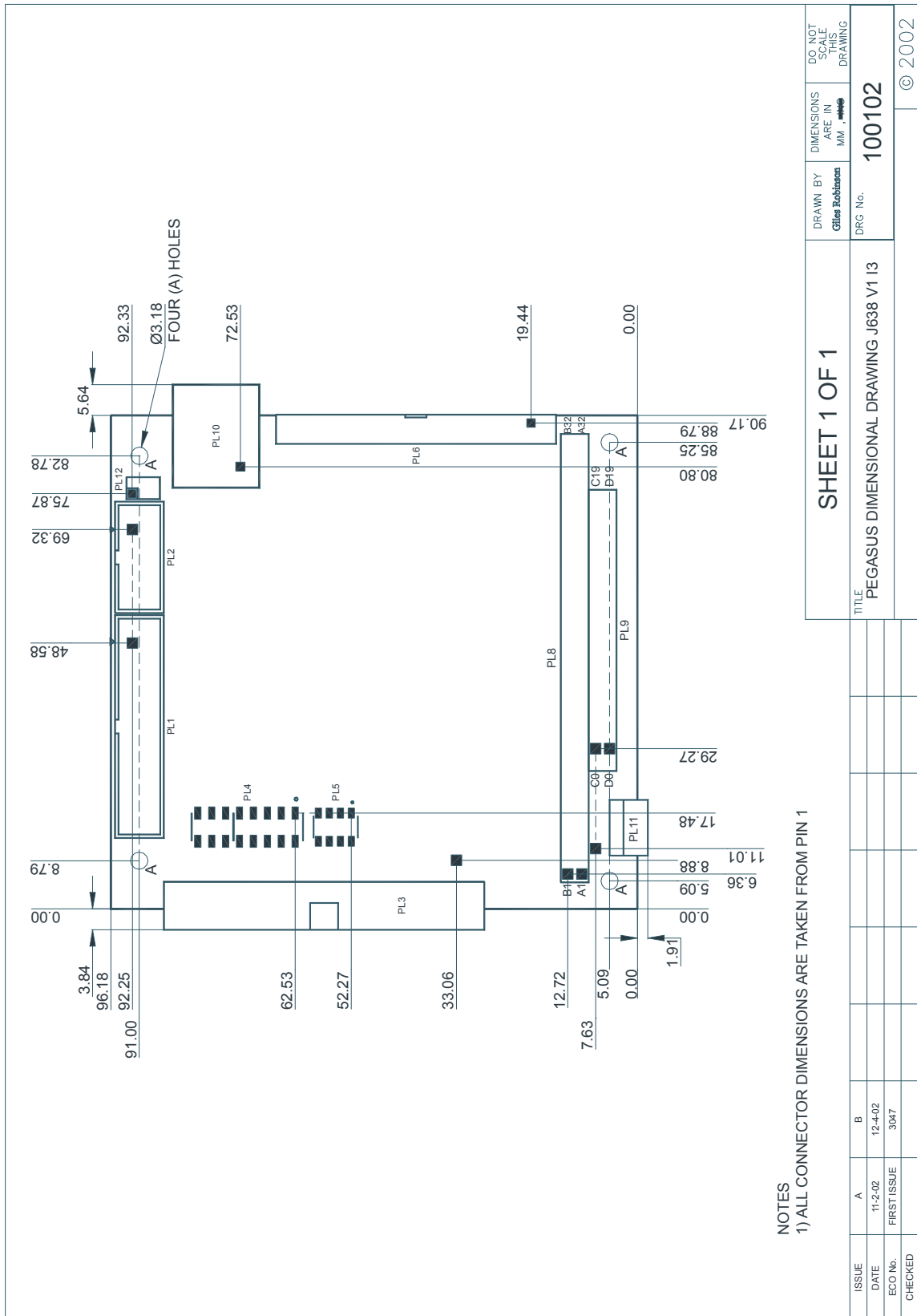
If the board does not start running when power is applied and the display remains blank, then there may be a problem with the system configuration. Follow the steps below to determine the cause of the problem:

- 1 Switch **off** the PEGASUS and disconnect from the power. Switch **on** the power supply and measure the output voltage with a digital voltmeter (DVM). This should be between +4.85V and +5.25V. If it is not, adjust the output voltage and re-apply the power to the board. If the board still does not work, go to step 2.
- 2 With the power supply connected and switched **on**, check the voltage at the power connector PL11 between pin 1 (+5V) and pin 2 (GND). If this voltage is outside the tolerance stated in step 1, adjust the supply until it meets the specification. The board should automatically start running when the supply reaches the minimum voltage, but it is safest to switch **off** then **on** again to make sure that the board starts correctly. If the board still does not work, go to step 3.
- 3 Remove any PC/104 adapter boards plugged into the PEGASUS. Apply power to the board and see if it starts working. If the board starts to boot check the link settings on the PC/104 boards to ensure that they do not conflict with devices on the PEGASUS. Once the settings have been checked replace the PC/104 board and apply power. If the board still does not work, go to step 4.
- 4 Check all link settings are in the default location as detailed in the section [Links](#), page [23](#), and remove all cables except coms and the power supply cable. Apply power and check to see if the board starts correctly.

If you have completed all of the above steps and the board still fails to operate, then you will need to return it to Eurotech for repair. Please contact the technical support department who will be able to provide details of the returns procedure (see page [51](#)).



# Appendix D – Mechanical drawing

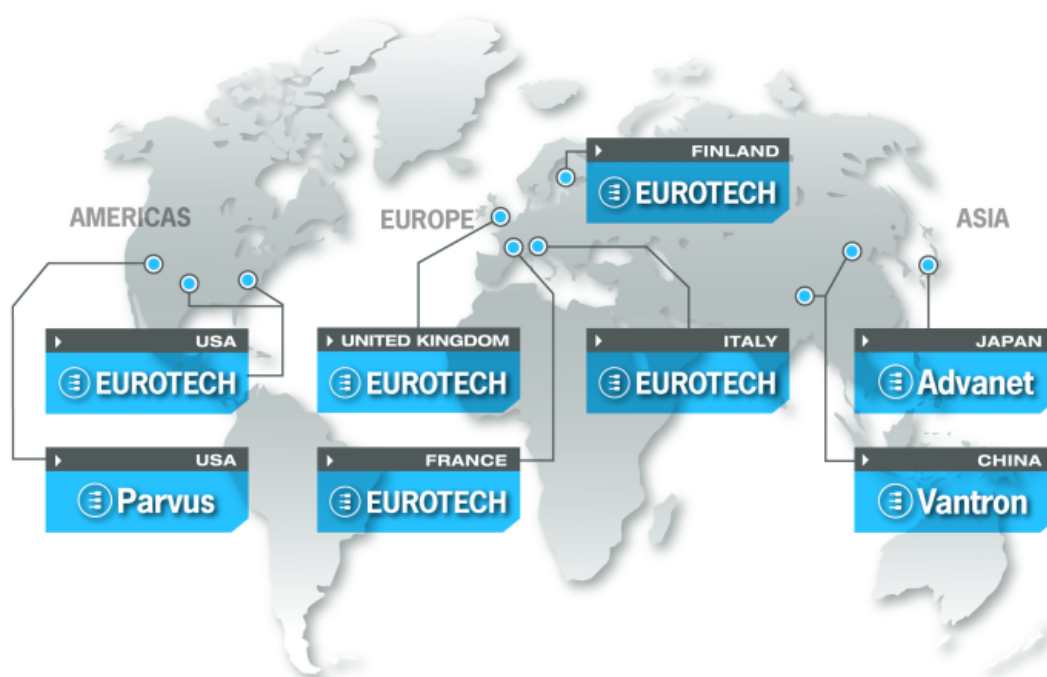


NOTES  
1) ALL CONNECTOR DIMENSIONS ARE TAKEN FROM PIN 1

|   |             |                             |                                    |
|---|-------------|-----------------------------|------------------------------------|
| DRAWN BY<br><b>Cliff Robinson</b>               |             | DIMENSIONS<br>ARE IN<br>MM. | DO NOT<br>SCALE<br>THIS<br>DRAWING |
| DRG No. <b>100102</b>                           |             |                             |                                    |
| <b>SHEET 1 OF 1</b>                             |             |                             |                                    |
| TITLE<br>PEGASUS DIMENSIONAL DRAWING J638 V1 I3 |             |                             |                                    |
| ISSUE   | A           | B                           |                                    |
| DATE  | 11-2-02     | 12-4-02                     |                                    |
| ECO No.   | FIRST ISSUE | 3047                        |                                    |
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# Eurotech Group Worldwide Presence



## AMERICAS

## EUROPE

## ASIA



### North America

#### EUROTECH USA

US toll free +1 800.541.2003  
 tel. +1 301.490.4007  
 fax +1 301.490.4582  
 e-mail: sales.us@eurotech.com  
 e-mail: support.us@eurotech.com  
 www.eurotech-inc.com

#### PARVUS CORPORATION

US toll-free +1 800.483.3152  
 tel. +1 801.483.1533  
 fax +1 801.483.1523  
 e-mail: sales@parvus.com  
 e-mail: tsupport@parvus.com  
 www.parvus.com

### Central & Southern Europe

#### EUROTECH Italy

tel. +39 0433.485.411  
 fax +39 0433.485.499  
 e-mail: sales.it@eurotech.com  
 e-mail: support.it@eurotech.com  
 www.eurotech.com

#### Western Europe

#### EUROTECH UK

tel. +44 (0) 1223.403410  
 fax +44 (0) 1223.410457  
 e-mail: sales.uk@eurotech.com  
 e-mail: support.uk@eurotech.com  
 www.eurotech.com

#### EUROTECH France

tel. +33 04.72.89.00.90  
 fax +33 04.78.70.08.24  
 e-mail: sales.fr@eurotech.com  
 e-mail: support.fr@eurotech.com  
 www.eurotech.com

### Northern & Eastern Europe

#### EUROTECH Finland

tel. +358 9.477.888.0  
 fax +358 9.477.888.99  
 e-mail: sales.fi@eurotech.com  
 e-mail: support.fi@eurotech.com  
 www.eurotech.com

### Japan

#### ADVANET

tel. +81 86.245.2861  
 fax +81 86.245.2860  
 e-mail: sales@advanet.co.jp  
 www.advanet.co.jp

### China

#### VANTRON

tel. +86 28.85.12.39.30  
 fax +86 28.85.12.39.35  
 e-mail: sales@vantrontech.com.cn  
 e-mail: support.cn@eurotech.com  
 www.vantrontech.com.cn

